axelite 亞瑟萊特科技股份有限公司 AXElite Technology Co.,Ltd

USB Dedicated Charging Port Controller for Fast Charging Protocol and QC 2.0/3.0

❖ GENERAL DESCRIPTIO

The AX9291Q is a fast charging protocol controller for HiSilicon Fast Charging Protocol (FCP) and Qualcomm® Quick ChargeTM 2.0/3.0 (QC 2.0/3.0) USB interface. The AX9291Q monitors USB D+/D− data line and automatically adjusts the output voltage depending on different powered device (PD). The charging time of PD is therefore optimized by the AX9291Q.

AX9291Q can support not only USB BC compliant devices, but also Apple / Samsung / HUAWEI devices and automatically detects whether a connected powered device is QC 2.0/3.0 or FCP capable before enabling output voltage adjustment. If a PD is not compliant with QC 2.0/3.0 and FCP, the AX9291Q will disable the adjustment of output voltage and keep the default 5V output voltage for safe operation.

The AX9291Q is available in a space-saving SOT-23-6 package.

❖ FEATURES

- Supports HiSilicon Fast Charging Protocol (FCP)
- Supports Qualcomm® Quick ChargeTM 2.0/3.0 Class A : 3.6V up to 12V Output Voltage
- Automatically Selects FCP and QC2.0/3.0 Protocols
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2
- Complies with Chinese Telecommunication Industry Standard YD/T 1591-2009
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line
- SOT-23-6 Package
- AEC-Q100 Automotive qualified.

❖ **Applications**

- Wall-Adapter, Smart Phones, Tablets, Notebooks
- Mobile / Tablet Power Bank
- Car Charger
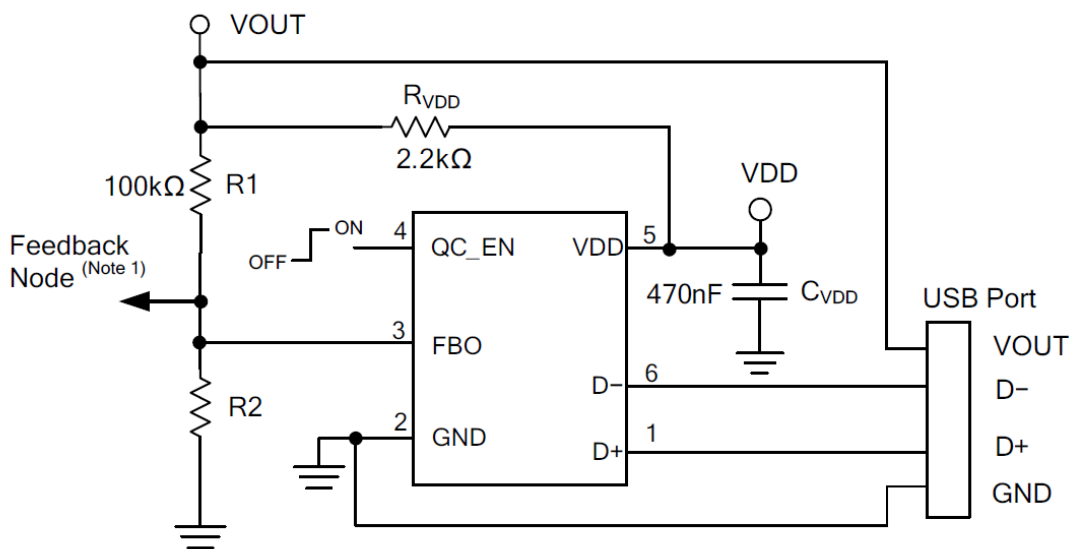- USB Power Output Ports

❖ **BLOCK DIAGRAM**

Figure 2. Typical Application Schematic

Note 1: The recommended voltage of feedback node ranges between 0.4V and 1.5V

Output Voltage Lookup Table (QC 2.0/3.0)

D+	D-	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

❖ **Functional Pin Description**

| Pin Name	Pin No.	Pin Function
D+	1	USB D+ data line. Recommended this pin connect without resistors(open) or with a resistor higher than 1MΩ connect to GND.
GND	2	Ground pin.
FBO	3	Feedback output pin. Current Sink/Source FB Node.
QC_EN	4	QC_Enable: QC2.0/3.0 and FCP function are enabled by either logic high or high-Z. Contrarily, QC2.0/3.0 and FCP function are disabled by logic low.
VDD	5	Power supply input pin.
D−	6	USB D− data line.

❖ **Block Diagram**
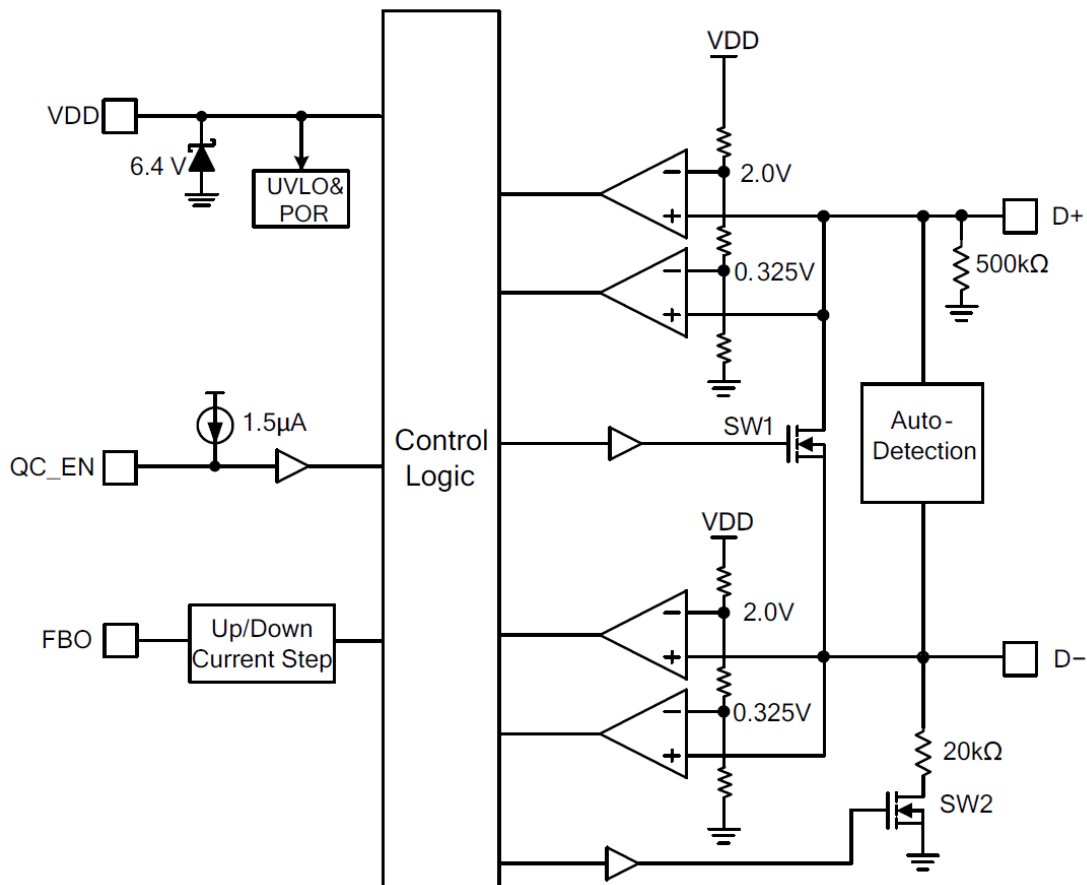
Figure 3. Block Diagram of AX9291Q

Absolute Maximum Ratings (Note 2)

- Input Supply Voltage VDD -- -0.3V to +7V
- D+,D−Pins Voltage -- -0.3V to +14V
- All Other Pins Voltage -- -0.3V to +7V
- Maximum Junction Temperature (T_J) --- +150℃
- Storage Temperature (T_S) --- -65℃ to +150℃
- Lead Temperature (Soldering, 10sec.) -- +260°C
- Package Thermal Resistance, (θ_{JA}) (Note 3)
        SOT-23-6   -- 250°C/W
- Package Thermal Resistance, (θ_{JC})
        SOT-23-6   -- 110°C/W

Note 2: Stresses beyond this listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Note 3: θJA is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

Recommended Operating Conditions

- Input Supply Voltage (VDD) --- +3.2V to +6.8V

- Operation Temperature Range (T_{OPR}) --- -40°C to +85°C

Rev.1.0 Dec.04, 2018

❖ Electrical Characteristics

(VDD=5V, TA=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VDD Input Voltage Range	VDD		3.2		6.8	V
Input UVLO Threshold	VUVLO(VTH)	VDD Falling	2.5		2.9	V
VDD Supply Current		VDD =5V, Measure VDD		180		µA
VDD Shunt Voltage	VDD(SHUNT)	IVDD = 3mA	5.9	6.4	6.8	V
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	VDAT(REF)		0.25	0.325	0.4	V
Output Voltage Selection Reference	VSEL_REF		1.8	2.0	2.2	V
D+ High Glitch Filter Time	TGLITCH(BC)-D+_H		1000	1250	1500	ms
D− Low Glitch Filter Time	TGLITCH(BC)-D−_L			1		ms
Output Voltage Glitch Filter Time	TGLITCH(V) CHANGE		20	40	60	ms
D− Pull-Down Resistance	RD−(DWN)			20		kΩ
Continuous Mode Glitch Filter Time (Note 3)	TGLITCH-CONT-CHANGE		100		200	µs
D+ Leakage Resistance	RDAT-LKG	VDD =3.2-6.4V,VD+=0.6-3.6V Switch SW1=Off	300	500	800	kΩ
Switch SW1 On-Resistance	RDS_ON_N1	VDD =5V,SW1= 200µA			40	Ω
Up/Down Current Step	IUP, IDOWN	IUP = 40µA (9V), 70µA (12V), IDOWN = 14µA (3.6V)		2		µA
Feedback Output Voltage	VFBO		0.4		1.5	V
DCP Charging Mode						
D+_0.48V/D−_0.48V Line Output Voltage			0.44	0.48	0.52	V
D+_0.48V/D−_0.48V Line Output Impedance				900		kΩ

Rev.1.0 Dec.04, 2018

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❖ **Electrical Characteristics (Continued)**

(VDD=5V, TA=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Apple Mode						
D+_2.7V/D−_2.7V Line Output Voltage			2.57	2.7	2.84	V
D+_2.7V/D−_2.7V Line Output Impedance				33.6		kΩ
D− SECTION (FCP)						
D− FCP Tx Valid Output High	VTX-VOH		2.55		3.6	V
D− FCP Tx Valid Output Low	VTX-VOL				0.3	V
D− FCP Rx Valid Output High	VRX-VIH		1.4		3.6	V
D− FCP Rx Valid Output Low	VRX-VIL				1.0	V
D− Output Pull-Low Resistance (FCP) (Note 4)	RPD		400	500	600	Ω
Unit Interval For FCP PHY Communication	UI	fCLK = 125kHz	144	160	180	μs
Others						
QC_EN High-Level Input Voltage	VIH		1.2			V
QC_EN Low-Level Input Voltage	VIL				0.4	V

Note 3: Not production tested.

❖ **PIN ASSIGNMENT**

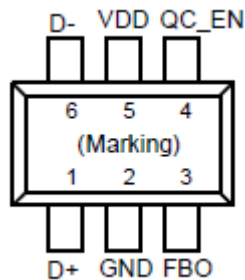The packages of AX9291Q is SOT-23-6; the pin assignment is given by:

Figure 1. Pin Assignment of AX9291Q

Rev.1.0 Dec.04, 2018

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❖ **ORDER/MARKING INFORMATION**

Order Information	Top Marking
AX9291Q X X Package Type Packing C: SOT-23-6L Blank : Tube A : Taping	

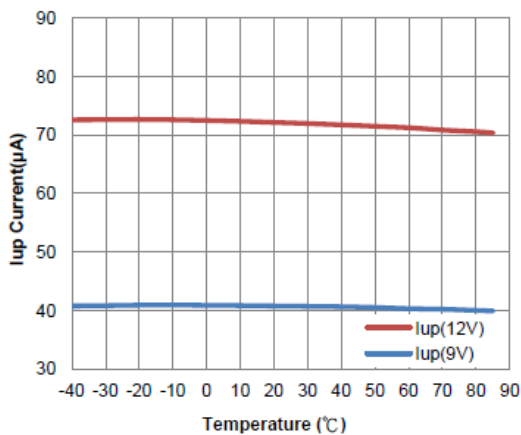| Part Number	Product Code
AX9291QCA	**FT4**

❖ **Typical Performance Curves**

Figure 4. UP Current vs. Temperature
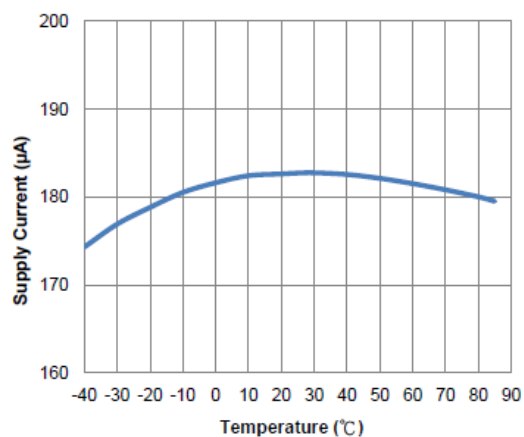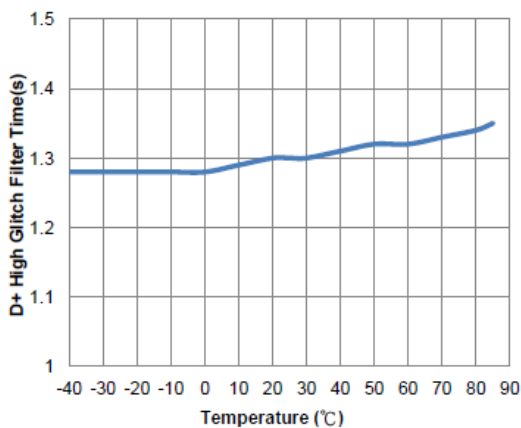

Figure 5. Supply Current vs. Temperature

Figure 6. D+ High Glitch Filter Time vs. Temperature

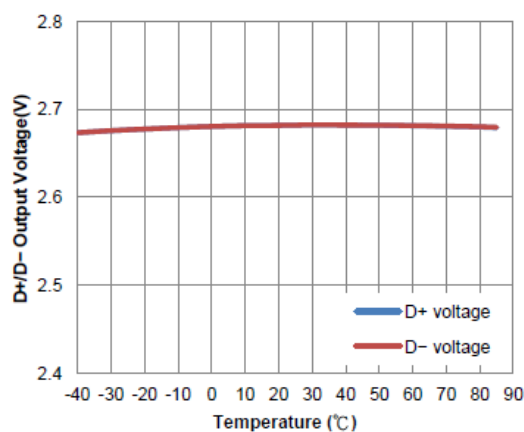Figure 7. D+/D- Output Voltage vs. Temperature

Rev.1.0 Dec.04, 2018

❖ **Application Information**

Function Description

The AX9291Q integrates both USB high voltage dedicated charging port interface IC for Qualcomm$^{®}$ Quick Charge^{TM} 2.0/3.0 class A and

HiSilicon FCP specification.

The AX9291Q can fast charge most of the handheld devices. It could be treated as the original charging adapter.

The AX9291Q supports BC1.2, Samsung and HUAWEI devices. It also supports output voltage range of QC 3.0 Class A (3.6V to 12V) or QC 2.0 Class A (5V, 9V, 12V).

Quick Charge 2.0/3.0 Interface

When the AX9291Q is powered on, D+ and D− pin are applied to 2.7V for Apple device. If handheld device has the function of QC 2.0/3.0, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will short to D− pin through the switch SW1 for entering BC 1.2. If D+ is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the AX9291Q will enter QC 2.0/3.0 or FCP operation mode.

When the voltage of D+ pin and D− pin simultaneously satisfy these two inequalities $V_{DAT(REF)}$< D+ <V_{SEL_REF} and D− > V_{SEL_REF}, the AX9291Q would enter continuous mode.

In the continuous mode, each voltage pulse on D+ pin generated by powered device is between 1V and 3V. In the meanwhile, the high level of pulse should be keep at least 200us. If the specified conditions are satisfied, the FBO pin will sink 2uA per pulse. The maximum sink current is 70uA for output voltage 12V.

In the continuous mode, each voltage pulse on D−pin generated by powered device is between 3V and 1V. At the same time, the low level of pulse should be keep at least 200us. If the specified conditions are satisfied, the FBO pin will source 2uA per pulse. The maximum source current is 14uA for output voltage 3.6V.

If the powered device doesn't support QC 2.0, the AX9291Q will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than $V_{DAT(REF)}$ and the output default voltage 5V is also applied.

Shunt Regulator

The VDD of AX9291Q is supplied by the wide output voltage through the external resistor RVDD. The internal Zener-Diode is utilized to clamp the VDD at 6.4V. The recommended value of RVDD and CVDD are 2.2kΩ and 470nF, respectively.

QC_EN Function

QC 2.0/3.0 and FCP function are disabled by connecting the QC_EN pin to ground. On the contrary, QC 2.0/3.0 and FCP function could be enabled by connecting QC_EN pin to VDD or high-Z. Additionally, when AX9291Q is already accessed QC 2.0/3.0 or FCP mode, the selected mode can't be changed by setting QC_EN pin.

Data Line Protection

When D+/D− pin is touched by the output voltage in abnormal situation, the D+/D− pin of both sink device and source device may be damaged. In order to protect the D+/D− pin of the devices from damage in abnormal situation, the AX9291Q will return the output voltage to default output voltage 5V when the voltage of D+/D− pin is touched larger than 7.5V.
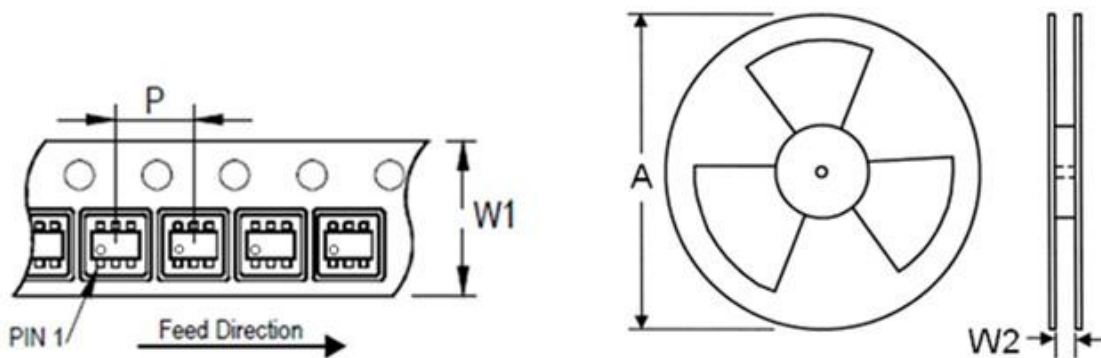
❖ PACKAGE OUTLINES

SOT-23-6 Package (Unit: mm)
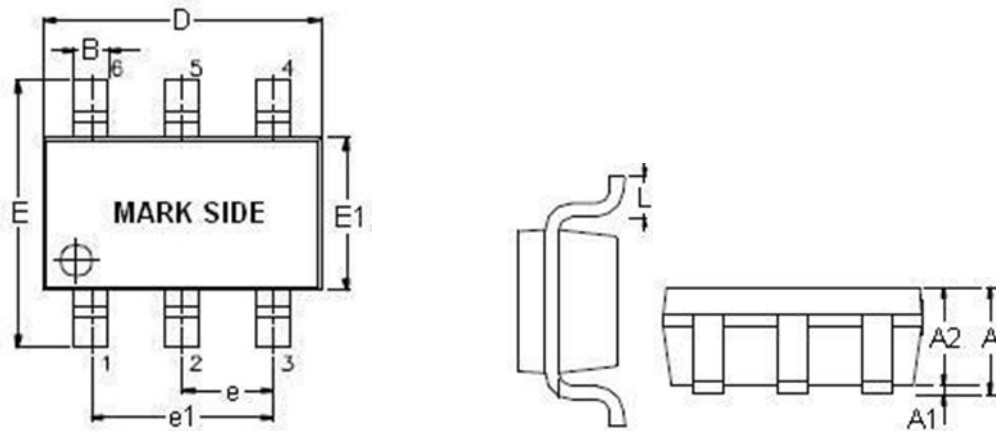
SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note: Followed From JEDEC MO-178-C.

Carrier Dimensions

Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000