N-CH40V Fast Switching MOSFETs

❖ GENERAL DESCRIPTION

The AMN4008 is the high cell density trenched N-ch MOSFETs, which provides excellent RDSON and efficiency for most of the small power switching and load switch applications.

The AMN4008 meet the RoHS and Green Product requirement with full function reliability approved.

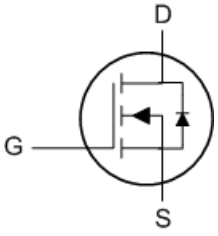
❖ FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

Product Summery

BVDSS	RDSON	ID
40V	37mΩ	4.5A

SOT23 Pin configuration



❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AMN4008 X X Package Type: R: SOT-23-3L Packing: Blank : Bag, A : Taping	B2YW⊠⊠ → ID code: internal WW: 01~26(A~Z), 27~52(a~z) Year: 1= 2011 … 9= 2019 AMN4008

❖ ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current, V_{GS} @ 10V (Note 1)	I_D@T_A=25°C	4.5	A
Continuous Drain Current, V_{GS} @ 10V (Note 1)	I_D@T_A=70°C	3.5	A
Pulsed Drain Current (Note 2)	I_{DM}	14	A
Total Power Dissipation (Note 3)	P_D@T_A=25°C	1	W
Storage Temperature Range	T_{STG}	-55 to 150	°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Thermal Resistance Junction-ambient (Note 1)	$R_{\theta JA}$	125	°C/W
Thermal Resistance Junction-Case (Note 1)	$R_{\theta JC}$	80	°C/W

Note 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
Note 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
Note 3.The power dissipation is limited by 150°C junction temperature
Note 4.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

❖ ELECTRICAL CHARACTERISTICS

(T_J=25 °C, unless otherwise noted)

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=250uA	40	-	-	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C, I_D=1mA	-	0.032	-	V/°C
Static Drain-Source On-Resistance (Note 2)	$R_{DS(ON)}$	V_{GS}=10V , I_D=4A	-	30	37	mΩ
		V_{GS}=4.5V , I_D=3A	-	40	50	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.5	V
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}$		-	-4.5	-	mV/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=32V , V_{GS}=0V , T_J=25°C	-	-	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=55°C	-	-	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	-	-	±100	nA
Forward Transconductance	gfs	V_{DS}=5V , I_D=4A	-	8	-	S
Gate Resistance	R_g	V_{DS}=0V , V_{GS}=0V , f=1MHz	-	2.4	4.8	Ω
Total Gate Charge (4.5V)	Q_g	V_{DS}=15V , V_{GS}=4.5V, I_D=3A	-	5	-	nC
Gate-Source Charge	Q_{gs}		-	1.54	-	
Gate-Drain Charge	Q_{gd}		-	1.84	-	
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=15V , V_{GS}=10V, R_G=3.3Ω, I_D=1A	-	7.8	-	ns
Rise Time	T_r		-	2.1	-	
Turn-Off Delay Time	$T_{d(off)}$		-	29	-	
Fall Time	T_f		-	2.1	-	
Input Capacitance	C_{iss}	V_{DS}=15V , V_{GS}=0V , f=1MHz	-	452	-	pF
Output Capacitance	C_{oss}		-	51	-	
Reverse Transfer Capacitance	C_{rss}		-	38	-	
Diode Characteristics						
Continuous Source Current (Note 1, 4)	I_S	V_G=V_D=0V , Force Current	-	-	4.5	A
Pulsed Source Current (Note 2, 4)	I_{SM}		-	-	14	A
Diode Forward Voltage (Note 2)	V_{SD}	V_{GS}=0V , I_S=1A , T_J=25°C	-	-	1.2	V

Note 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
Note 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
Note 3.The power dissipation is limited by 150°C junction temperature
Note 4.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

❖ TYPICAL CHARACTERISTICS

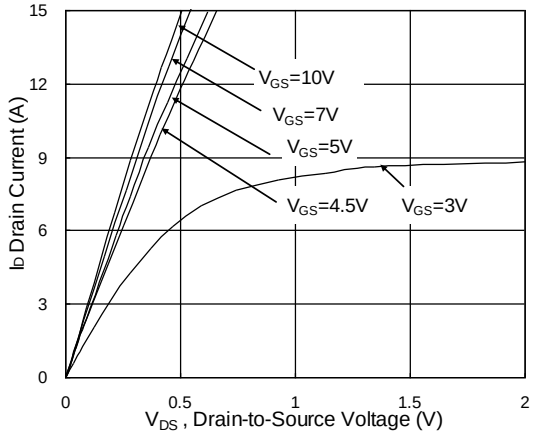


Fig.1 Typical Output Characteristics

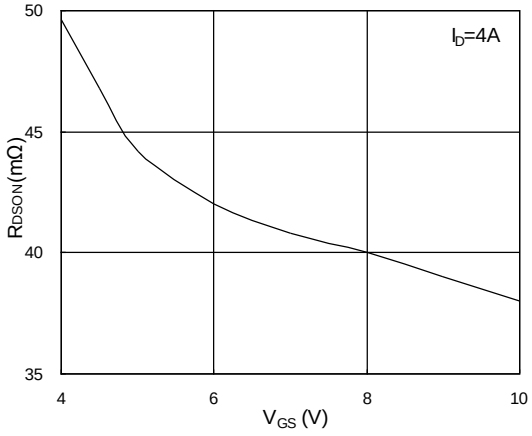


Fig.2 On-Resistance vs. Gate-Source

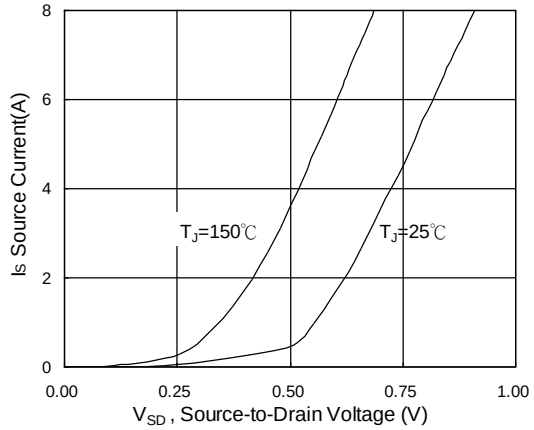


Fig.3 Forward Characteristics of Reverse

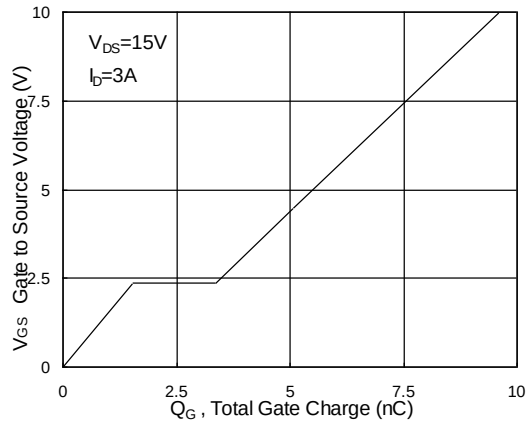


Fig.4 Gate-Charge Characteristics

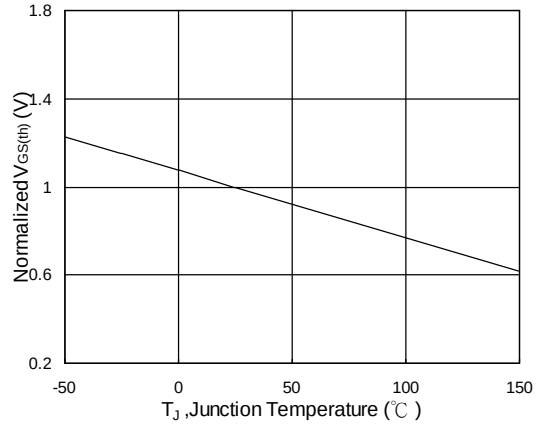


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

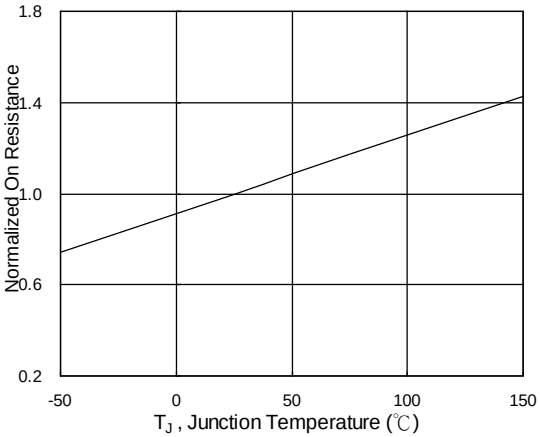


Fig.6 Normalized R_{DSON} vs. T_J

❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

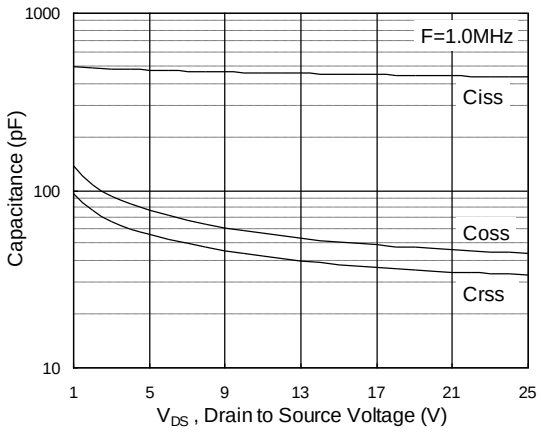


Fig.7 Capacitance

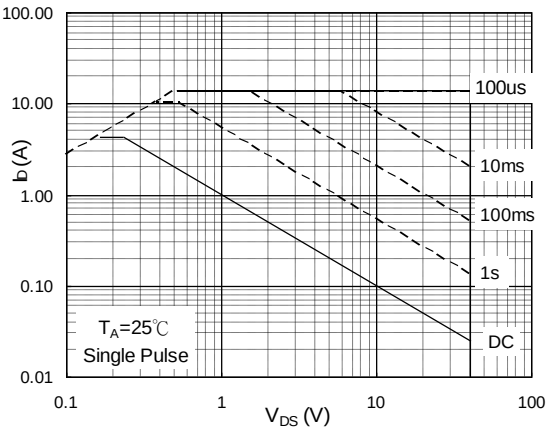


Fig.8 Safe Operating Area

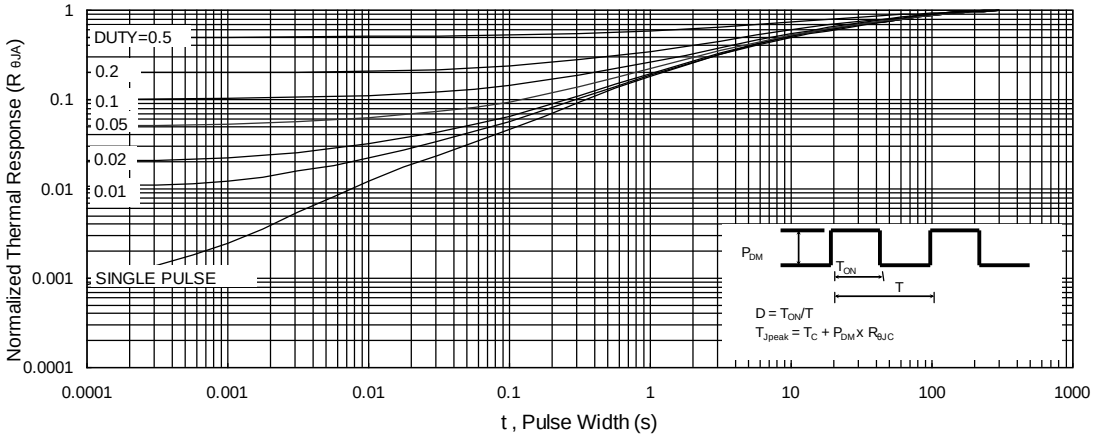


Fig.9 Normalized Maximum Transient Thermal Impedance

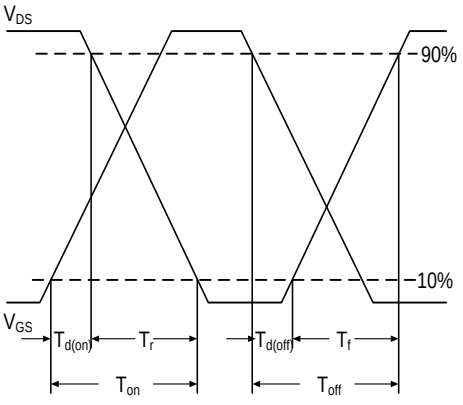


Fig.10 Switching Time Waveform

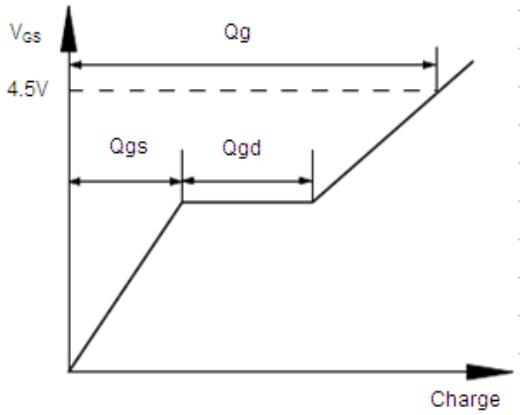


Fig.11 Gate Charge Waveform