Dual N-CH40V Fast Switching MOSFETs

❖ GENERAL DESCRIPTION

The AMS4204 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The AMS4204 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

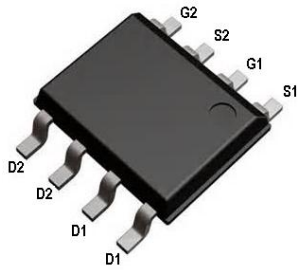
❖ FEATURES

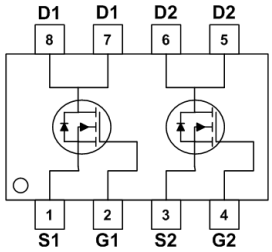
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summery

BVDSS	RDSON	ID
40V	15mΩ	7.5A

SOP8 Pin configuration





❖ ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current, V_{GS} @ -10V (Note 1)	I_D@T_A=25°C	7.5	A
Continuous Drain Current, V_{GS} @ -10V (Note 1)	I_D@T_A=70°C	6	A
Pulsed Drain Current (Note 2)	I_{DM}	30	A
Single Pulse Avalanche Energy (Note 3)	EAS	69	mJ
Avalanche Current	I_{AS}	25	A
Total Power Dissipation (Note 4)	P_D@T_A=25°C	1.5	W
Storage Temperature Range	T_{STG}	-55 to 150	°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Thermal Resistance Junction-Ambient (Steady State) (Note 1)	$R_{\theta JA}$	85	°C/W
Thermal Resistance Junction-Case (Note 1)	$R_{\theta JC}$	36	°C/W

Note 1: The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
Note 2: The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
Note 3: The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-27.2A
Note 4: The power dissipation is limited by 150°C junction temperature
Note 5: The Min. value is 100% EAS tested guarantee.
Note 6: The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

❖ ELECTRICAL CHARACTERISTICS

(T_J=25 °C, unless otherwise noted)

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_D=250uA	40	-	-	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C, I_D=1mA	-	0.034	-	V/°C
Static Drain-Source On-Resistance (Note 2)	$R_{DS(ON)}$	V_{GS}=10V , I_D=6A	-	12	15	mΩ
		V_{GS}=4.5V , I_D=3A	-	16	20	
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.5	V
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}$		-	-5.64	-	mV/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=32V , V_{GS}=0V , T_J=25°C	-	-	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=55°C	-	-	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V , V_{DS}=0V	-	-	±100	nA
Forward Transconductance	gfs	V_{DS}=5V , I_D=6A	-	31	-	S
Gate Resistance	R_g	V_{DS}=0V , V_{GS}=0V , f=1MHz	-	2.1	4.2	Ω
Total Gate Charge (4.5V)	Q_g	V_{DS}=20V , V_{GS}=4.5V, I_D=6A	-	10.7	-	nC
Gate-Source Charge	Q_{gs}		-	3.3	-	
Gate-Drain Charge	Q_{gd}		-	4.2	-	
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=12V , V_{GS}=10V, R_G=3.3Ω I_D=6A	-	8.6	-	ns
Rise Time	T_r		-	3.4	-	
Turn-Off Delay Time	$T_{d(off)}$		-	25	-	
Fall Time	T_f		-	2.2	-	
Input Capacitance	C_{iss}	V_{DS}=15V , V_{GS}=0V, f=1MHz	-	1314	-	pF
Output Capacitance	C_{oss}		-	120	-	
Reverse Transfer Capacitance	C_{rss}		-	88	-	
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy (Note 5)	EAS	V_{DD}=25V , L=0.1mH , I_{AS}=20A	45	-	-	mJ
Diode Characteristics						
Continuous Source Current (Note 1, 6)	I_S	V_G=V_D=0V , Force Current	-	-	7.5	A
Pulsed Source Current (Note 2, 6)	I_{SM}		-	-	30	A
Diode Forward Voltage (Note 2)	V_{SD}	V_{GS}=0V , I_S=1A , T_J=25°C	-	-	1.2	V

Note 1: The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
Note 2: The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
Note 3: The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-27.2A
Note 4: The power dissipation is limited by 150°C junction temperature
Note 5: The Min. value is 100% EAS tested guarantee.
Note 6: The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

❖ TYPICAL CHARACTERISTICS

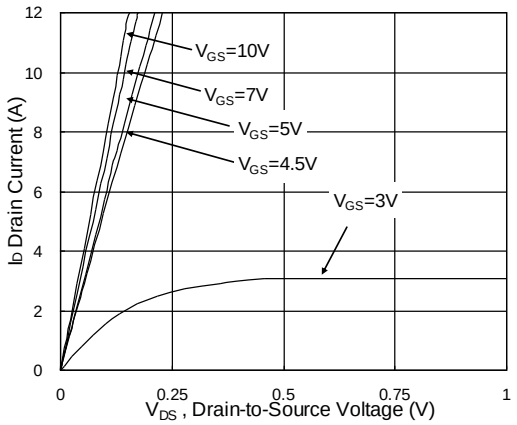


Fig.1 Typical Output Characteristics

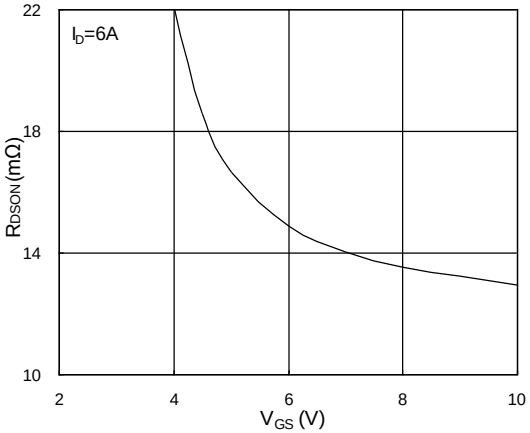


Fig.2 On-Resistance vs. G-S Voltage

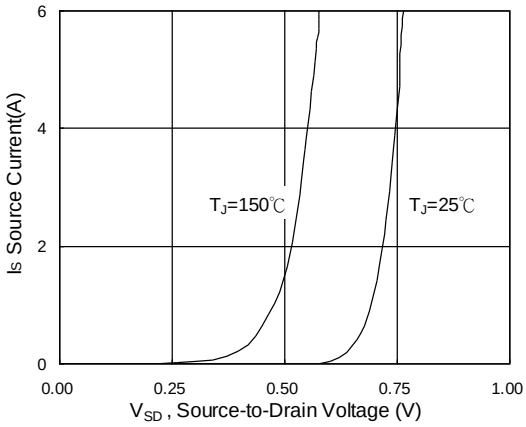


Fig.3 Forward Characteristics of Reverse

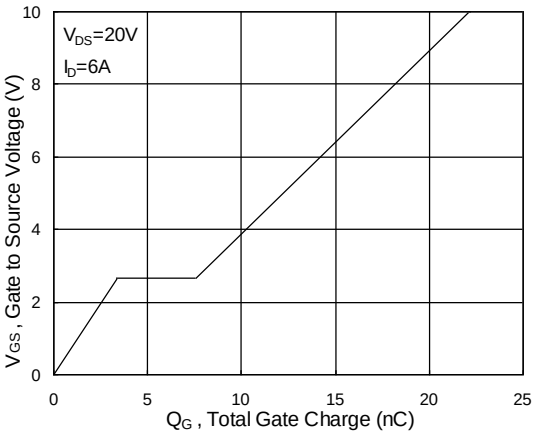


Fig.4 Gate-Charge Characteristics

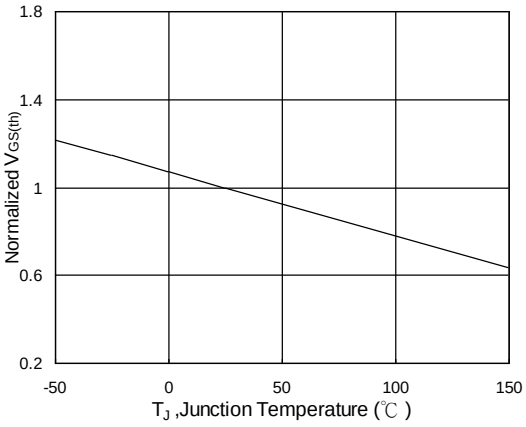


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

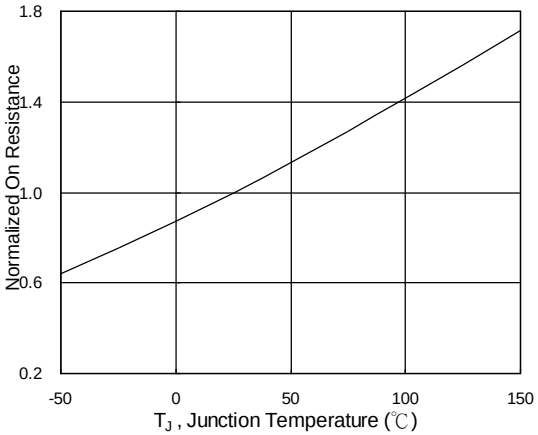


Fig.6 Normalized R_{DSON} vs. T_J

❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

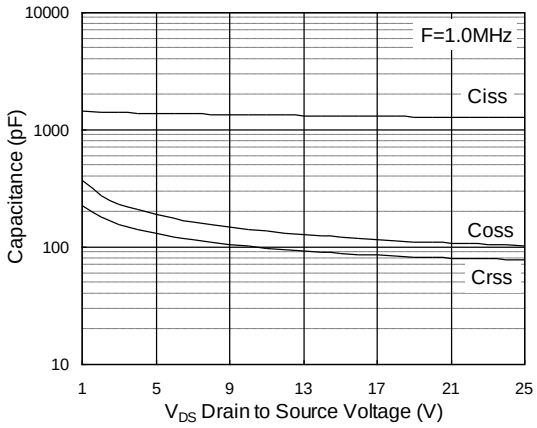


Fig.7 Capacitance

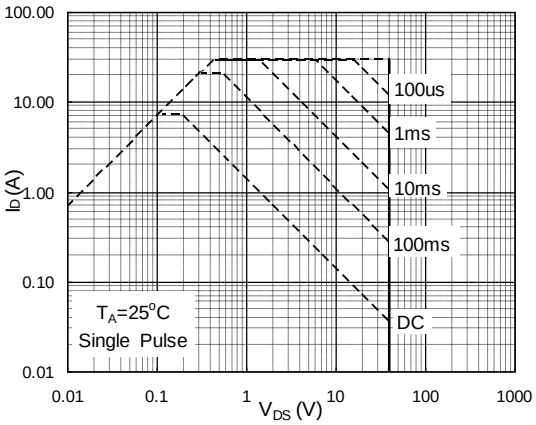


Fig.8 Safe Operating Area

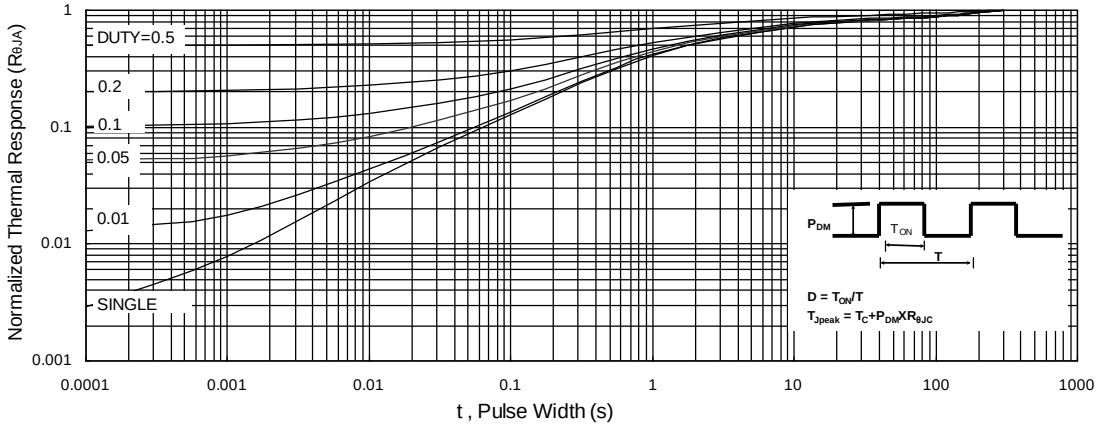


Fig.9 Normalized Maximum Transient Thermal Impedance

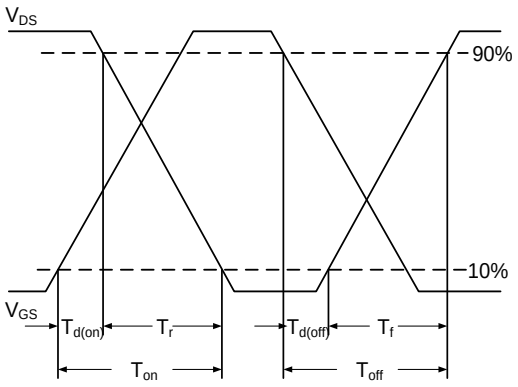


Fig.10 Switching Time Waveform

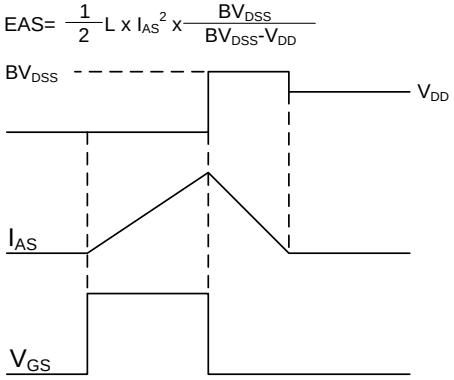


Fig.11 Unclamped Inductive Switching Waveform