

Dual N-CH Fast Switching MOSFETs

❖ GENERAL DESCRIPTION

The AMS4210 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The AMS4210 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

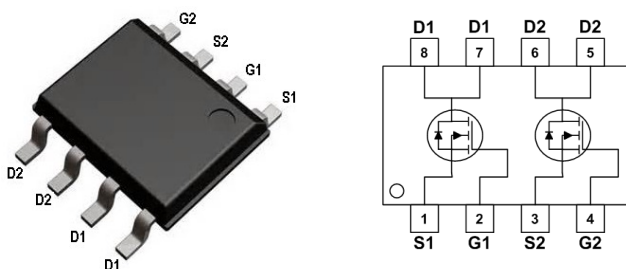
❖ FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
40V	17m Ω	7A
40V	8.5m Ω	10.5A

SOP8 Pin configuration



❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
<p>AMS4210 X X</p> <p>Package Type Packing S: SOP-8L Blank : Bag A : Taping</p>	<p>AM 4 2 1 0 → Part number YY WWX → ID code:internal → WW:01~26 (A~Z) 27~52 (a~z) → Year: 11=2011 12=2012 ⋮ 19=2019</p>

❖ ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating		Units
		Q1	Q2	
Drain-Source Voltage	V_{DS}	40	40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current, V_{GS} @ 10V (Note 1)	$I_D@T_A=25^{\circ}C$	7.5	10.5	A
Continuous Drain Current, V_{GS} @ 10V (Note 1)	$I_D@T_A=70^{\circ}C$	5.7	8.4	A
Pulsed Drain Current (Note 2)	I_{DM}	50	50	A
Single Pulse Avalanche Energy (Note 3)	EAS	55	166	mJ
Avalanche Current	I_{AS}	25	39	A
Total Power Dissipation (Note 4)	$P_D@T_A=25^{\circ}C$	1.5	1.5	W
Storage Temperature Range	T_{STG}	-55 to 150		°C
Operating Junction Temperature Range	T_J	-55 to 150		°C
Thermal Resistance Junction-Ambient (Note 1)	$R_{\theta JA}$	85		°C/W
Thermal Resistance Junction-Case (Note 1)	$R_{\theta JC}$	36		°C/W

Note 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.

Note 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

Note 3.The EAS data shows Max. ratin . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=25A$

Note 4.The power dissipation is limited by 150°C junction temperature

Note 5.The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

❖ ELECTRICAL CHARACTERISTICS

 (T_J=25 °C, unless otherwise noted)

Q1 N-Channel						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V , I _D =250uA	40	-	-	V
BVDSS Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA	-	-	-	V/°C
Static Drain-Source On-Resistance (Note 2)	R _{DS(ON)}	V _{GS} =10V , I _D =10A	-	-	17	mΩ
		V _{GS} =4.5V , I _D =8A	-	-	22	
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250uA	1.0	-	2.5	V
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)}		-	-4.8	-	mV/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =32V , V _{GS} =0V , T _J =25°C	-	-	1	uA
		V _{DS} =32V , V _{GS} =0V , T _J =55°C	-	-	5	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V , V _{DS} =0V	-	-	±100	nA
Forward Transconductance	G _{fs}	V _{DS} =5V , I _D =7A	-	32	-	S
Gate Resistance	R _g	V _{DS} =0V , V _{GS} =0V , f=1MHz	-	2.1	-	Ω
Total Gate Charge (4.5V)	Q _g	V _{DS} =32V , V _{GS} =4.5V , I _D =7A	-	10	-	nC
Gate-Source Charge	Q _{gs}		-	2.6	-	
Gate-Drain Charge	Q _{gd}		-	4.1	-	
Turn-On Delay Time	T _{d(on)}	V _{DD} =20V , V _{GS} =10V , R _G =3.3Ω I _D =7A	-	2.8	-	ns
Rise Time	T _r		-	12.8	-	
Turn-Off Delay Time	T _{d(off)}		-	21.2	-	
Fall Time	T _f		-	6.4	-	
Input Capacitance	C _{iss}	V _{DS} =15V , V _{GS} =0V , f=1MHz	-	1013	-	pF
Output Capacitance	C _{oss}		-	107	-	
Reverse Transfer Capacitance	C _{rss}		-	76	-	
Diode Characteristics						
Continuous Source Current (Note 1,5)	I _S	V _G =V _D =0V , Force Current	-	-	7.2	A
Pulsed Source Current (Note 2,5)	I _{SM}		-	-	50	A
Diode Forward Voltage (Note 2)	V _{SD}	V _{GS} =0V , I _S =1A , T _J =25°C	-	-	1	V

 Note 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.

Note 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

 Note 3.The EAS data shows Max. rati n . The test condition is V_{DD}=25V , V_{GS}=10V , L=0.1mH , I_{AS}=25A

Note 4.The power dissipation is limited by 150°C junction temperature

 Note 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

❖ ELECTRICAL CHARACTERISTICS (COUNTINOUS)

 (T_J=25 °C, unless otherwise noted)

Q2 N-Channel						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V , I _D =250uA	40	-	-	V
BVDSS Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA	-	-	-	V/°C
Static Drain-Source On-Resistance (Note 2)	R _{DS(ON)}	V _{GS} =10V , I _D =10A	-	-	8.5	mΩ
		V _{GS} =4.5V , I _D =8A	-	-	12	
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250uA	1.0	-	2.5	V
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)}		-	-4.96	-	mV/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =32V , V _{GS} =0V , T _J =25°C	-	-	1	uA
		V _{DS} =32V , V _{GS} =0V , T _J =55°C	-	-	5	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V , V _{DS} =0V	-	-	±100	nA
Forward Transconductance	G _{fs}	V _{DS} =5V , I _D =7A	-	40	-	S
Gate Resistance	R _g	V _{DS} =0V , V _{GS} =0V , f=1MHz	-	1.6	-	Ω
Total Gate Charge (4.5V)	Q _g	V _{DS} =32V , V _{GS} =4.5V , I _D =10A	-	18.8	-	nC
Gate-Source Charge	Q _{gs}		-	4.7	-	
Gate-Drain Charge	Q _{gd}		-	8.2	-	
Turn-On Delay Time	T _{d(on)}	V _{DD} =20V , V _{GS} =10V , R _G =3.3Ω I _D =10A	-	14.3	-	ns
Rise Time	T _r		-	2.6	-	
Turn-Off Delay Time	T _{d(off)}		-	77	-	
Fall Time	T _f		-	4.8	-	
Input Capacitance	C _{iss}	V _{DS} =15V , V _{GS} =0V , f=1MHz	-	2332	-	pF
Output Capacitance	C _{oss}		-	193	-	
Reverse Transfer Capacitance	C _{rss}		-	138	-	
Diode Characteristics						
Continuous Source Current (Note 1,5)	I _S	V _G =V _D =0V , Force Current	-	-	10.5	A
Pulsed Source Current (Note 2,5)	I _{SM}		-	-	50	A
Diode Forward Voltage (Note 2)	V _{SD}	V _{GS} =0V , I _S =1A , T _J =25°C	-	-	1	V

 Note 1: The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.

Note 2: The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

 Note 3: The EAS data shows Max. rating . The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=39A

Note 4: The power dissipation is limited by 150°C junction temperature

 Note 5: The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

❖ TYPICAL CHARACTERISTICS

Q1 N-Channel

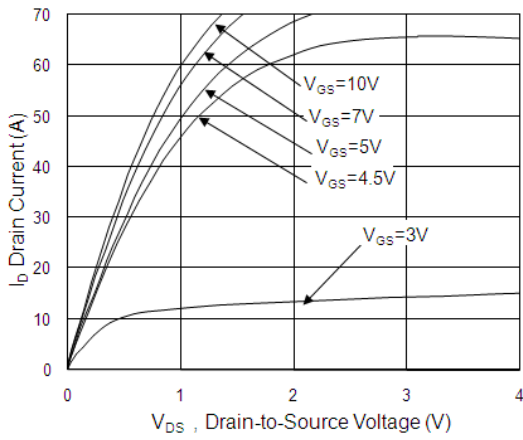


Fig.1 Typical Output Characteristics

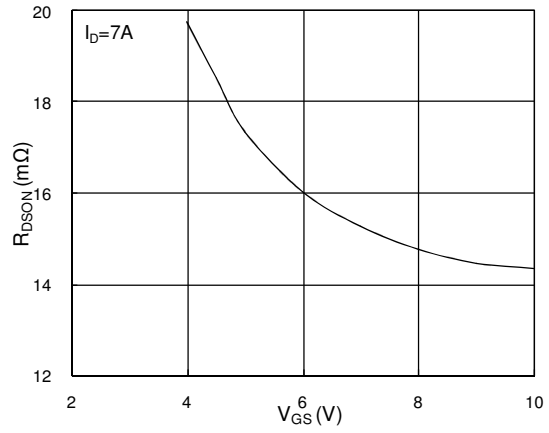


Fig.2 On-Resistance vs. G-S Voltage

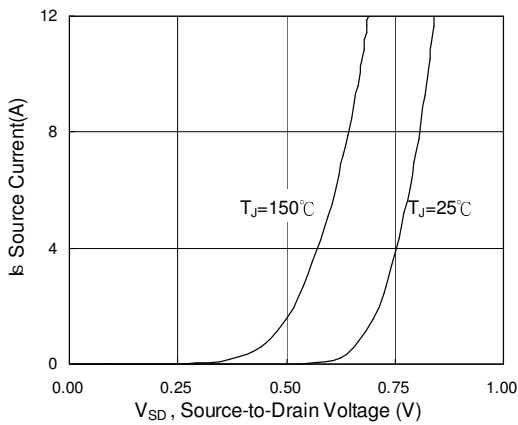


Fig.3 Forward Characteristics Of Reverse

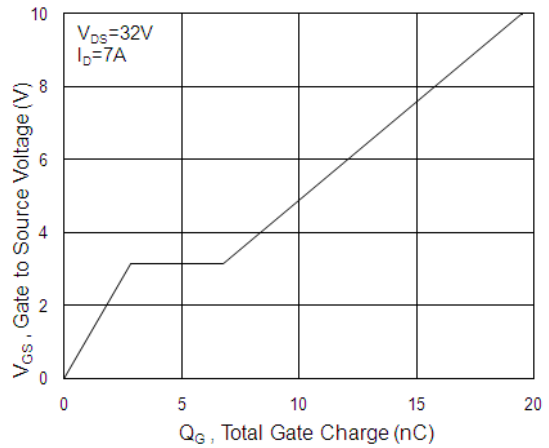


Fig.4 Gate-Charge Characteristics

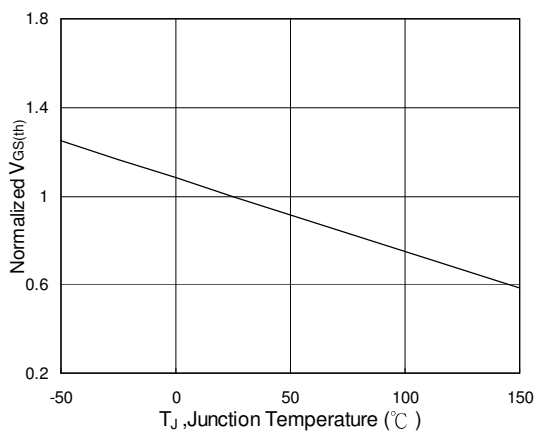


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

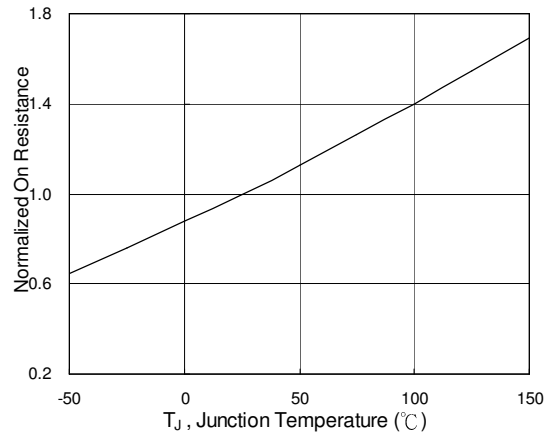


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

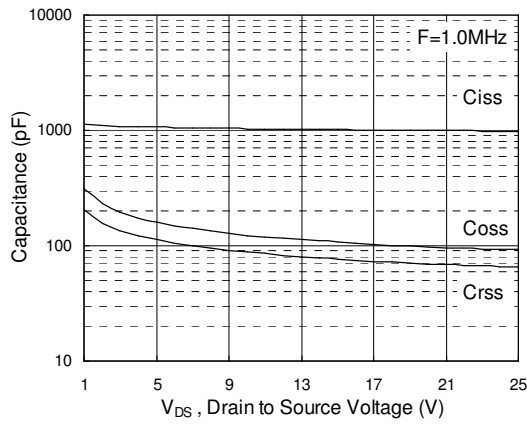


Fig.7 Capacitance

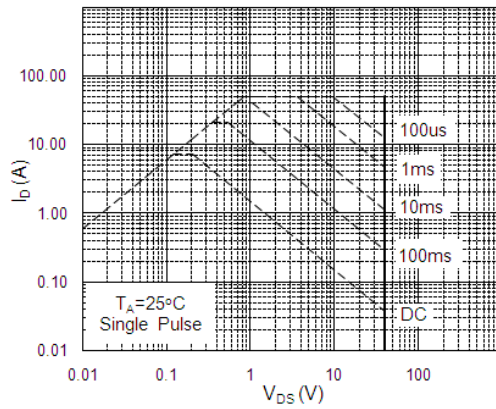


Fig.8 Safe Operating Area

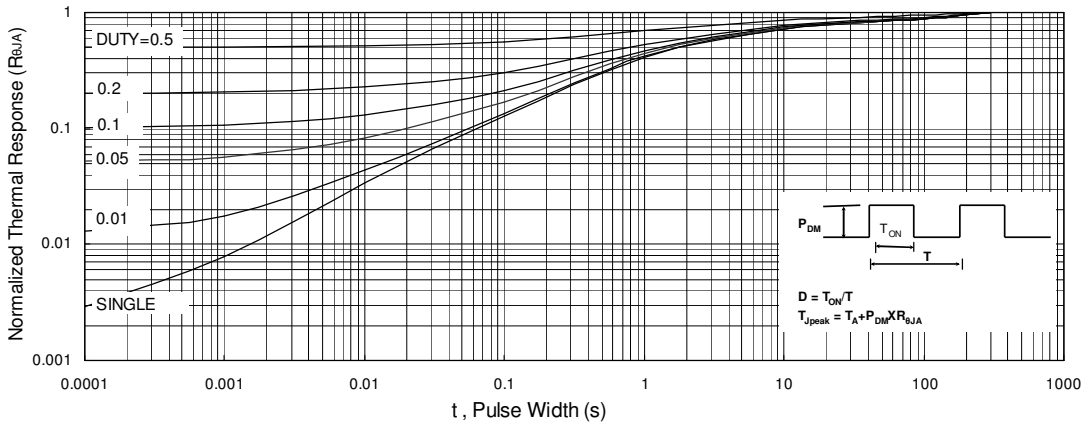


Fig.9 Normalized Maximum Transient Thermal Impedance

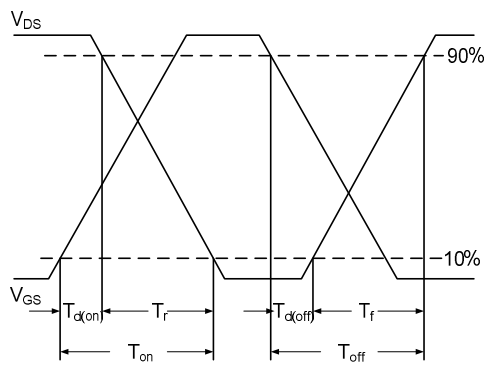


Fig.10 Switching Time Waveform

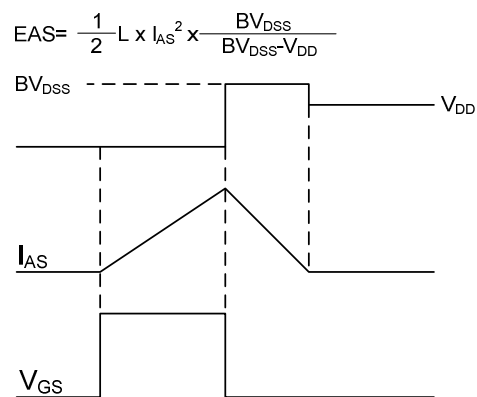


Fig.11 Unclamped Inductive Switching Waveform

❖ **TYPICAL CHARACTERISTICS (COUNTINOUS)**
Q2 N-Channel

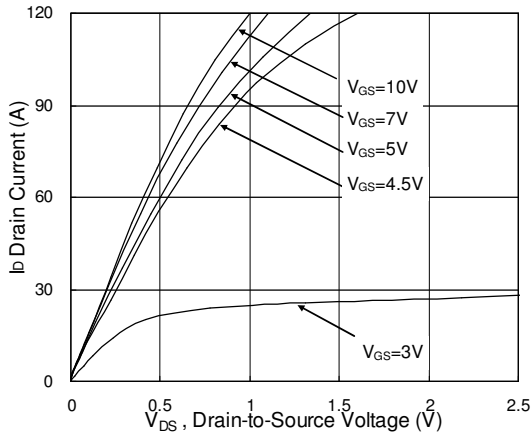


Fig.1 Typical Output Characteristics

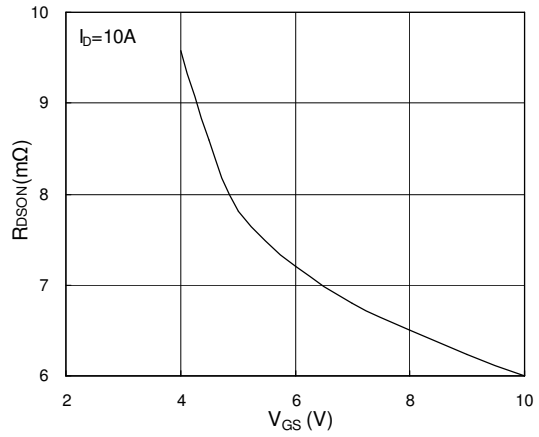


Fig.2 On-Resistance vs. G-S Voltage

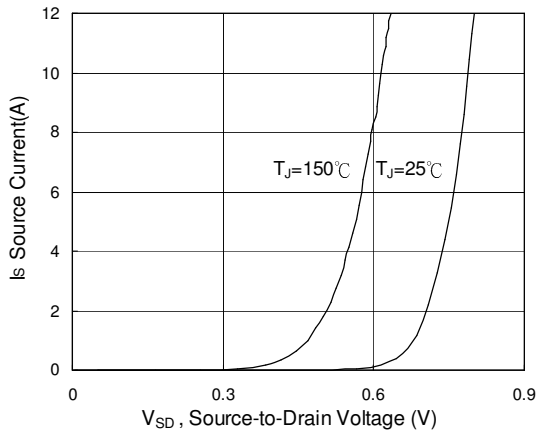


Fig.3 Forward Characteristics Of Reverse

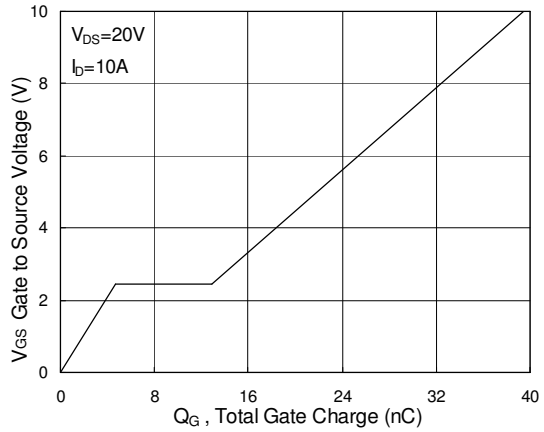


Fig.4 Gate-Charge Characteristics

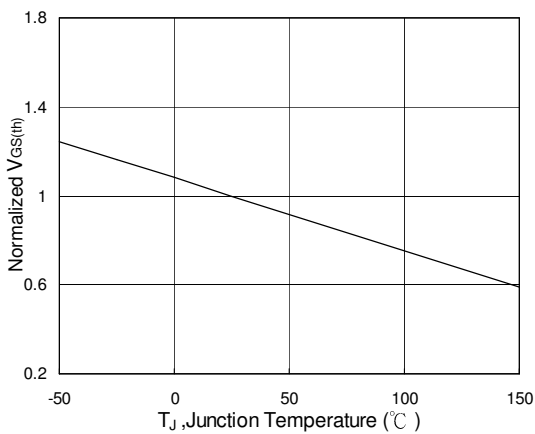


Fig.5 Normalized V_{GS(th)} vs. T_J

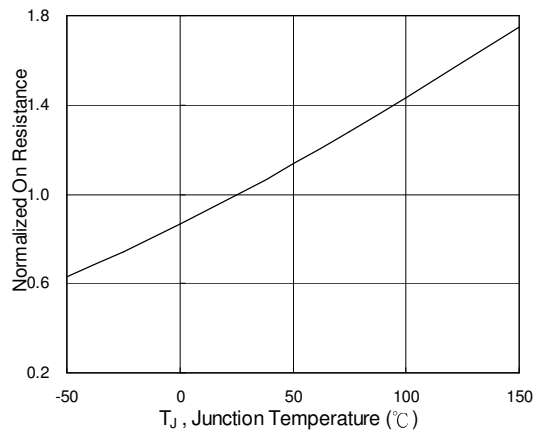


Fig.6 Normalized R_{DS(on)} vs. T_J

❖ TYPICAL CHARACTERISTICS (COUNTINOUS)

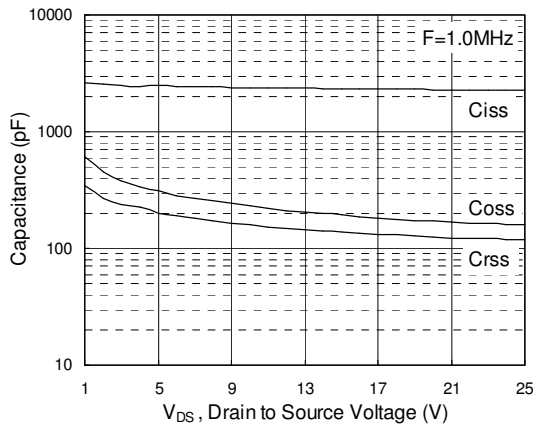


Fig.7 Capacitance

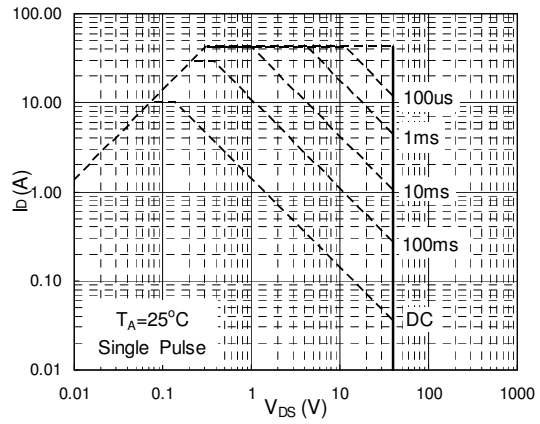


Fig.8 Safe Operating Area

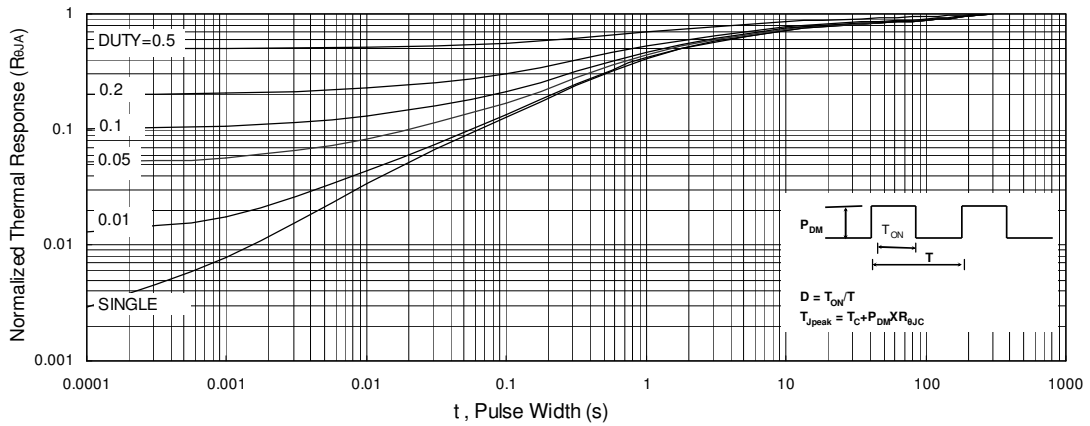


Fig.9 Normalized Maximum Transient Thermal Impedance

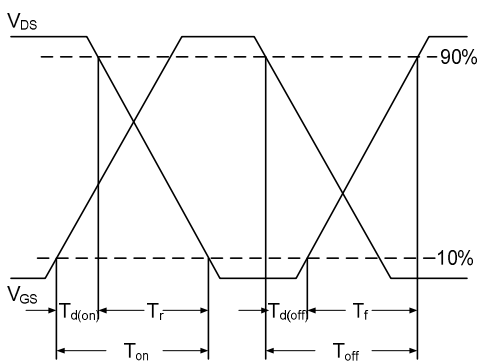


Fig.10 Switching Time Waveform

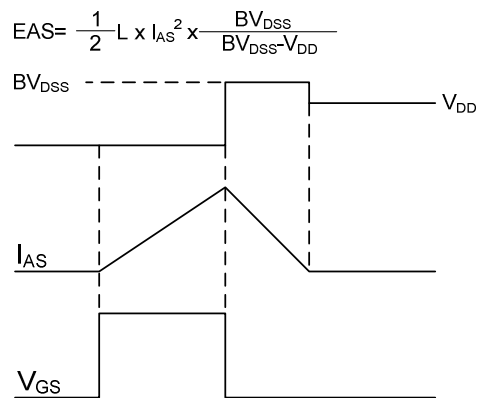


Fig.11 Unclamped Inductive Switching Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$