

3A Sink/Source Bus Termination Regulator

❖ GENERAL DESCRIPTION

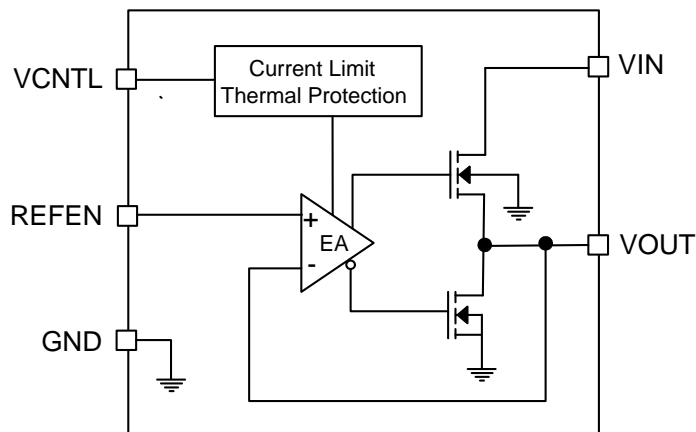
AX1250D5 is a linear regulator designed as a cost-effective solution for active termination of DDR SDRAM. The converting voltage range is from 1.6V to 6V into a desired output voltage, which is adjusted by two external resistors. The current sourcing and sinking capability of the regulator is up to 3A while the output voltage within 3%.

This device provides on-chip thermal shutdown and current limit functions for circuit tolerance of the output fault conditions. TO252-5L package is available for all commercial and industrial surface mount applications.

❖ FEATURES

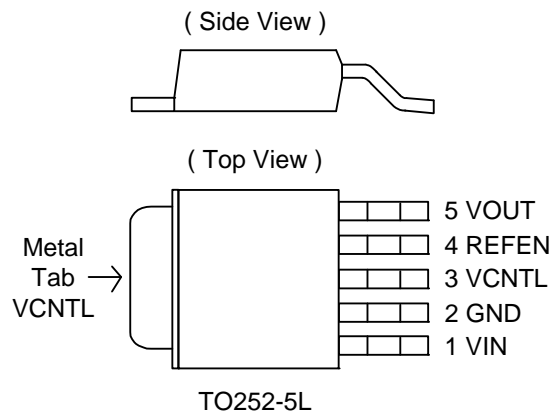
- Ideal for DDR-I and DDR-II applications
- Capable of sourcing and sinking current 3A
- Integrated power MOSFETs
- Current-shoot-through protection
- Current limiting protection
- Thermal shutdown protection
- High accuracy output voltage at full load
- Output adjustment by external resistors
- Minimum external components
- Shutdown for standby or suspend mode operation with high-Impedance output
- TO252-5L Pb-Free Package.

❖ BLOCK DIAGRAM



❖ PIN ASSIGNMENT

The package of AX1250D5 is TO252-5L; the pin assignment is given by:



Name	Description
VIN	IC power supply pin
GND	Ground pin
REFEN	Reference voltage input and chip enable
VOUT	Output Voltage pin
VCNTL	Gate drive voltage

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
<p>AX1250 X X X</p> <p>Package Type D5: TO252-5L</p> <p>Packing Blank: Tube A: Taping</p>	<p>→ Part number</p> <p>1 2 5 0 G H → Package Code</p> <p>Y W W S S S → Date Code Y: Last Digit of the year WW: Week SSS: Sequence</p>

❖ ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Characteristics	Symbol	Rating	Unit
VIN Supply Voltage	V _{IN}	6	V
Control Voltage	V _{CNTL}	6	V
Power Dissipation	PD	Internally Limited	W
Storage Temperature Range	T _{ST}	-55 to +150	°C
Operating Ambient Temperature	T _A	-40 to +85	°C
Operating Junction Temperature	T _J	-40 to +125	°C
Thermal Resistance from Junction to case	θ _{JC}	10	°C/W
Thermal Resistance from Junction to ambient	θ _{JA}	45	°C/W

Note: θ_{JA} is measured with the PCB copper area (need connect to all VCNTL pins) of approximately 1.5 in² (Multi-layer).

❖ ELECTRICAL CHARACTERISTICS

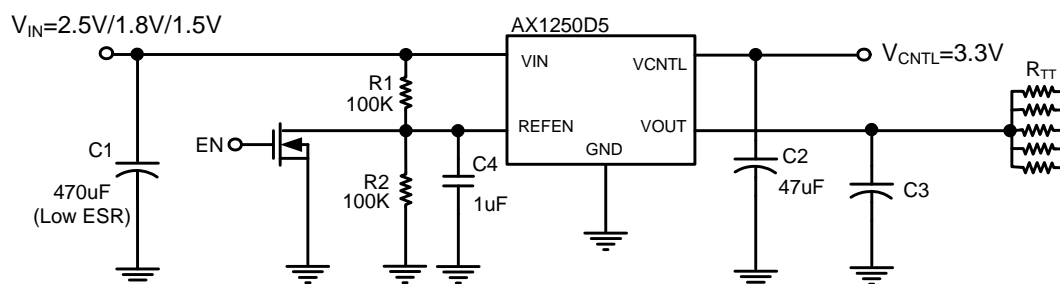
* $V_{IN}=2.5V$, $V_{CNTL}=3.3V$, $V_{REFEN}=1.25V$, $C_{OUT}=10\mu F$ (Ceramic), $T_A=25^\circ C$, unless otherwise specified

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range (DDR I/II)	V_{IN}	$V_{CNTL} \geq V_{IN}$ (Note1)	1.6	1.5/1.8	-	V
Gate Drive Voltage Range	V_{CNTL}	$V_{CNTL} \geq V_{IN}$ (Note1)	-	3.3	6	V
Quiescent Current	I_{CNTL}	$I_{OUT}=0A$	-	1	3	mA
Standby Current	I_{STBY}	$V_{REFEN} < 0.2V$ (Shutdown) $R_{LOAD} = 180\Omega$	-	10	90	μA
Output Offset Voltage	V_{OS}	$I_{OUT}=0A$ (Note2)	-20	-5	+20	mV
Load Regulation	ΔV_{Load}	$I_{OUT}=+1.5A$	-	+0.5	+2	%
		$I_{OUT}=-1.5A$	-	-0.5	-2	
Shutdown Threshold	V_{IH}	Enable	0.8	-	-	V
	V_{IL}	Shutdown	-	-	0.2	V
Current Limit	CL		-	3	-	A
Thermal Shutdown	T_{SD}	$3.3V \leq V_{CNTL} \leq 5V$	-	140	-	$^\circ C$

Note 1: Keep $V_{CNTL} \geq V_{IN}$ at power on/off sequences.

Note 2: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN} .

❖ APPLICATION CIRCUIT



$$R_{TT}=50\Omega/33\Omega/25\Omega$$

$C3=10\mu F$ (Ceramic) + 1000 μF under the worst case testing condition

❖ APPLICATION INFORMATION

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AX1250D5. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AX1250D5 and the preceding power converter.

Thermal Considerations

The AX1250D5 series can deliver a current of up to 3A over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$PD (MAX) = (T_{J (MAX)} - T_A) / \theta_{JA}$$

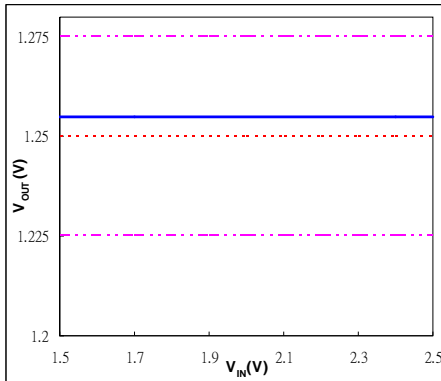
Where $T_{J (MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) for TO252-5L package at recommended minimum footprint is 45°C/W on 1.5 in² and Multi-layer PCB layout. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula:

$$PD (MAX) = (125^\circ\text{C} - 25^\circ\text{C}) / 45^\circ\text{C} / \text{W} = 2.22\text{W}$$

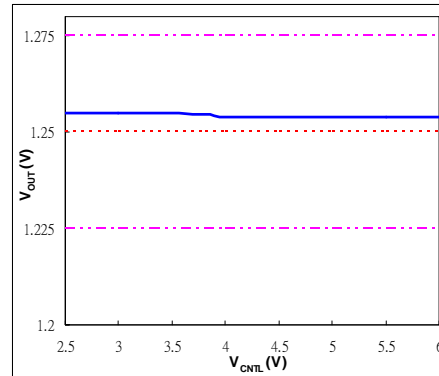
The thermal resistance θ_{JA} of TO252-5L is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding wide copper to tap (VCNTL) pin. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

❖ TYPICAL CHARACTERISTICS

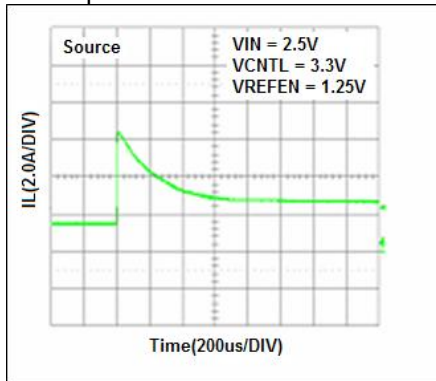
Line Regulation(VIN vs. VOUT)



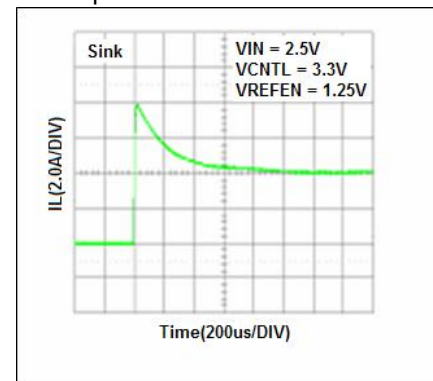
Line Regulation(VCNTL vs. VOUT)



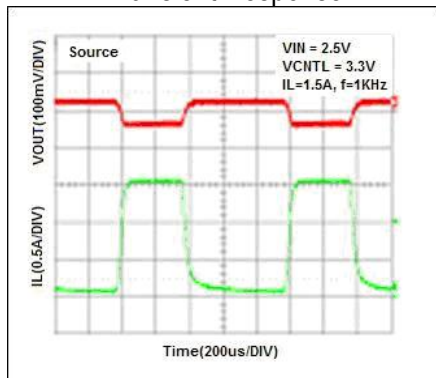
Output Short-Circuit Protection



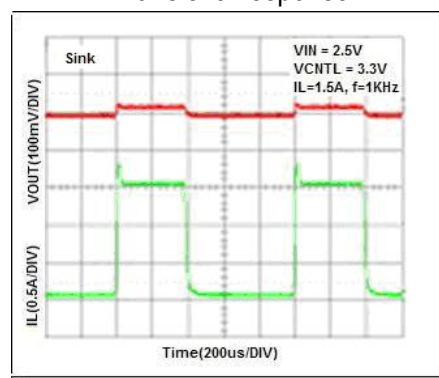
Output Short-Circuit Protection



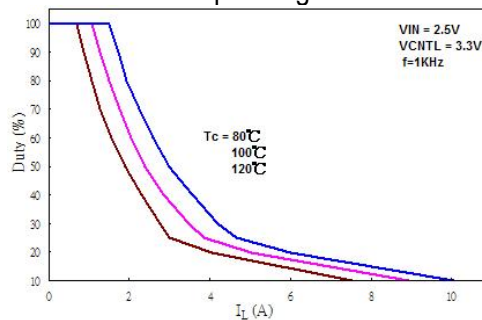
Transient Response



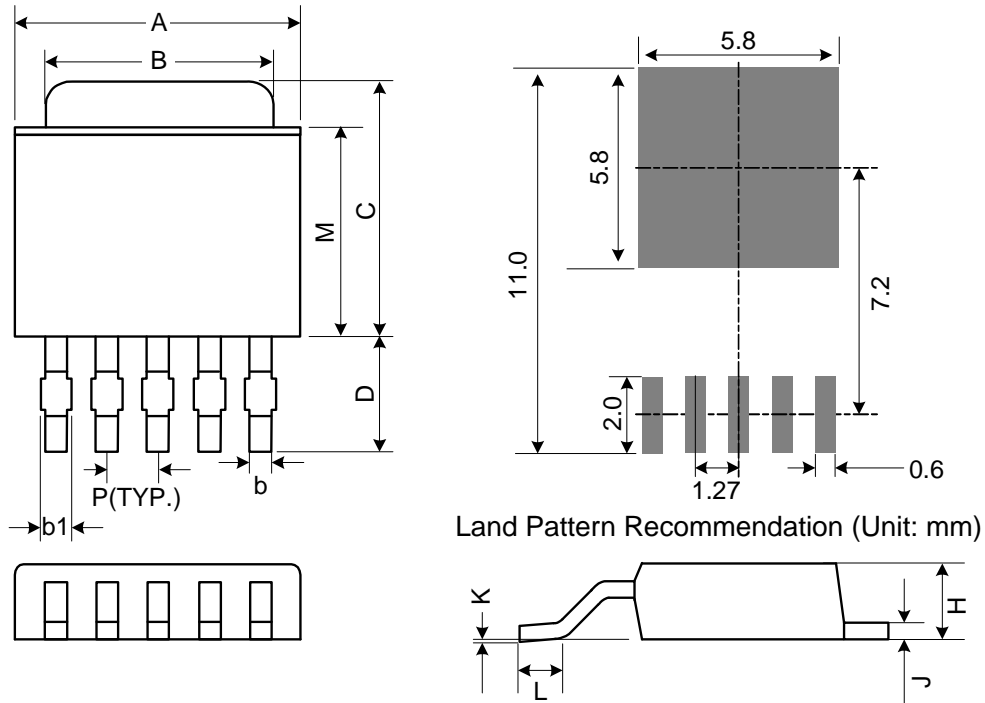
Transient Response



Safe Operating Area



❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	6.35	6.60	6.85	0.250	0.260	0.270
B	5.20	5.35	5.50	0.205	0.211	0.217
C	6.80	7.00	7.30	0.268	0.276	0.287
D	2.20	2.50	2.80	0.087	0.098	0.110
P	1.27 REF.			0.050 REF.		
H	2.20	2.30	2.40	0.087	0.091	0.094
J	0.45	0.52	0.58	0.018	0.020	0.023
K	0.00	0.08	0.15	0.000	0.003	0.006
L	0.90	1.20	1.63	0.035	0.047	0.064
M	5.40	5.80	6.20	0.213	0.228	0.244
b	0.50	0.65	0.80	0.020	0.026	0.031
b1	0.40	0.50	0.63	0.016	0.020	0.025