1.5A Sink/Source Bus Termination Regulator

❖ GENERAL DESCRIPTION

AX1250GM is a linear regulator designed as a cost-effective solution for active termination of DDR SDRAM. The converting voltage range is from 1.6V to 6V into a desired output voltage, which is adjusted by two external resistors. The current sourcing and sinking capability of the regulator is up to 1.5A while the output voltage within 2%.

This device provides on-chip thermal shutdown and current limit functions for circuit tolerance of the output fault conditions. SOP-8L package is available for all commercial and industrial surface mount applications.
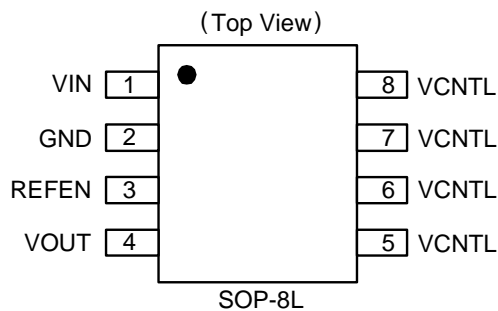
❖ FEATURES

- Ideal for DDR-I and DDR-II applications
- Capable of sourcing and sinking current 1.5A
- Integrated power MOSFETs
- Current-shoot-through protection
- Current limiting protection
- Thermal shutdown protection
- High accuracy output voltage at full load
- Output adjustment by external resistors
- Minimum external components
- Shutdown for standby or suspend mode operation with high-Impedance output
- SOP-8L Pb-Free Package.

❖ Block Diagram
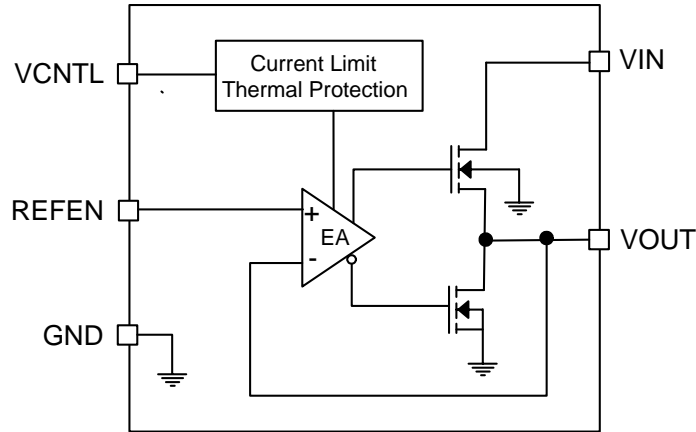
❖ PIN ASSIGNMENT

The package of AX1250GM is SOP-8L; the pin assignment is given by:

（Top View）

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VIN   [ 1            8 ]  VCNTL
GND   [ 2            7 ]  VCNTL
REFEN [ 3            6 ]  VCNTL
VOUT  [ 4            5 ]  VCNTL
```

SOP-8L

Name	Description
VIN	IC power supply pin
GND	Ground pin
REFEN	Reference voltage input and chip enable
VOUT	Output Voltage pin
VCNTL	Gate drive voltage

❖ ORDER INFORMATION

Order Information	Top Marking
AX1250GM X X Package Type S : SOP-8L Packing Blank : Tube A : Taping	1250GMP → Part number / Package Code YWWSSS → Date Code Y : Last Digit of the year WW: Week SSS: Sequence

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❖ Absolute Maximum Ratings (Ta=25)

Characteristics	Symbol	Rating	Unit
VIN Supply Voltage	V_{IN}	6	V
Control Voltage	V_{CNTL}	6	V
Power Dissipation	PD	Internally Limited	W
Storage Temperature Range	T_{ST}	-55 to +150	
Operating Ambient Temperature	T_A	-40 to +85	
Operating Junction Temperature	T_J	-40 to +125	
Thermal Resistance from Junction to case	θ_{JC}	20	/W
Thermal Resistance from Junction to ambient	θ_{JA}	60	/W

Note: θ_{JA} is measured with the PCB copper area (need connect to all VCNTL pins) of approximately 1.5 in^2 (Multi-layer).

## ❖ Electrical Characteristics

*V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REFEN}=1.25V, C_{OUT}=10μF (Ceramic), T_A=25ºC, unless otherwise specified

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range (DDR I/II)	V_{IN}	V_{CNTL} >= V_{IN} (Note1)	1.6	1.5/1.8	-	V
Gate Drive Voltage Range	V_{CNTL}	V_{CNTL} >= V_{IN} (Note1)	-	3.3	6	V
Quiescent Current	I_{CNTL}	I_{OUT}=0A	-	1	3	mA
Standby Current	I_{STBY}	V_{REFEN} < 0.2V (Shutdown) R_{LOAD} = 180Ω	-	10	90	uA
Output Offset Voltage	V_{OS}	I_{OUT}=0A (Note2)	-20	-5	+20	mV
Load Regulation	V_{Load}	I_{OUT}=+1.5A	-	+0.5	+2	%
		I_{OUT}=-1.5A	-	-0.5	-2	
Shutdown Threshold	V_{IH}	Enable	0.8	-	-	V
	V_{IL}	Shutdown	-	-	0.2	V
Current Limit	CL		-	2	-	A
Thermal Shutdown	TSD	3.3V ≤ V_{CNTL} ≤ 5V	-	140	-	

Note 1: Keep V_{CNTL} >= V_{IN} at power on/off sequences.
Note 2: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

❖ Application Circuit
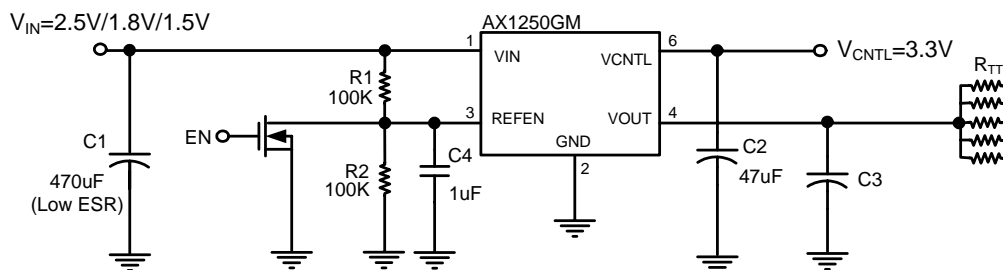
R_{TT}=50 /33 /25

C3=10uF(Ceramic) + 1000uF under the worst case testing condition

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❖ Application Information

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AX1250GM. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AX1250GM and the preceding power converter.

Thermal Considerations

The AX1250GM series can deliver a current of up to 1.5A over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

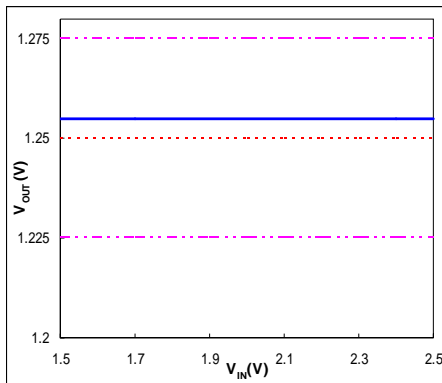$$PD\ (MAX) = (T_{J\ (MAX)} - T_A) / \theta_{JA}$$

Where $T_{J\ (MAX)}$ is the maximum junction temperature of the die (125° C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) for SOP-8L package at recommended minimum footprint is 60°C/W on 1.5 in^2 and Multi-layer PCB layout. The maximum power dissipation at T_A = 25 can be calculated by following formula:
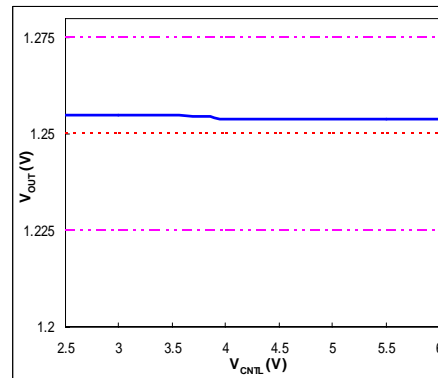
$$PD\ (MAX) = (125 - 25) / 60 /W = 1.67W$$

The thermal resistance θ_{JA} of SOP-8L is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding wide copper to VCNTL pins. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

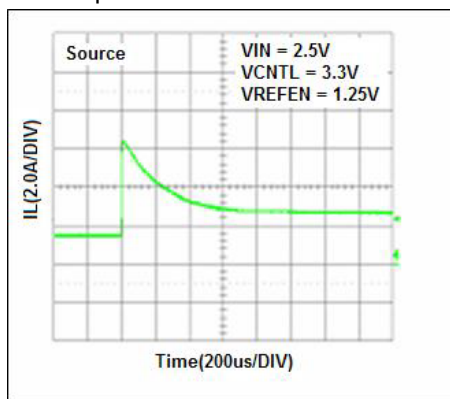**AXElite** 亞瑟萊特科技股份有限公司 AXElite Technology Co., Ltd.
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❖ **Typical Characteristics**

Line Regulation(VIN vs. VOUT)

Line Regulation(VCNTL vs. VOUT)

Output Short-Circuit Protection
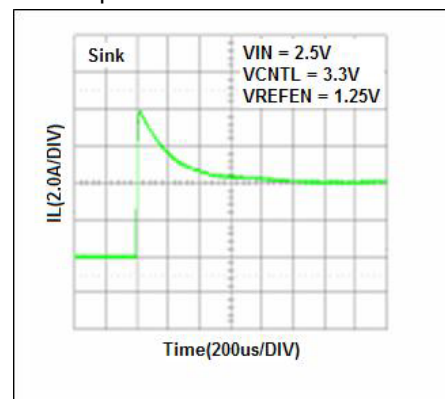
Source
VIN = 2.5V
VCNTL = 3.3V
VREFEN = 1.25V
IL(2.0A/DIV)
Time(200us/DIV)

Output Short-Circuit Protection

Sink
VIN = 2.5V
VCNTL = 3.3V
VREFEN = 1.25V
IL(2.0A/DIV)
Time(200us/DIV)

Transient Response

Source
VIN = 2.5V
VCNTL = 3.3V
IL=1.5A, f=1KHz
VOUT(100mV/DIV)
IL(0.5A/DIV)
Time(200us/DIV)

Transient Response

Sink
VIN = 2.5V
VCNTL = 3.3V
IL=1.5A, f=1KHz
VOUT(100mV/DIV)
IL(0.5A/DIV)
Time(200us/DIV)

Safe Operating Area

VIN = 2.5V
VCNTL = 3.3V
f=1KHz
Tc = 80℃
100℃
120℃

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❖ Package Outlines

DETAIL A

7°(4X)

DETAIL A
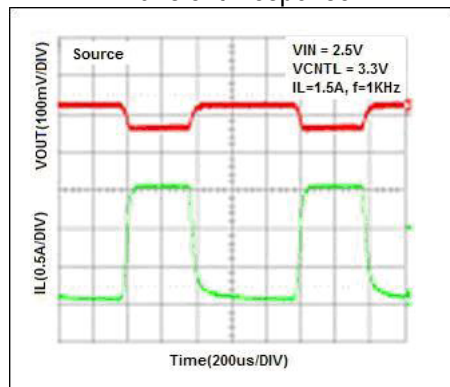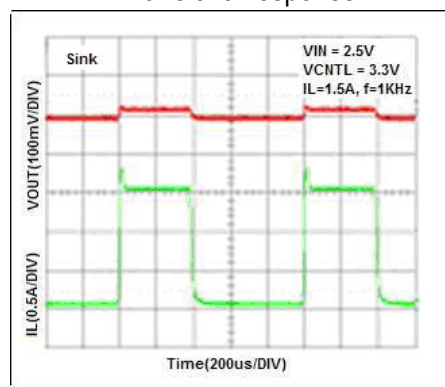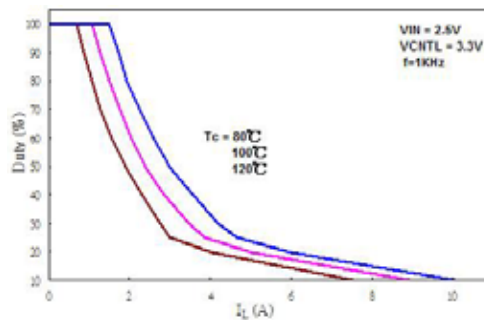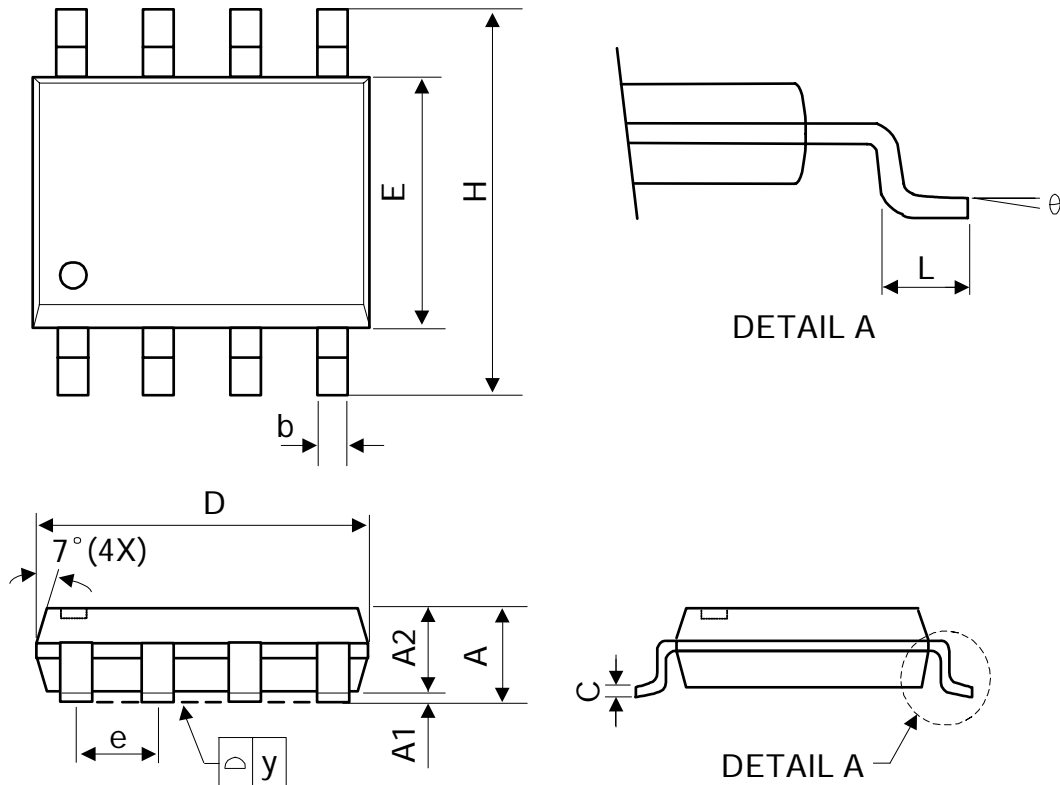
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
b	0.33	0.41	0.51	0.013	0.016	0.020
e	1.27 TYP			0.050 TYP		
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°