1A Sink/Source Bus Termination Regulator

❖ GENERAL DESCRIPTION

The AX1251 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 1A while regulating an output voltage to within 20mV. The output termination voltage cab be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The AX1251 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

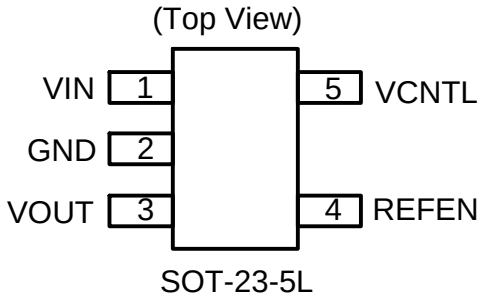
The AX1251 is available in the SOT-23-5L surface mount package.

❖ FEATURES

- Ideal for DDR-I, DDR-II and DDR-III VTT Applications
- Sink and Source 1A Continuous Current
- Integrated Power Driver
- Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting and Thermal Shutdown Protections
- SOT-23-5L Pb-Free Package.

❖ PIN ASSIGNMENT

The package of AX1251 is SOT-23-5L; the pin assignment is given by:



Name	Description
VIN	IC power supply pin
GND	Ground pin
REFEN	Reference voltage input and chip enable
VCNTL	Gate drive voltage
VOUT	Output Voltage pin

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AX1251 X X Package Type B: STO-23-5L Packing Blank: Tube A : Taping	DaYWX → ID code: internal WW: 01~26(A~Z) 27~52(a~z) Year: A=2010 1=2011 AX1251

❖ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Characteristics	Symbol	Rating	Unit
Input Voltage	V_{IN}	2.5 to 1.5 ±3%	V
Control Voltage	V_{CNTL}	6.5 to 3.3 ±5%	V
VIN Supply Voltage	V_{IN}	7	V
Control Voltage	V_{CNTL}	7	V
Power Dissipation	PD	Internally Limited	W
Ambient Temperature	T_A	-40 to +85	°C
Junction Temperature	T_J	-40 to +125	°C
Storage Temperature Range	T_{ST}	-65 to +150	°C
Thermal Resistance from Junction to case	θ_{JC}	180	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	250	°C/W

Note: θ_{JA} is measured with the PCB copper area of approximately 1.5 in^2 (Multi-layer).

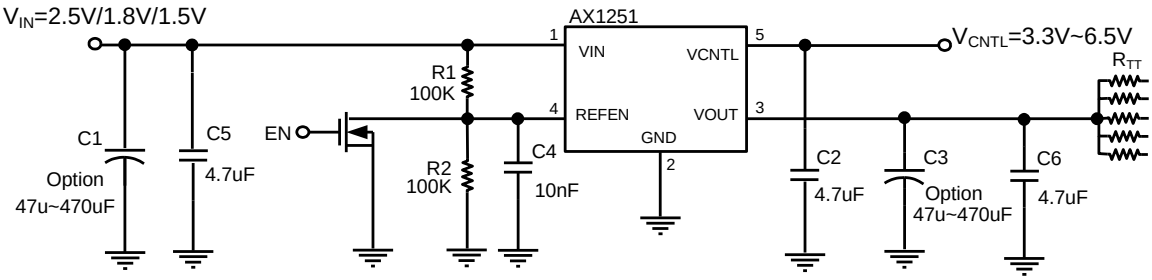
❖ ELECTRICAL CHARACTERISTICS

*V_{IN}=2.5V/1.8V/1.5V, V_{CNTL}=3.3V, V_{REFEN}=1.25V/0.9V/0.75V, C_{OUT}=4.7µF (Ceramic), T_A=25ºC, unless otherwise specified

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
V_{CNTL} Operating Current	I_{CNTL}	I_{OUT}=0A	-	1	2.5	mA
Standby Current	I_{STBY}	V_{REFEN} < 0.2V (Shutdown) R_{LOAD} = 180Ω	-	150	200	uA
Output Offset Voltage **(Note1)**	V_{OS}	I_{OUT}=0A	-10	-	+10	mV
Load Regulation **(Note2)**	Δ V_{OUT}	I_{OUT}=+0.75A	-20	-	+20	mV
		I_{OUT}=-0.75A				
Shutdown Threshold	V_{REF-H}	Enable	0.6	-	-	V
	V_{REF-L}	Shutdown	-	-	0.2	V
Current Limit	CL		1.1	-	-	A
Thermal Shutdown	T_{SD}		-	140	-	°C
Thermal Shutdown Hysteresis	T_{SH}		-	20	-	°C

Note 1: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.
Note 2: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 0.75A.

❖ APPLICATION CIRCUIT



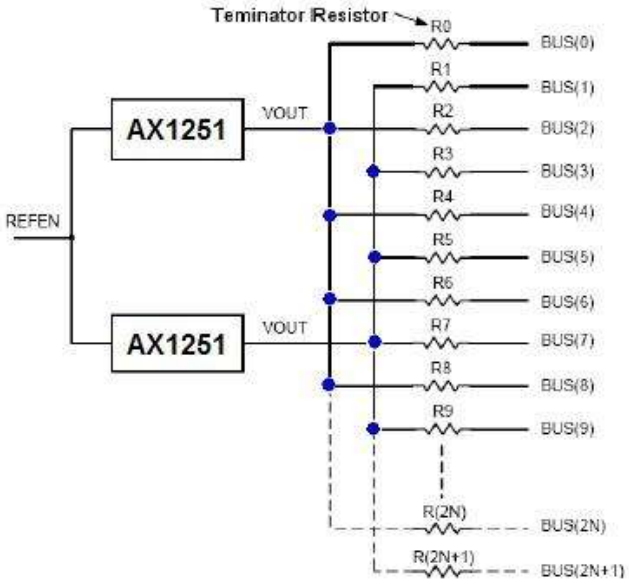
R_{TT}=50Ω/33Ω/25Ω

$$V_{OUT} = V_{REFEN} = V_{IN} \times \left(\frac{R2}{R1+R2}\right)$$

❖ APPLICATION INFORMATION

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the low pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Capacitor Selection

Normally, use a 4.7μF Multi-layer chip capacitor (MLCC) on the input and output capacitors are sufficient. A lower ESR (X5R, X7R) is recommended for input and output capacitors. Add a larger than 47uF in input and output capacitors to provide better output-noise and transient response. A higher- value output capacitor may be necessary if large, fast transients are anticipated and the device is located several inches from the power source.

Thermal Considerations

The AX1251 series can deliver a current of up to 1A over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

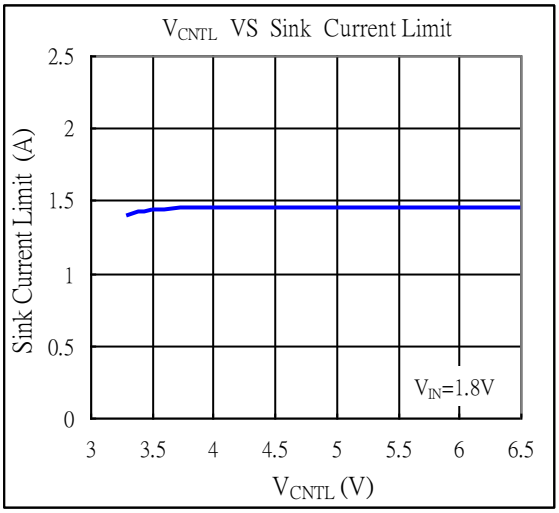
$$PD\ (MAX) = (T_{J\ (MAX)} - T_A) / \theta_{JA}$$

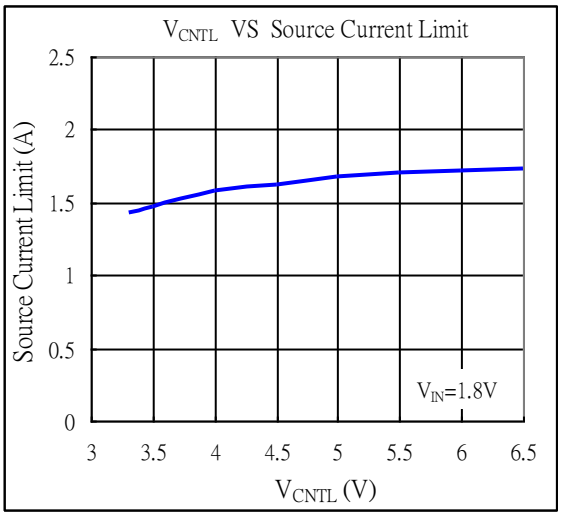
Where $T_{J\ (MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) for SOT-23-5L package at recommended minimum footprint is 250°C/W on 1.5 in^2 and Multi-layer PCB layout. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

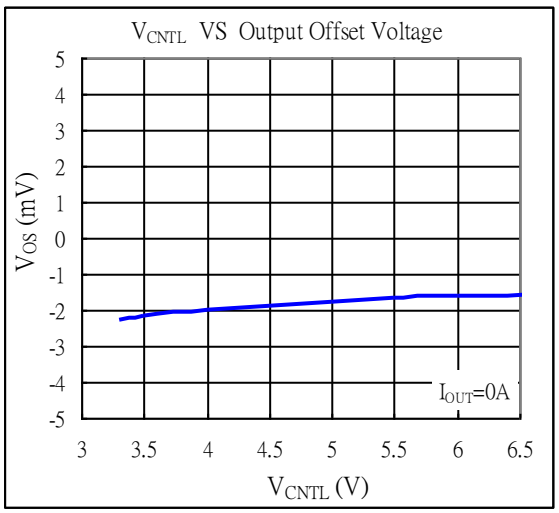
$$PD\ (MAX) = (125°C - 25°C) / 250°C/W = 0.4W$$

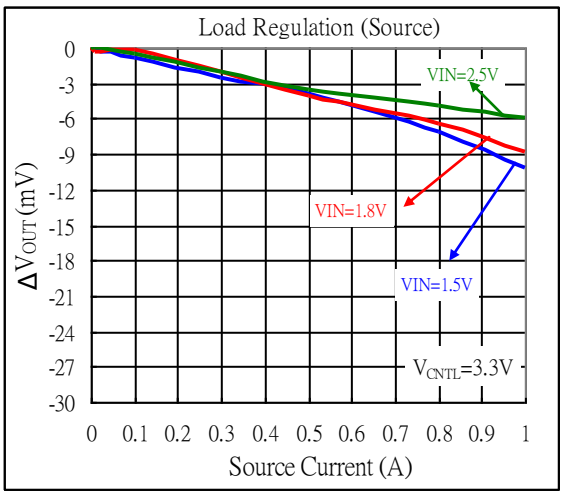
The thermal resistance θ_{JA} of SOT-23-5L is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper to ground pin. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

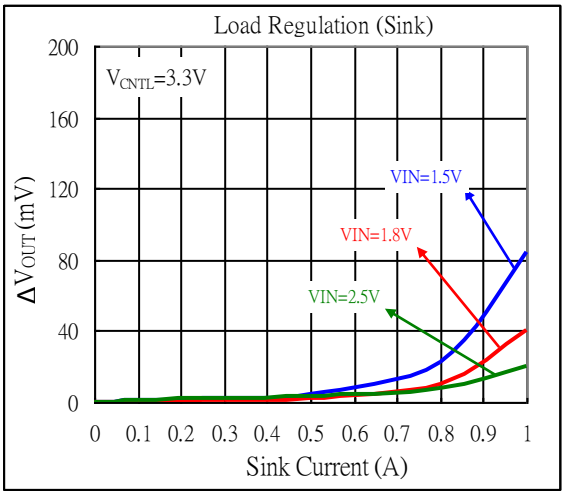
❖ TYPICAL CHARACTERISTICS

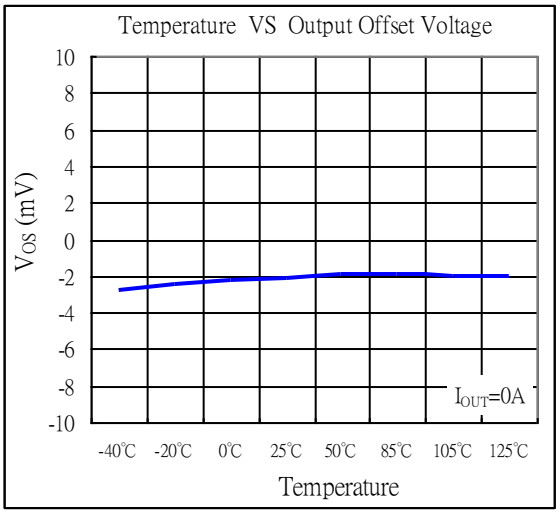






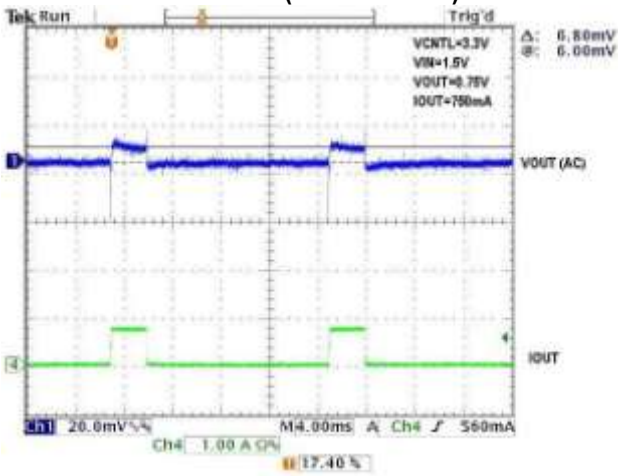




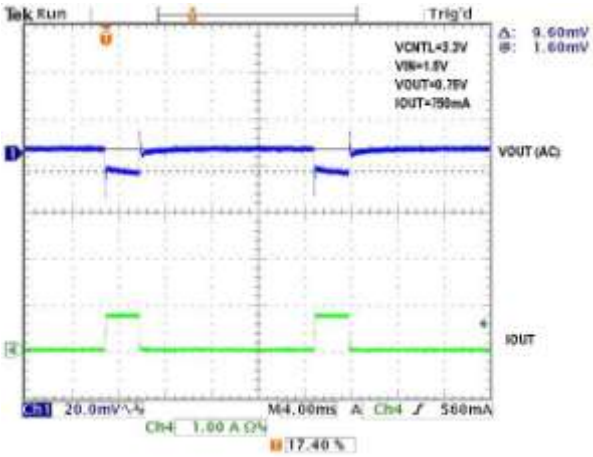


❖ TYPICAL CHARACTERISTICS (CONTINUOUS)

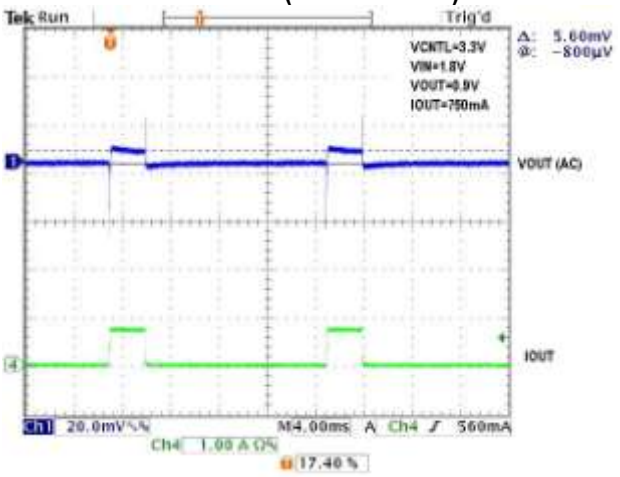
Transient (Sink Current)



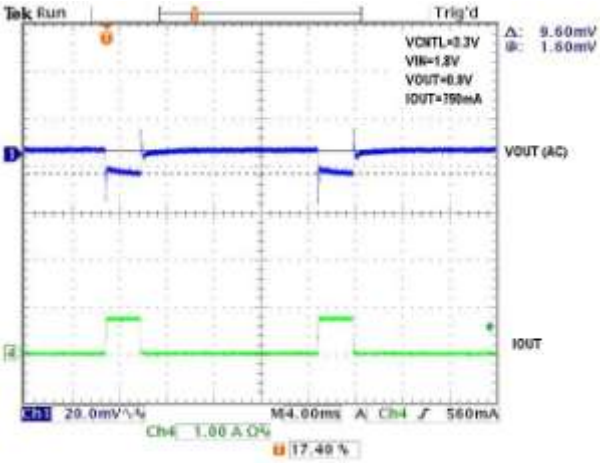
Transient (Source Current)



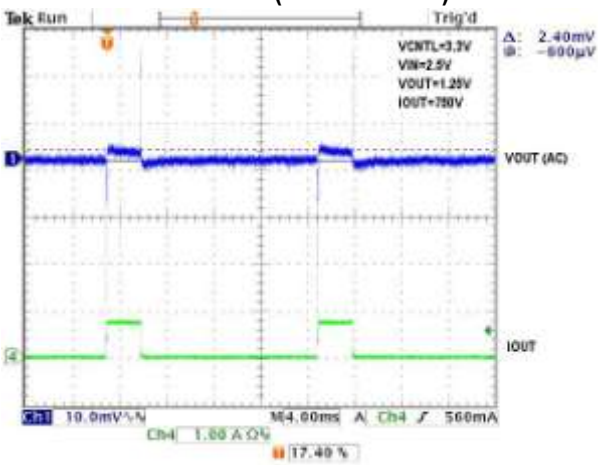
Transient (Sink Current)



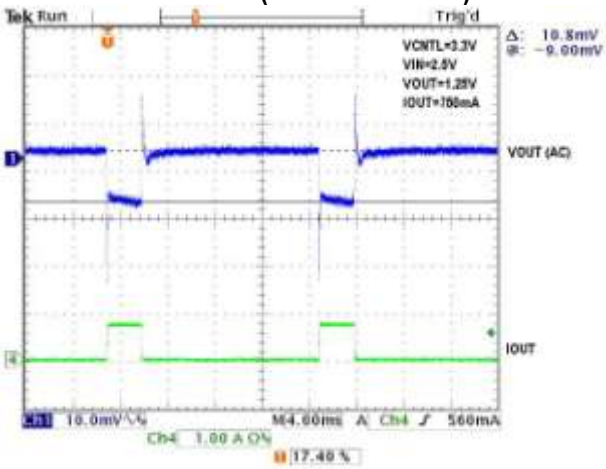
Transient (Source Current)



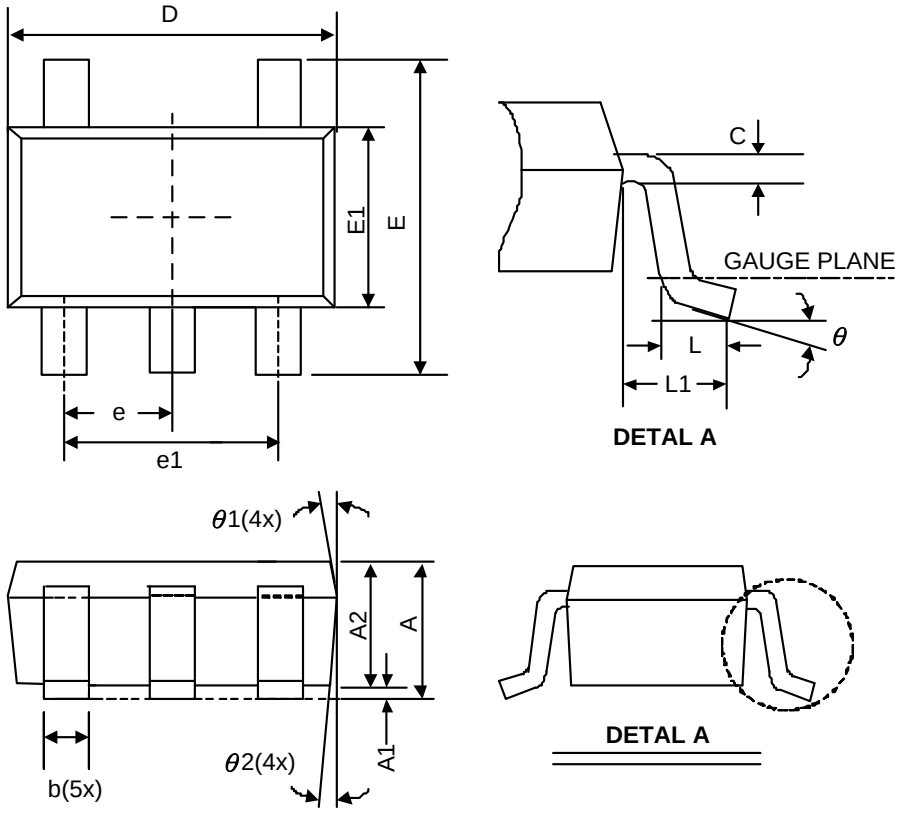
Transient (Sink Current)



Transient (Source Current)



❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.45	-	-	0.057
A1	0	0.08	0.15	0	0.003	0.006
A2	0.9	1.1	1.3	0.035	0.043	0.051
b	0.3	0.4	0.5	0.012	0.016	0.02
C	0.08	0.15	0.22	0.003	0.006	0.009
D	2.7	2.9	3.1	0.106	0.114	0.122
E1	1.4	1.6	1.8	0.055	0.063	0.071
E	2.6	2.8	3	0.102	0.11	0.118
L	0.3	0.45	0.6	0.012	0.018	0.024
L1	0.5	0.6	0.7	0.02	0.024	0.028
e1	1.9 BSC			0.075 BSC		
e	0.95 BSC			0.037 BSC		
θ	0°	4°	8°	0°	4°	8°
θ 1	5°	10°	15°	5°	10°	15°
θ 2	5°	10°	15°	5°	10°	15°

JEDEC outline: MO-178 AA