1A Sink/Source Bus Termination Regulator with 1A LDO

❖ GENERAL DESCRIPTION

The AX1252 is a 1A low dropout linear regulator with a high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The DDR regulator is capable of actively sinking or sourcing up to 1A. The output termination voltage cab be tightly regulated to track 1/2VDD by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The AX1252 has an adjustable output LDO. The regulator output can be used to DDR input (VDD) this application is avoided two power input. The supply voltage is from 2.8V to 5.5V.

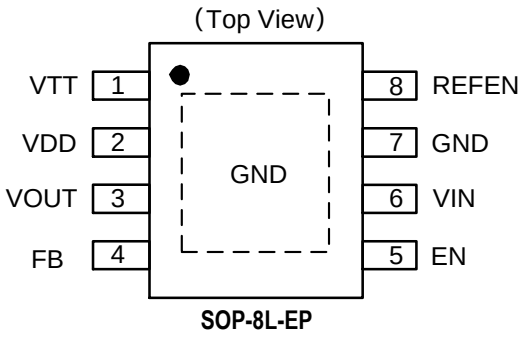
The AX1252 incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in and thermal shut-down protection. The AX1252 is available in the SOP-8L-EP (Exposed Pad) surface mount package.

❖ FEATURES

- Ideal for DDR-I, DDR-II and DDR-III VTT Applications
- Each channel 1A Continuous Current for LDO and DDR
- Integrated Power Driver
- Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- DDR Output Adjustment by Two External Resistors
- LDO adjustable output by outside resistors.
- Low External Component Count
- Independent Shutdown function
- Current Limiting and Thermal Shutdown Protections
- SOP-8L with exposed pad Pb-Free Package.

❖ PIN ASSIGNMENT

The package of AX1252 is SOP-8L-EP; the pin assignment is given by:



SOP-8L-EP

Name	Description
VIN	LDO power supply pin
VDD	DDR IC power supply pin
GND	Ground pin
REFEN	Reference voltage input and chip enable
VTT	DDR IC Output Voltage pin
VOUT	LDO Output Voltage pin
EN	LDO shutdown input pin
FB	LDO feedback input for setting the output voltage.

❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
AX1252 XX X Package Type ES: SOP-8L-EP Packing Blank: Tube A : Taping	Logo ← AX1252 → Part number Y Y WW X → ID code: internal WW: 01~52 Year: 10=2010 11=2011

❖ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Characteristics	Symbol	Rating	Unit
Input Voltage **(Note1)**	V_{IN}	2.6 to 5.5	V
VDD Input Voltage	V_{DD}	2.5 to 1.5 ±3%	V
VOUT Voltage	V_{OUT}	0.8 to 5.0	V
VIN Supply Voltage	V_{IN}	7	V
VDD Supply Voltage	V_{DD}	6	V
EN Voltage	V_{EN}	GND - 0.3 to + 6	V
Power Dissipation	PD	Internally Limited	W
Ambient Temperature	T_A	-40 to +85	°C
Junction Temperature	T_J	-40 to +125	°C
Storage Temperature Range	T_{ST}	-65 to +150	°C
Thermal Resistance from Junction to case	θ_{JC}	15	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	40	°C/W

Note: θ_{JA} is measured with the PCB copper area (need connect to Exposed pad) of approximately 1.5 in^2 (Multi-layer).

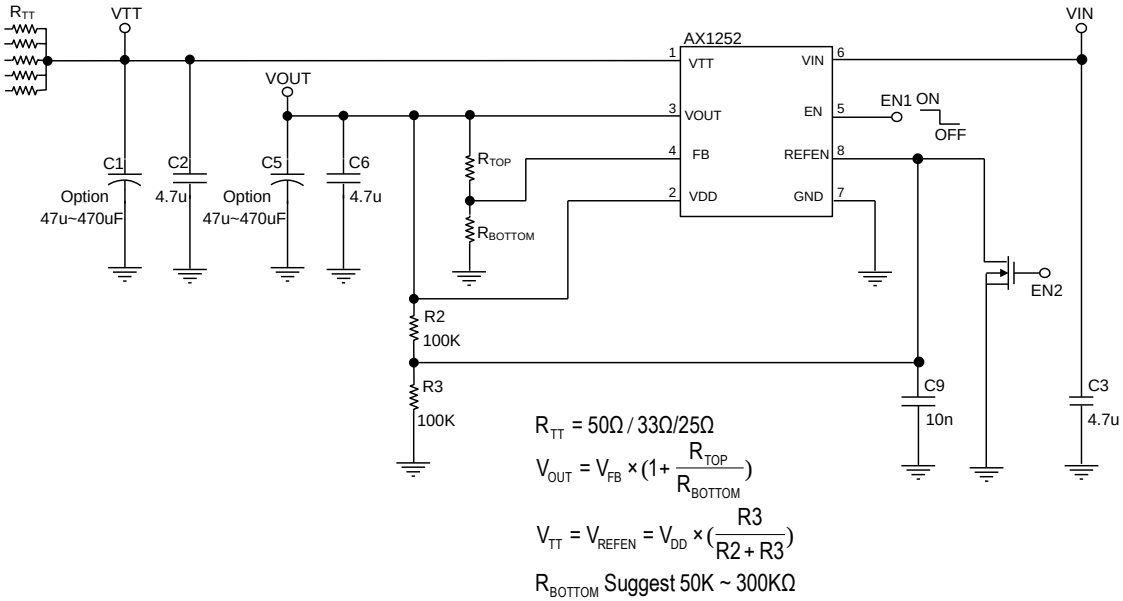
❖ ELECTRICAL CHARACTERISTICS

V_{DD}=2.5V/1.8V/1.5V, V_{IN}=3.3V, V_{REFEN}=1.25V/0.9V/0.75V, C_{OUT}=4.7µF (Ceramic), T_A=25ºC, unless otherwise specified

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
V_{IN} Operating Current	I_{IN}	I_{OUT}=0A, I_{TT}=0A	-	1	2.5	mA
Standby Current	I_{STB}	V_{REFEN} < 0.2V (Shutdown) R_{TT} = 180Ω, V_{EN} = 0V	-	150	200	uA
Thermal Shutdown	T_{SD}		-	140	-	°C
Thermal Shutdown Hysteresis	T_{SH}		-	20	-	°C
DDR Channel						
Output Offset Voltage **(Note2)**	V_{OS}	I_{TT}=0A	-10	-	+10	mV
Shutdown Threshold	V_{REF-H}	Enable	0.6	-	-	V
	V_{REF-L}	Shutdown	-	-	0.2	V
Load Regulation **(Note3)**	$\triangle V_{TT}$	I_{TT}=+0.75A	-20	-	+20	mV
		I_{TT}=-0.75A				
Current Limit **(Note 4)**	CL		1.1	-	-	A
LDO Channel						
FB Voltage	V_{FB}	V_{IN}=2.6V to 5.5V I_{OUT}=1mA	0.784	0.8	0.816	V
FB Input Leakage Current	I_{FB}	V_{FB} = 0.8V	-100	-	+100	nA
Dropout Voltage	V_{DROP}	I_{OUT}=1.0A, V_{OUT}=1.50V	-	1.10	1.4	V
		I_{OUT}=1.0A, V_{OUT}=1.80V	-	0.8	1.1	
		I_{OUT}=1.0A, V_{OUT}=2.50V	-	0.57	0.7	
Current Limit **(Note 4)**	I_{LIMIT}		1.3	1.5	-	A
Short Circuit Current	I_{SHORT}	Output Voltage < 0.375*V_{OUT}	-	600	-	mA
Load Regulation	ΔV_{OUT}	I_{OUT} = 10m~1.0A	-	0.5	1	%
Enable Input Threshold	V_{ENH}	Regulator Enable	2.0	-	-	V
	V_{ENL}	Regulator Shutdown	-	-	0.6	V

Note 1: Minimum V_{IN} voltage is defined by output adds a dropout voltage.
Note 2: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.
Note 3: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 0.75A.
Note 4: Current limit is measured at constant junction temperature by using pulsed testing with a low ON time.

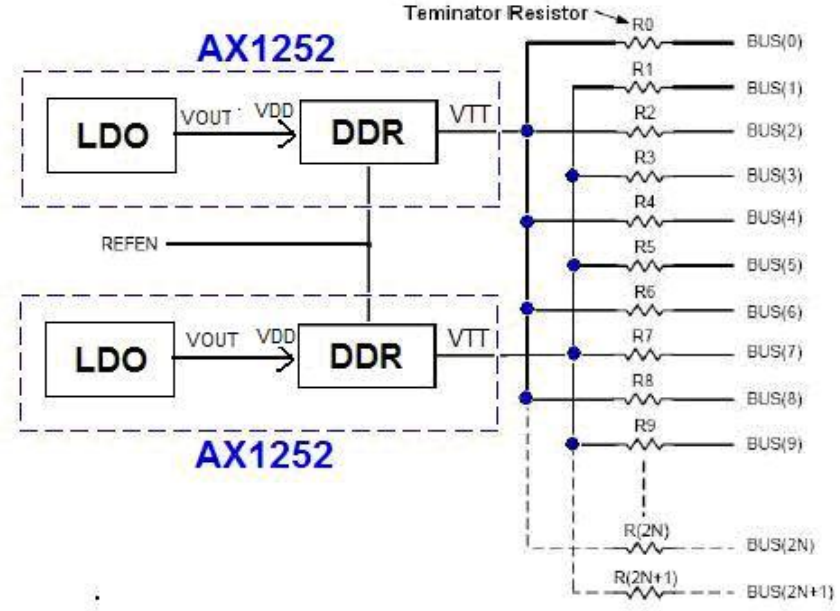
❖ APPLICATION CIRCUIT



❖ APPLICATION INFORMATION

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the low pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



General Regulator

The AX1252 include one low dropout regulator (LDO) and one general linear regulator (DDR). The LDO's output is an adjustable version, the FB voltage is 0.8V. The output voltage can be set by outside resistances. The output voltage, $V_{OUT,}$ is then given by the following equation:

$$V_{OUT} = 0.8* (1 + R_{TOP}/R_{BOTTOM})$$

For the reasons of reducing power dissipation and loop stability, R_{BOTTOM} is recommending to choose 50K~300KΩ.

The DDR channel accepts an external reference voltage at REFEN pin and provides output voltage regulated to this reference voltage.

$$V_{TT} \fallingdotseq V_{REFEN} = V_{DD}* R3*(R2+R3)$$

Normally, for idea DDR-I, DDR-II and DDR-III applications, the LDO channel supply VDD voltage to DDR channel used.

Capacitor Selection

Normally, use a 4.7μF Multi-layer chip capacitor (MLCC) on the input and output capacitors are sufficient. A lower ESR (X5R, X7R) is recommended for input and output capacitors. Add a larger than 47uF in output capacitors (LDO and DDR) to provide better output-noise and transient response. A higher- value output capacitor may be necessary if large, fast transients are anticipated and the device is located several inches from the power source.

Thermal Considerations

The AX1252 series can deliver a current of up to 1A over the full operating junction temperature range by each channel. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

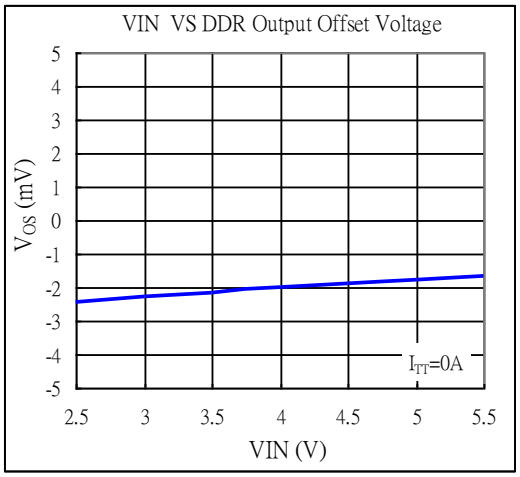
$$PD\ (MAX) = (T_{J\ (MAX)} - T_A) / \theta_{JA}$$

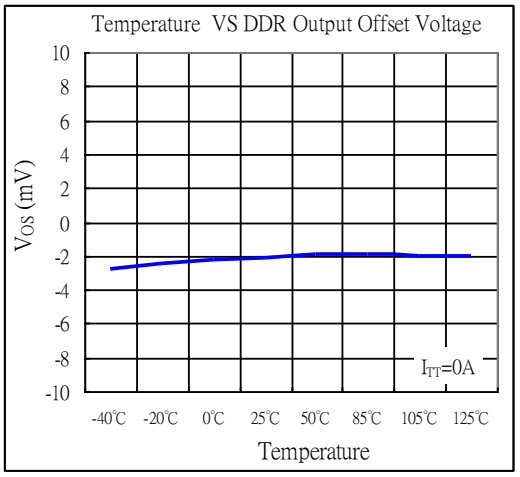
Where $T_{J\ (MAX)}$ is the maximum junction temperature of the die (125° C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) for SOP-8L-EP (Exposed pad) package at recommended minimum footprint is 40°C/W on 1.5 in^2 and Multi-layer PCB layout. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

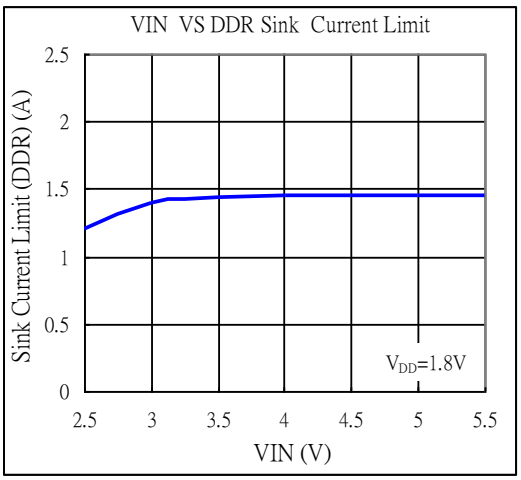
$$PD\ (MAX) = (125°C - 25°C) / 40°C/W = 2.5W$$

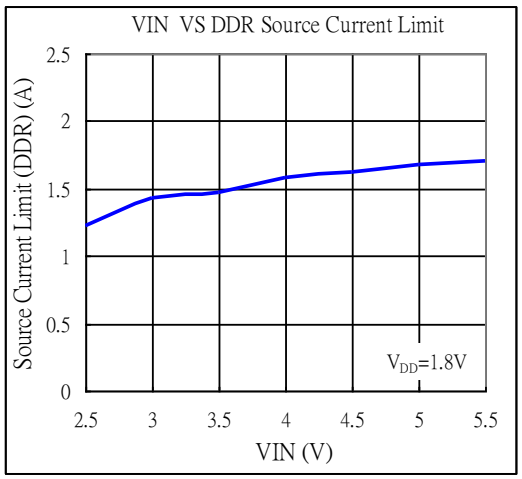
The thermal resistance θ_{JA} of SOP-8L-EP (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of SOP-8L-EP package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

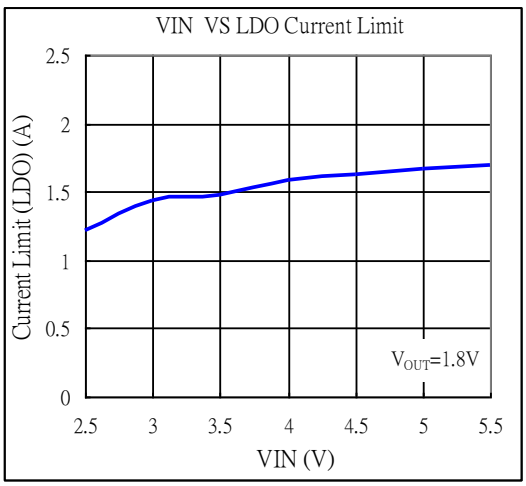
❖ TYPICAL CHARACTERISTICS

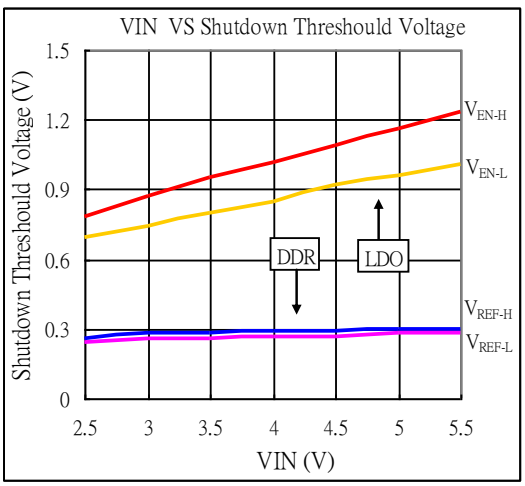




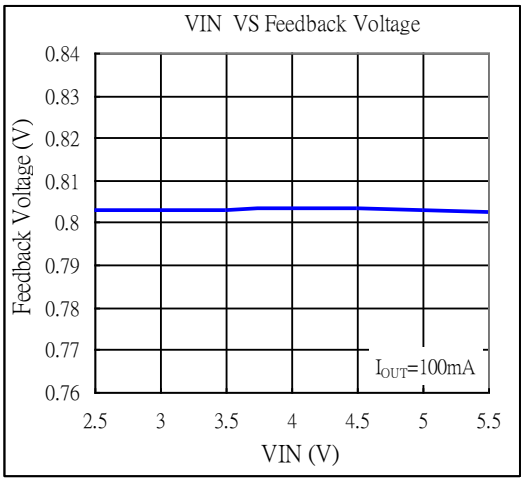


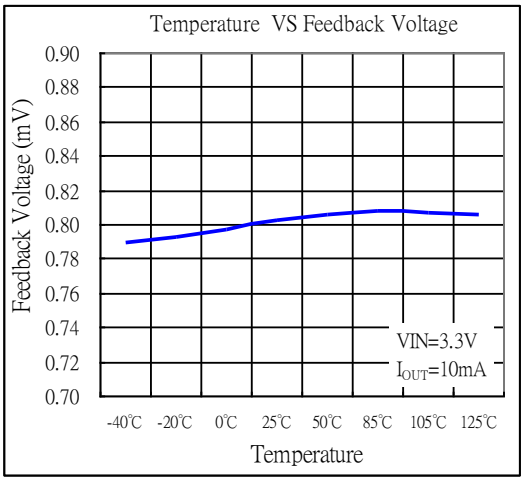


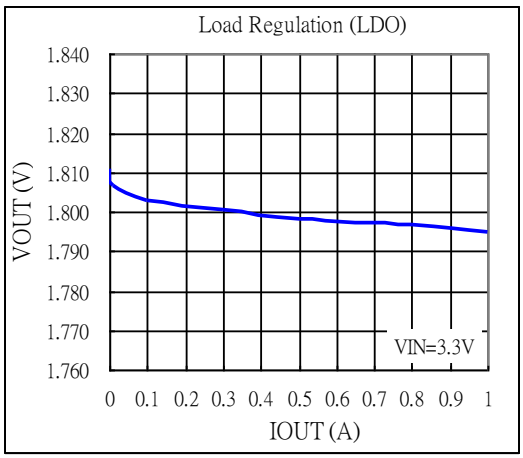


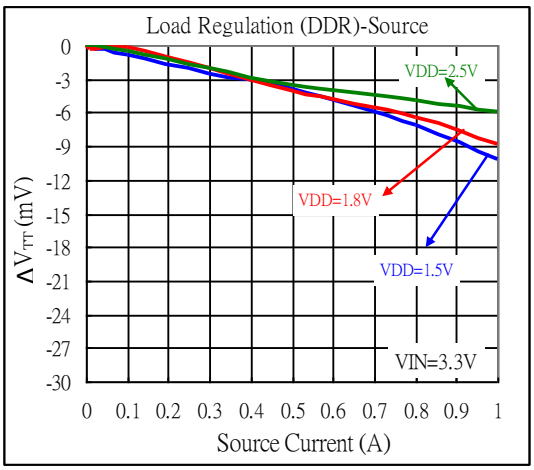


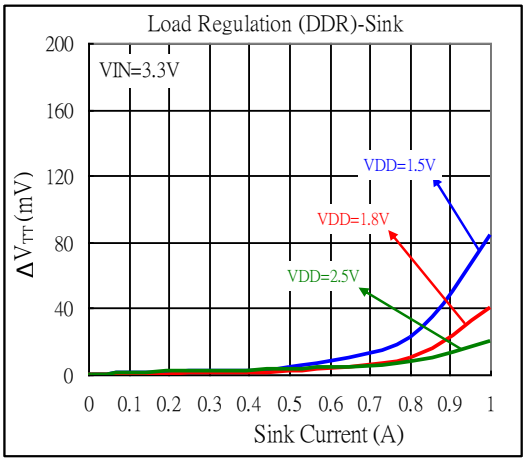
❖ TYPICAL CHARACTERISTICS (CONTINUOUS)





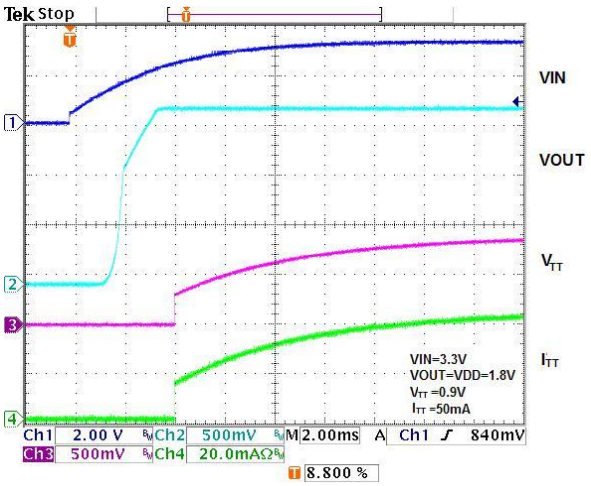




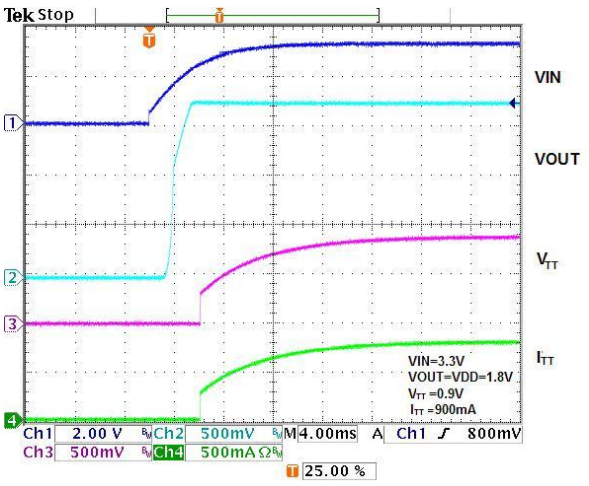


❖ TYPICAL CHARACTERISTICS (CONTINUOUS)

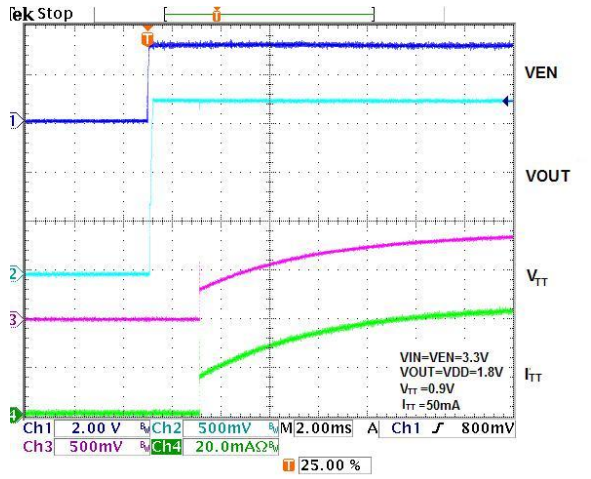
Power ON



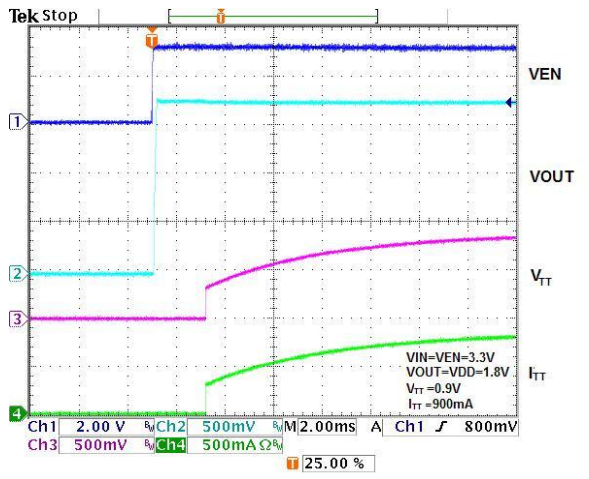
Power ON



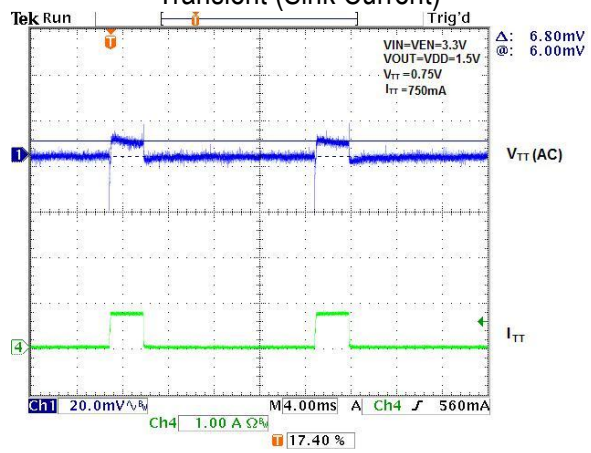
EN ON



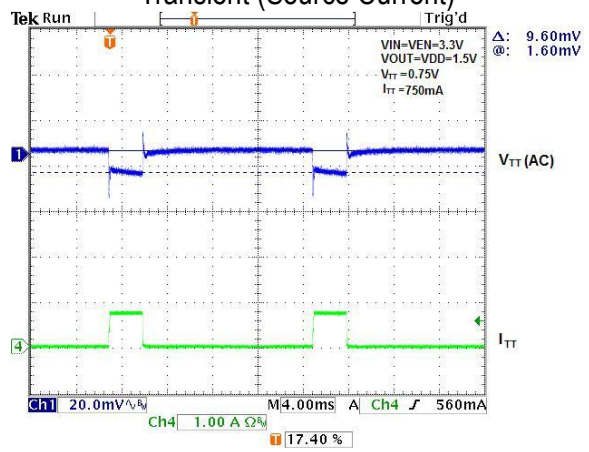
EN ON



Transient (Sink Current)

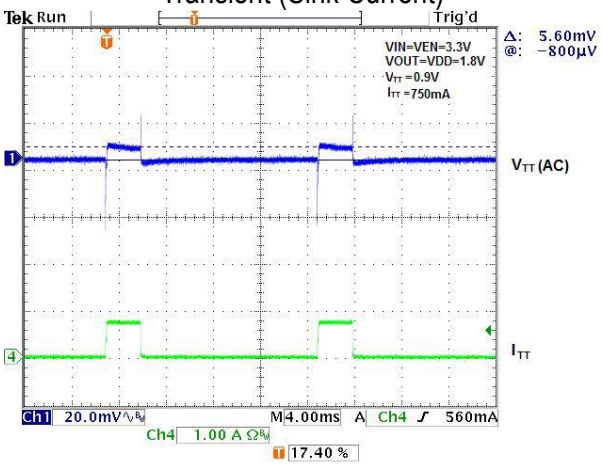


Transient (Source Current)



❖ TYPICAL CHARACTERISTICS (CONTINUOUS)

Transient (Sink Current)



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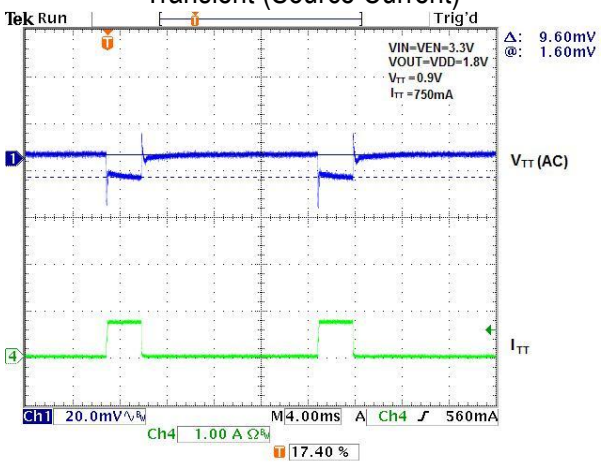

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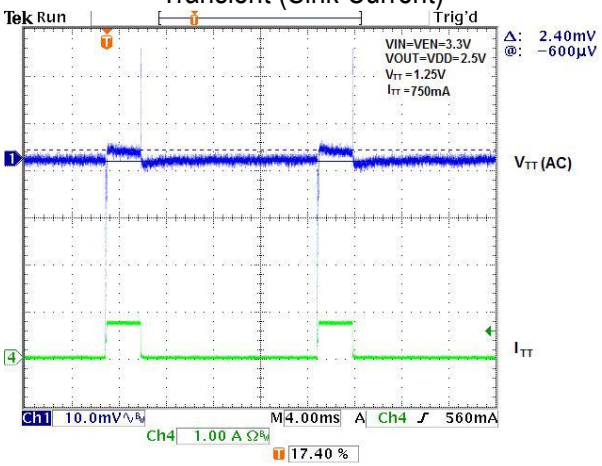

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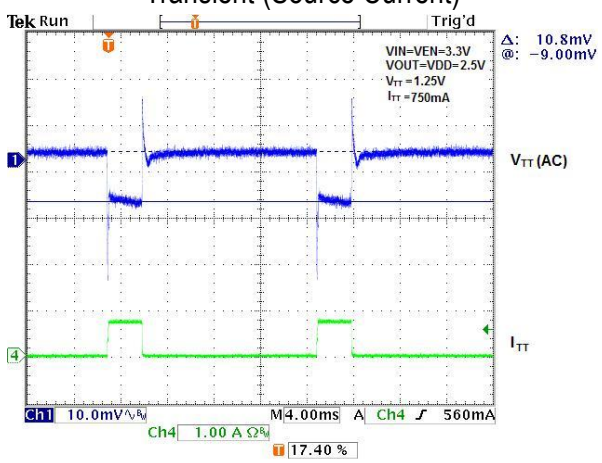
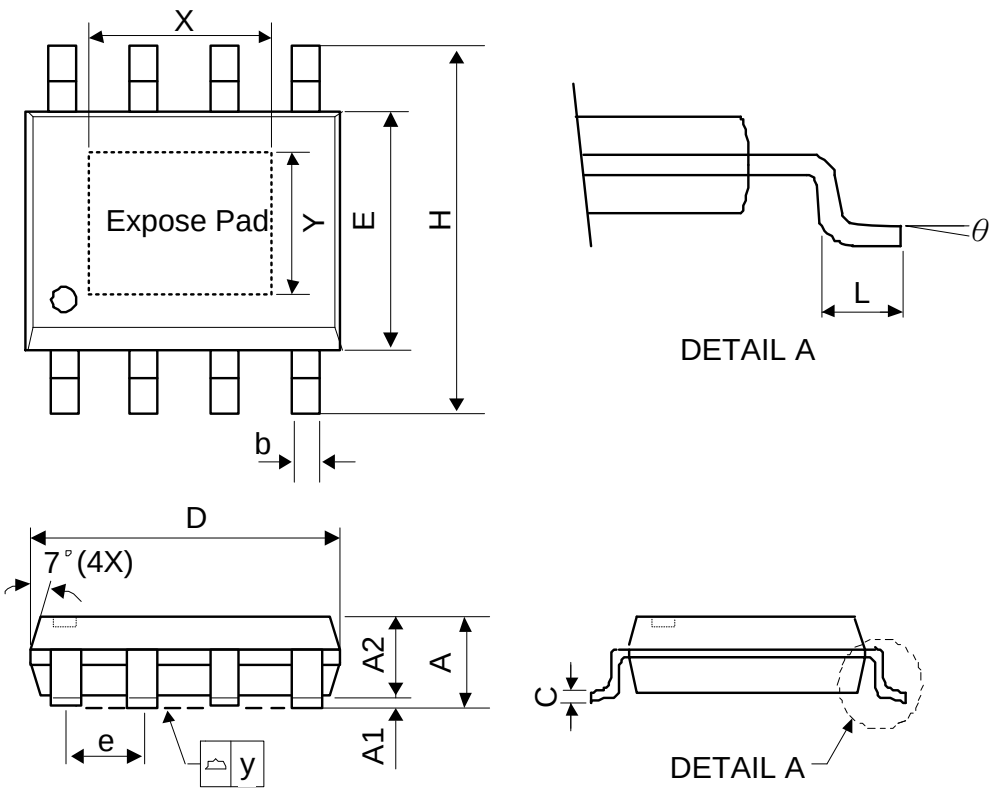


❖ PACKAGE OUTLINES



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.75	-	-	0.069
A1	0	-	0.15	0	-	0.06
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
X	-	2.34	-	-	0.092	-
Y	-	2.34	-	-	0.092	-
θ	0°	-	8°	0°	-	8°

Mold flash shall not exceed 0.25mm per side
JEDEC outline: MS-012 BA