PT1305

High Voltage Step-Up Converter

GENERAL DESCRIPTION

The PT1305 is a step-up DC/DC converter designed for driving up to 24V from a single cell Lithium Ion battery. The PT1305 switches at 1.25MHz, allowing the use of tiny, low cost and low height inductors and capacitors. A constant frequency internally compensated current mode PWM architecture results in low, predictable output noise that is easy to filter. Low ESR ceramic capacitors can be used at the output, further reducing noise to millivolt level. The high voltage switch on the PT1305 is rated at 26V, making the devices ideal for boost converters up 24V. It can generate 18V at 30mA from 3.6V supply. The PT1305 is available in SOT23-5 and SOT23-6 packages.

FEATURES

- 18V at 30mA from 3.6V
- Up to 90% Efficiency
- 1.25MHz Fixed Switching Frequency
- High output voltage up to 24V
- Uses small surface mount components
- Low shutdown current < 1uA
- SOT23-5 and SOT23-6 Packages

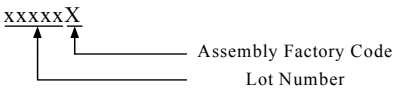
APPLICATIONS

- TFT-LCD Bias Supplies
- OLED Bias Supply
- Local 12V or 18V Supplies
- Cordless phones
- Digital Cameras

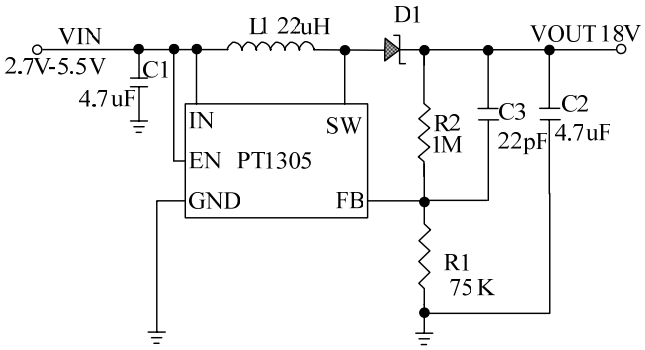
ORDERING INFORMATION

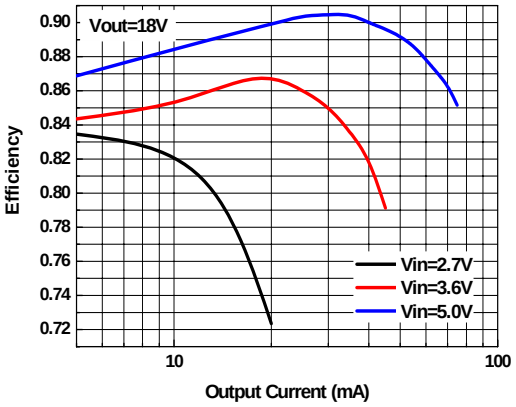
PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
SOT23-5	-40 °C to 85 °C	PT1305E23E	Tape and Reel 3000 units	PT1305 xxxxxX
SOT23-6	-40 °C to 85 °C	PT1305E23F	Tape and Reel 3000 units	PT1305 xxxxxX

Note:

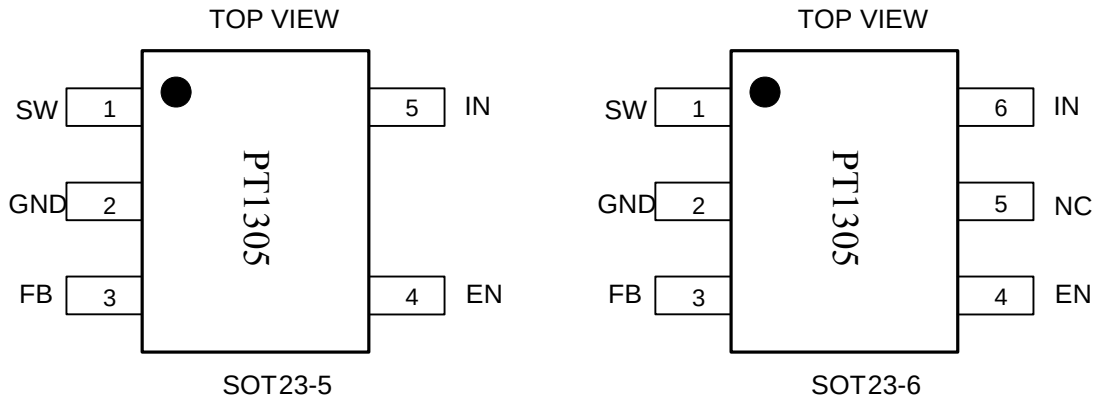


TYPICAL APPLICATIONS





PIN ASSIGNMENT



PIN DESCRIPTION

SOT23-5 Pin No.	SOT23-6 Pin No.	PIN NAMES	DESCRIPTION
1	1	SW	Power Switch Output. Connect the inductor and the blocking Schottky diode to SW.
2	2	GND	Ground
3	3	FB	Feedback input pin. The reference voltage at this pin is 1.25V.
4	4	EN	Enable pin. A high input at EN enables the device and a low input disables the devices. When not used, connect EN to the input source for automatic startup.
	5	NC	Not connection
5	6	IN	Input Supply Pin. Must be locally bypassed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	ITEMS	VALUE	UNIT
V_{IN}	Input Voltage	-0.3～6	V
V_{SW}	Voltage at SW Pin	-0.5～30	V
V_{IO}	All Other I/O Pins	GND-0.3 to VDD+0.3	V
P_{DMAX}	Power Dissipation (Note 2)	Internally Limited	W
P_{TR1}	Thermal Resistance，SOT-23-5, Θ_{JA}	220	℃/W
P_{TR2}	Thermal Resistance，SOT-23-6, Θ_{JA}	220	℃/W
Tstg	Storage Temperature	-55 to 150	℃
Tsolder	Package Lead Soldering Temperature	260℃, 10s	
	ESD Susceptibility (Note 3)	3	kV

RECOMMANDED OPERATING RANGE (Note 1)

SYMBOL	ITEMS	VALUE	UNIT
V_{IN}	VIN Supply Voltage	2.7 to 5.5	V
V_{SW}	Output Voltage	V_{IN} to 26	V
T_{OPT}	Operating Temperature	-40 to +85	℃

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS (Note 4, 5)

The following specifications apply for V_{IN}= V_{EN} =3.6V T_A=25 °C, typical application circuit, unless specified otherwise.

SYMBOL	ITEMS	CONDITIONS	Min.	Typ.	Max.	UNIT
V_{IN}	Input Voltage		2.7		5.5	V
V_{FB}	FB Pin Voltage	Open loop	1.125	1.25	1.375	V
Ioff	Operating Current（Shutdown）			0.1	1	μA
Isby	Operating Current（Quiescent）	V_{FB}=1.5V		100	350	μA
Fsw	Switching Frequency		1.0	1.25	1.5	MHz
Dmax	Maximum Duty Cycle	V_{FB}=0V	85	90		%
V_{EN_H}	EN Minimum High Level		1.5			V
V_{EN_L}	EN Maximum Low Level				0.4	V
R_{ON}	SW On Resistance			1.4		Ω
I_{LIMIT}	SW Current Limit			400		mA
I_{SW}	SW leakage current	V_{IN}= V_{EN} =0V, V_{SW} =30V		0.1	1	μA

Note 4: Typical parameters are measured at 25˚C and represent the parametric norm.

Note 5: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

SIMPLIFIED BLOCK DIAGRAM

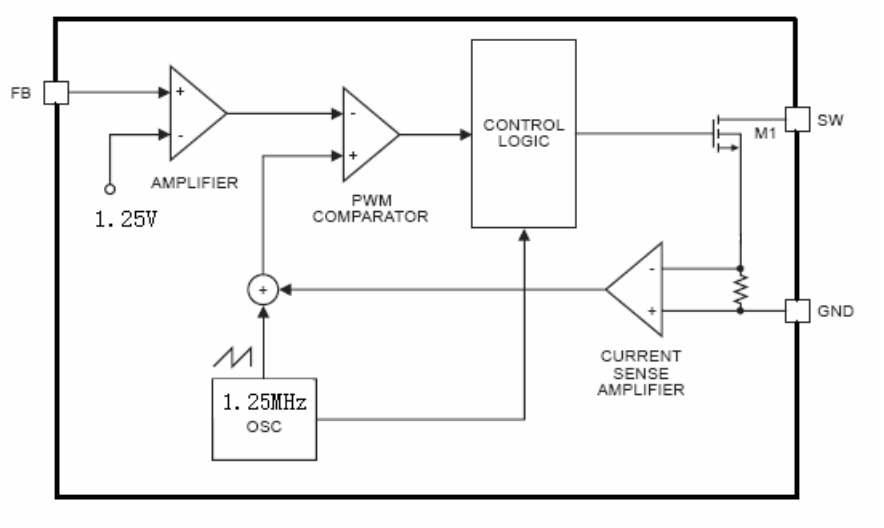


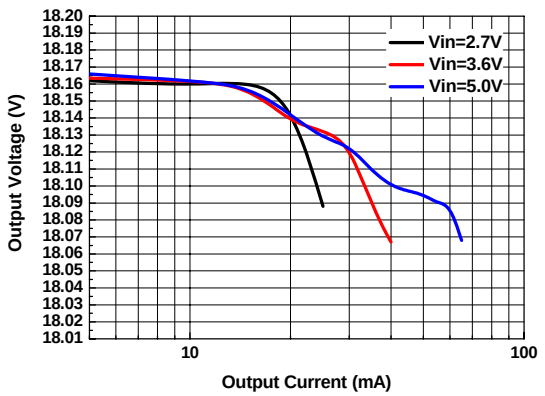
Figure 3. Simplified Block Diagram of the PT1305

OPERATION DESCRIPTION

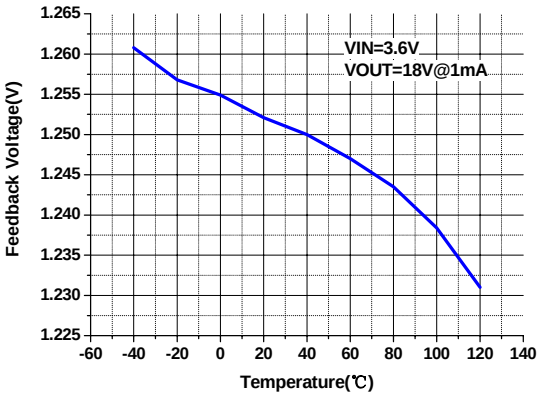
The PT1305 uses a constant frequency, peak current mode boost regulator architecture to regulate the output voltage. The operation of the PT1305 can be understood by referring to the simplified block diagram shown above. At the start of each oscillator cycle, the control logic turns on the power switch M1. The signal at the non-inverting input of the PWM comparator is proportional to the switch current, summed together with a portion of the oscillator ramp. When this signal reaches the level set by the output of error amplifier, the PWM comparator resets the latch in the control logic and turns off the power switch. In this manner, error amplifier sets the correct peak current level to keep the output voltage in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. This results in more current to flow through M1, hence increasing the power delivered to the output.

TYPICAL PERFORMANCE CHARACTERISTICS

Load regulation



Feedback voltage Vs Temperature



APPLICATION INFORMATION

- **Inductor Selections**

For most of the applications of the PT1305, it is recommended to use an inductor of 22uH. Although small size is one of the major factors in selecting an inductor, the smaller and thinner inductors give higher core losses at 1.25MHz and DRC, resulting in lower efficiencies. The following tab le provides a list of recommended inductors:

PARTNUMBER	DCR（Ω）	CURRENT RATING (mA）	MANUFACTURER
LQH3C220	0.71	250	MURATA
CDRH3D16-220	0.53	350	SUMIDA
LB2012B220M	1.7	75	TAIYO YUDEN
LEM2520-220	5.5	125	TAIYO YUDEN
EJPC220KF	4.0	160	PANASONIC

- **Capacitor Selection**

The small size of ceramic capacitors makes them ideal for PT1305 applications. X5R and X7R types are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 4.7 F input capacitor and a 4.7 F output capacitor are sufficient for most PT1305 applications.

The compensation capacitor C3 is selected as 22p in the typical application.

- **Diodes Selection**

Schottky diodes, with their low forward voltage drop and fast reverse recovery, are the ideal choices for PT1305 applications. The forward voltage drop of a Schottky diode represents the conduction losses in the diode, while the diode capacitance (CT or CD) represents the switching losses. For diode selection, both forward voltage drop and diode capacitance need to be considered. Schottky diodes with higher current ratings usually have lower forward voltage drop and larger diode capacitance, which can cause significant switching losses at the 1.25MHz switching frequency of the PT1305.

- **Resistor Selection**

The output voltage is controlled by the feedback resistor. The feedback reference is 1.25V. The output voltage is 1.25*(1+R2/R1). In order to have accurate output voltage, precision resistors are preferred (1% is recommended). The formula and table for R_1 and R_2 selection are shown below

$$V_{OUT} = 1.25*(1+R2/R1)$$

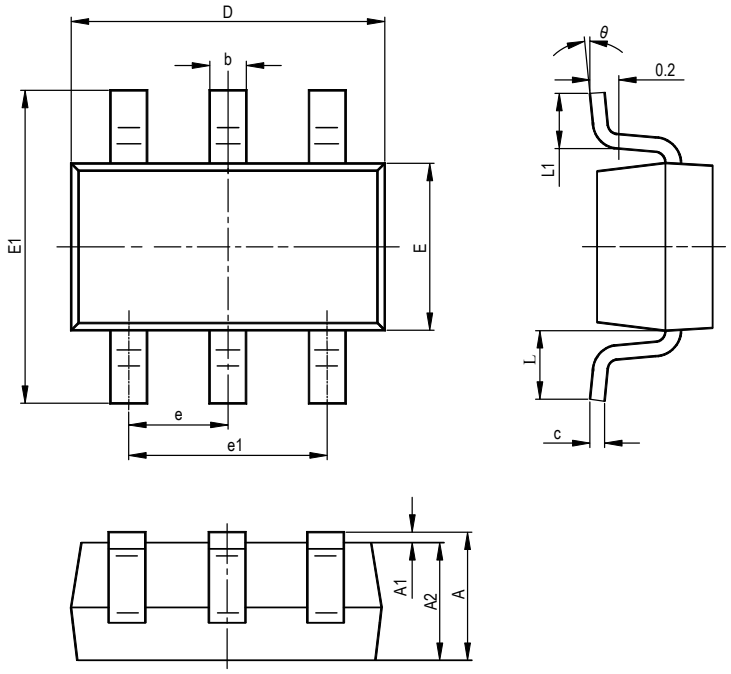
V_{OUT} （V）	R_1 Value （KΩ）	R_2 Value （KΩ）
12	210	1800
15	90	1000
18	75	1000
24	100	1800

- **Board Layout Consideration**

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signal of the SW pin has sharp rise and fall edges. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. In addition, the ground connection for the feedback resistor R1 should be tied directly to the GND pin and not shared with any other component, ensuring a clean, noise-free connection.

PACKAGE INFORMATION

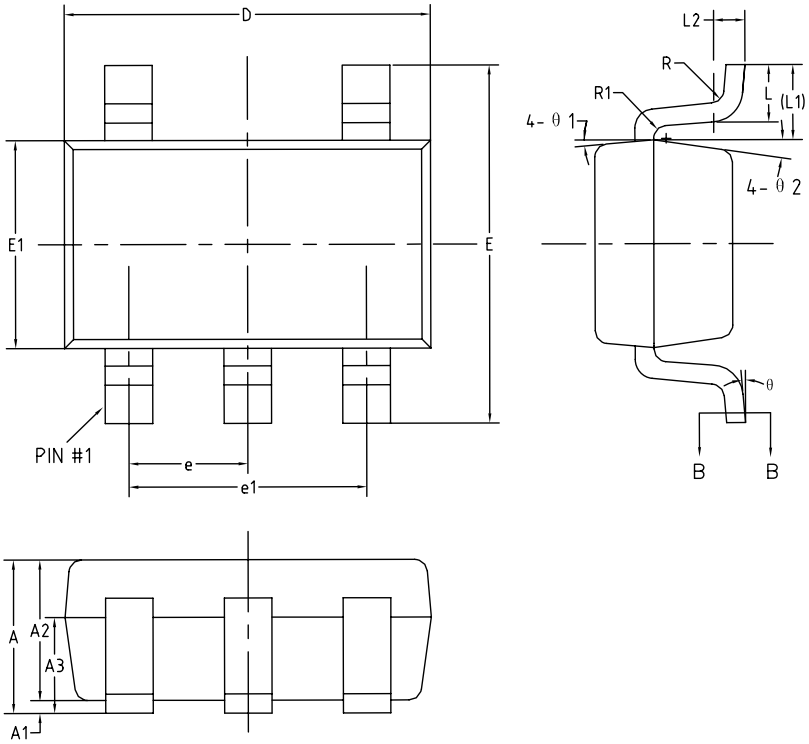
SOT23-6



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

PACKAGE INFORMATION

SOT23-5



SYMBOL	MILLIMETERS		
	MIN	TYP	MAX
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.95BSC		
e1	1.90BSC		
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	-	8°
θ1	3°	5°	7°
θ2	6°	8°	10°