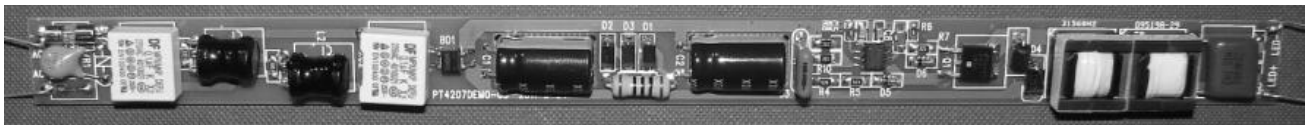
APPLICATION NOTE

Title	**20W T8 Non-isolated LED Driver Using PT4207**
Applications	**AC/DC LED Lighting**
Specification	**AC Input Range: 175-265Vac** **DC Output: 76V/240mA (CC) for Driving 12 Strings of 24pcs 20mA LED in Series**
Model No.	**PT4207_T8_01**
Doc. No.	**PT4207_AN01**
Revision	**1.1**



FEATURES

- Over 92% Efficiency
- More than 0.89 Power Factor
- Achieve ±5% Output Current Accuracy
- Soft-Start/Output Short Protection
- Fully Compliance with EN55015/CIPPR-22 Class B EMI Requirements

Table of Contents

1 INTRODUCTION

This application notes describes a non-isolated, power factor corrected, low THD, high-efficiency LED driver designed for T8 LED tube to drive 12 strings of 24pcs LED in series with 240mA constant current from an input voltage range of 175 VAC to 265 VAC based on PT4207 LED Driver.
This application notes contains the LED driver specification, schematic, PCB layout, bill of materials, magnetic components spec and test data. Please refer to datasheet for the details of LM4207

2 SPECIFICATION

DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
INPUT CHARATERISTIC					
Input Voltage		175	230	265	VAC
Input Current	Vin=175~230Vac			122	mA
Frequency		47	50/60	63	Hz
Power Factor	Vin=230Vac		0.903		
Efficiency	Vin=175~265Vac	92			%
OUTPUT CHARATERISTIC					
Rated Output Current	Driving 12 Strings of 24pcs LED in series		240		mA
Rated Output Voltage	Driving 24pcs LED in series		76		V
Line Regulation	Vin=175~265Vac			±1	%
Temperature Drift	Vin=230Vac, T=-20~80℃			±3	%
Turn-on Delay Time	Vin=230Vac		137		mS
PROTECTION					
Output Short Circuit Protection	Vin=230Vac	Shutdown with auto-restart			
Power on-off	Vin=230Vac, No Load, Ton=Toff=2s, 3000times		PASS		
ENVIRONMENTAL					
EMI		Meets CISPR22B / EN55022B			
Ambient Temperature	Free convection	-20		80	℃

3 DEMO BOARD PHOTO

FIGURE 1 TOP VIEW

4 SCHEMATIC

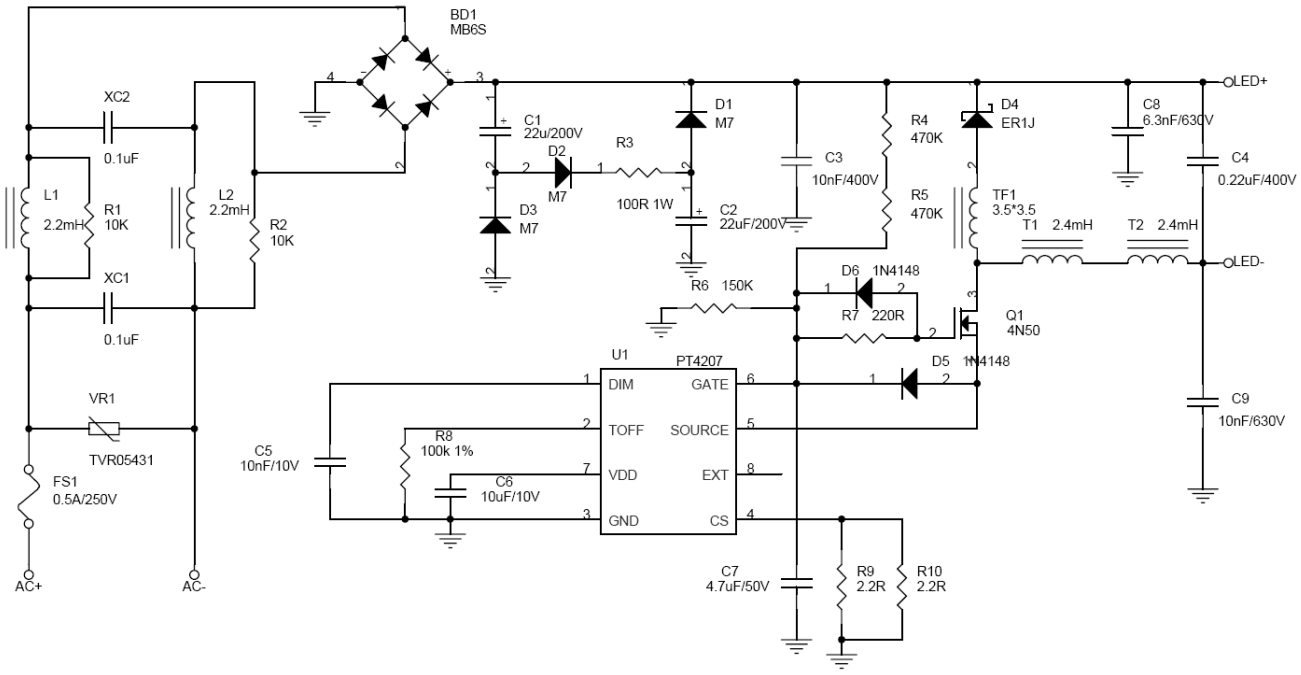


FIGURE 2 SCHEMATIC

5 PCB LAYOUT

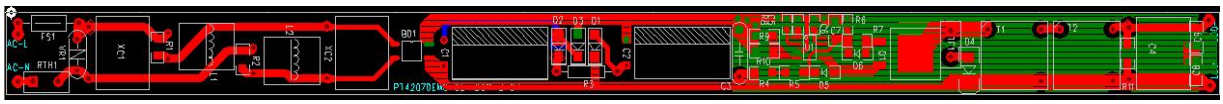


Figure 3 – PCB Layout (240mm*16mm)

6 BILL OF MATERIALS

Item	Reference	Description	QTY	Manufacturer
1	C1,C2	Electrolytic, 22uF/200V, RD series, Φ10mm*16mm	2	SAMWHA
2	C3	CBB Cap, 10nF/400V, P=7.5mm	1	Panasonic
3	C4	CBB Cap, 0.22uF/400V, P=10mm	1	Panasonic
4	C5	Ceramic, 0.01uF/10V, X7R, 0805	1	FENGHUA
5	C6	Ceramic, 10uF/10V, X7R, 0805	1	FENGHUA
6	C7	Ceramic, 4.7uF/50V, X7R, 1206	1	FENGHUA
7	C8,C9	Ceramic, 0.01uF/630V, X7R, 1206	2	FENGHUA
8	XC1,XC2	X2 Cap, 0.1uF/275VAC, P=10mm	2	VISHAY
9	R1,R2	Chip Resistor, 10K, ±5%, 1206	2	FENGHUA
10	R3	MetalFilm Resistor, 100R/1W	1	YAGEO

Item	Reference	Description	QTY	Manufacturer
11	R4,R5	Chip Resistor, 470K, ±5%, 1206	2	FENGHUA
12	R6	Chip Resistor, 150K, ±5%, 0805	1	FENGHUA
13	R7	Chip Resistor, 220R, ±5%, 1206	1	FENGHUA
14	R8	Chip Resistor, 100K, ±1%, 0805	1	FENGHUA
15	R9,R10	Chip Resistor, 2.2R, ±1%, 1206	2	FENGHUA
16	D1,D2,D3	Diode, General Rectifier, 1A/1kV, SMA	3	SIYU
17	D4	Diode, Ultra fast, ER1J, 1A/600V, SMB	1	DIODES
18	D5,D6	Diode, Fast recover, 1N4148, 0.1A/75V, SOD123	2	VISHAY
19	BD1	Bridge Rectifier, MB6S, 0.5A/600V, TO269AA	1	GENERAL SEMI
20	FS1	Fuse, 0.5A/250V	1	TY-OHM
21	T1,T2	Transformer Bobbin, E1312, Horizontal, 10pins	2	KANGSHUN
22	L1,L2	Power Inductor, SL1012-222	2	YAGEO
23	TF1	Ferrite Bead Inductor, Axial Φ3.5mm*5mm	1	TDK
24	Q1	MOSFET, N-Channel, 4N50, TO252	1	UTC
25	VR1	Varistor, TVR05431	1	THINKING
26	U1	IC, PT4207, SOP8	1	POWTECH

7 MAGNETIC COMPONENT SPECIFICATION

7.1 Physical Dimension

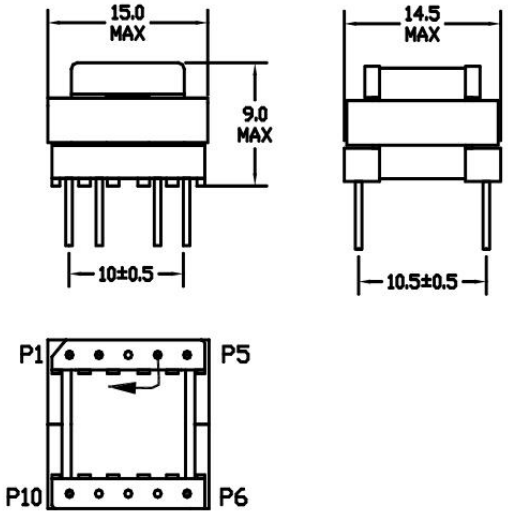


FIGURE 3 PHYSICAL DIMENSION

7.2 Winding Table

Winding	Terminal		Turns	Method	Wire			Insulation	
	Start	Finish			Type	Size*QTY	Layer	T/W	Layer
P1	1	10	180	Distribute Center	2UEW	0.23*1		0.025*8	2

7.3 Electrical Specifications

Item	Description	Condition	Limits
1	Inductance	Pin 1 to Pin10, measured at 40KHz, 1Vrms	2.4mH±5%

8 PERFORMANCE EVALUATION

All data were measured at TA=25^{o}C unless specified otherwise. The EUT were pre-heated for 0.5hrs before test.

8.1 PF and Efficiency

VIN	Iin	Pin	PF	Io	Vo	Eff.
(VAC)	(mA)	(W)		(mA)	(V)	(%)
175	121.3	19.611	0.925	239.0	75.97	92.58
200	106.2	19.527	0.915	238.2	75.91	92.60
230	93.46	19.495	0.903	238.6	75.85	92.83
265	82.43	19.46	0.891	238.0	75.80	92.71

8.2 Line and Load Regulation

Measuring the LED current under different Vin and the number of LED in series.
Unit: mA

Vin (VAC)	20LEDs Vo=64.0V	22LEDs Vo=70.4V	24LEDs Vo=76.8V	26LEDs Vo=83.2V	28LEDs Vo=89.6V	LoadReg (%)
175	250.3	244.6	239.0	235.8	228.1	9.27
200	250.4	244.7	238.2	235.6	227.4	9.61
230	249.6	244.3	238.6	235.7	227.3	9.33
265	249.6	243.9	238.0	235.2	227.4	9.30
LineReg(%)	0.32	0.33	0.42	0.25	0.35	

8.3 Output Current Deviation between chips

Measuring the LED current on the same board with 30pcs chip, Unit: mA

Condition: Vin=230Vac, 24LEDs in series output					
#1	236.8	#11	240.6	#21	241.7
#2	240.4	#12	238.3	#22	246.7
#3	235.6	#13	238.2	#23	240.8

#4	241.9	#14	236.7	#24	237.3
#5	238.2	#15	237.2	#25	244.8
#6	239.5	#16	239.6	#26	244.3
#7	238.8	#17	240.8	#27	244.0
#8	240.3	#18	241.0	#28	243.3
#9	239.1	#19	236.4	#29	244.5
#10	238.2	#20	235.4	#30	242.6
	Deviation=±2.35%				

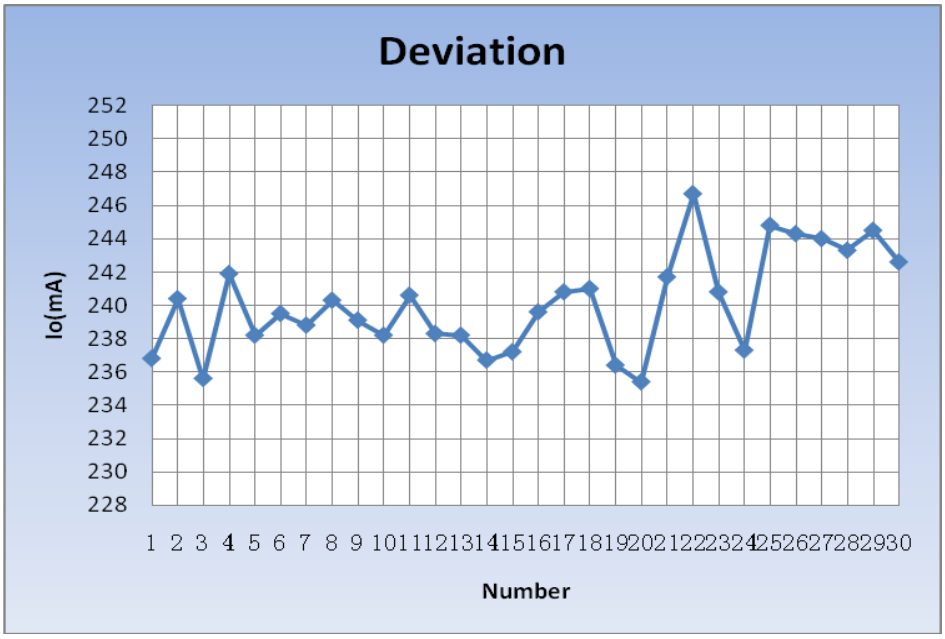


FIGURE 4 DEVIATION BETWEEN ICS

8.4 Temperature Drift

Test conditions: Vin=230VAC, Driving 12 strings of 24pcs LED in series

Temp(℃)	-20	0	20	40	60	80	Deviation (%)
Io(mA)	249	247	243	240	236	234	±3.1

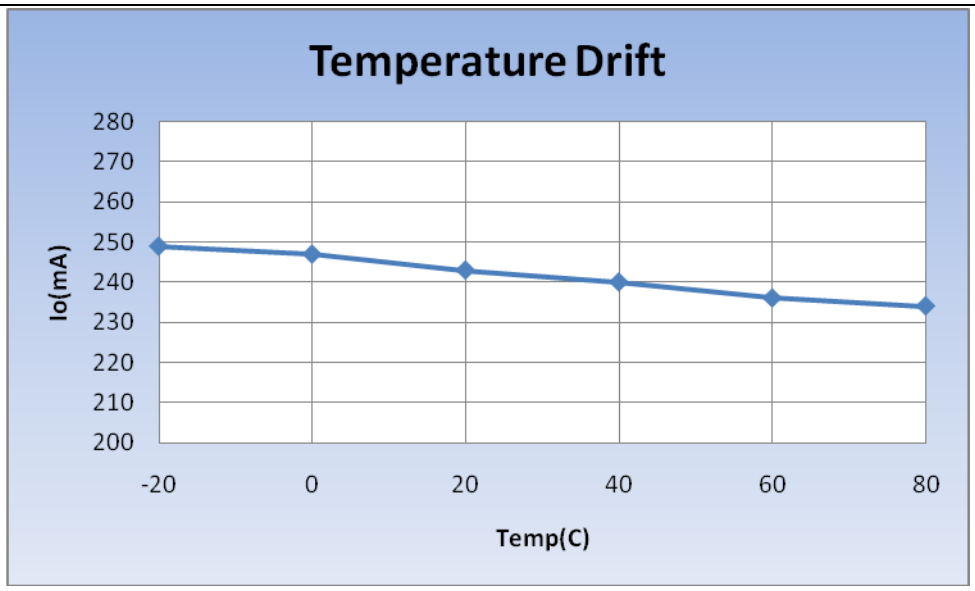


FIGURE 5 TEMPERATURE DRIFT OF LED CURRENT

8.5 Output Ripple Voltage and Current

Test Condition: Vin=230VAC, Driving 12 strings of 24pcs LED in series

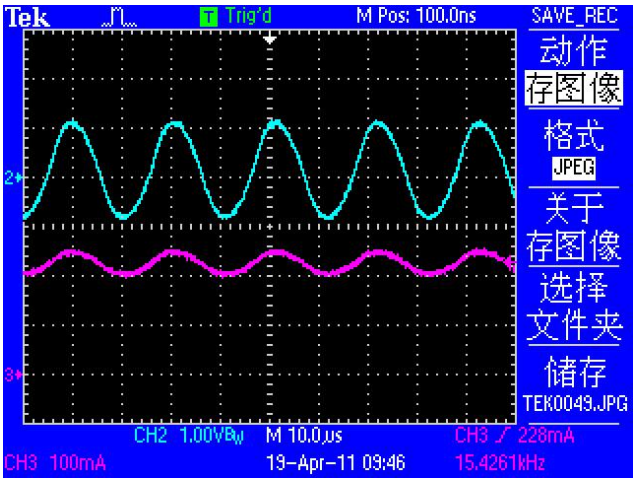


FIGURE 6 RIPPLE VOLTAGE AND CURRENT

8.6 Turn-on Delay Time

Test Condition: Vin=230VAC, Driving 12 strings of 24pcs LED in series

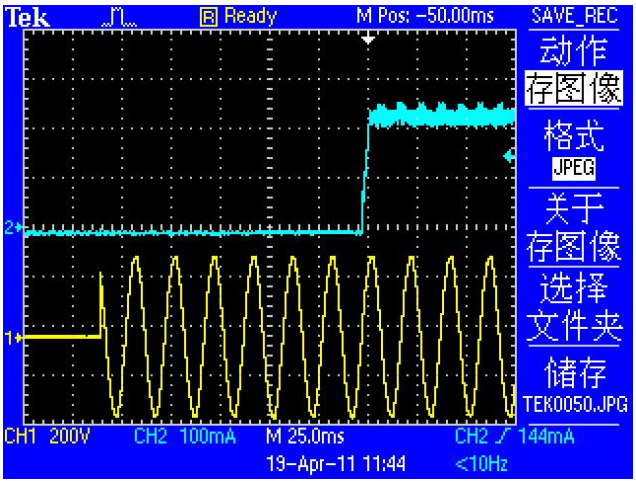


FIGURE 7 TURN-ON DELAY TIME

8.7 Thermal

Test Condition: in=230VAC, Driving 12 strings of 24pcs LED in series

Location	Temperature	Temp Rise
Ambient	24 C	
U1-Surface	39.3 C	15.3 C
T2-Core	37.0 C	13.0 C
D4-Pad	49.1 C	25.1 C
Q1-Drain Pad	51.3 C	27.1 C
C2-Surface	30.8 C	6.8 C

8.8 Output Short Protection

Vin(VAC)	175	200	230	265
Pin(mW)	93	110	130	180

8.9 Conducted EMI

Test Condition: Vin=230VAC, Driving 12 strings of 24pcs LED in series

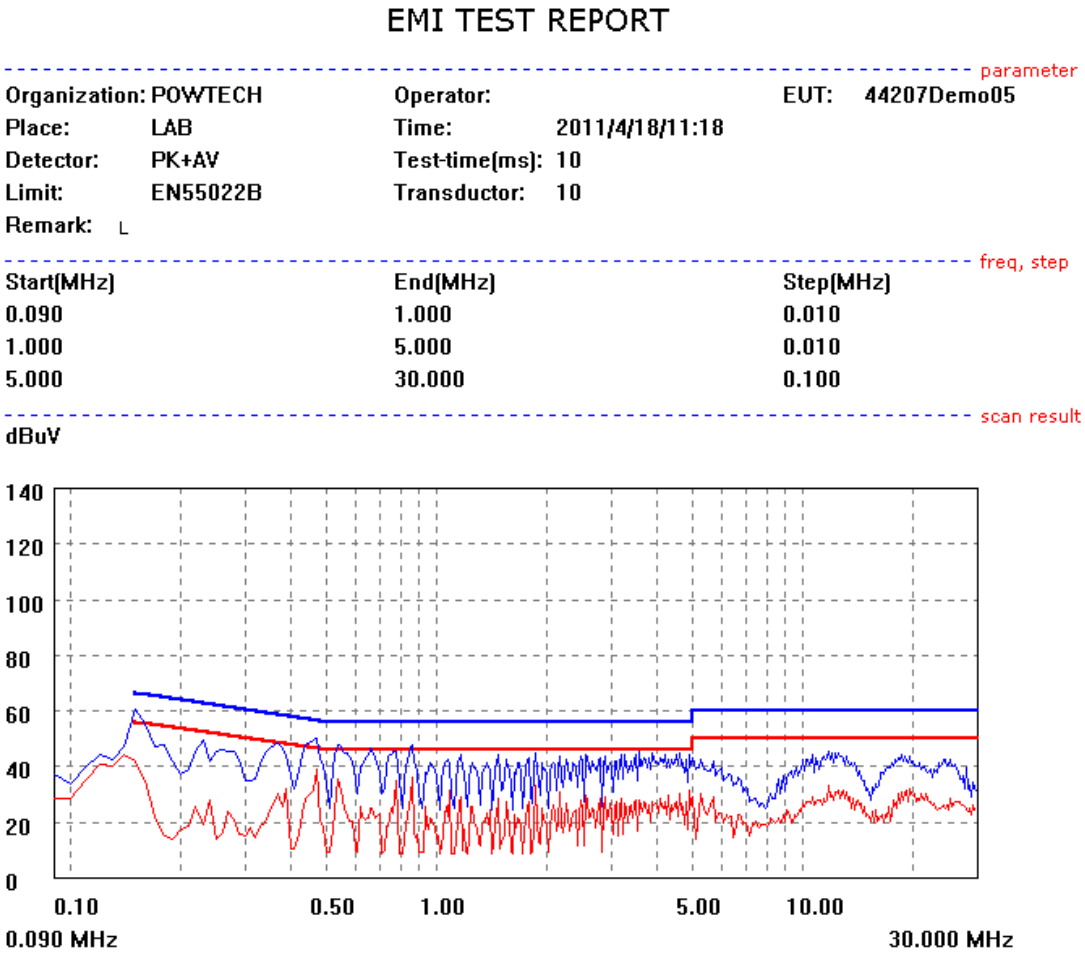


FIGURE 8 EMI CURVE－L

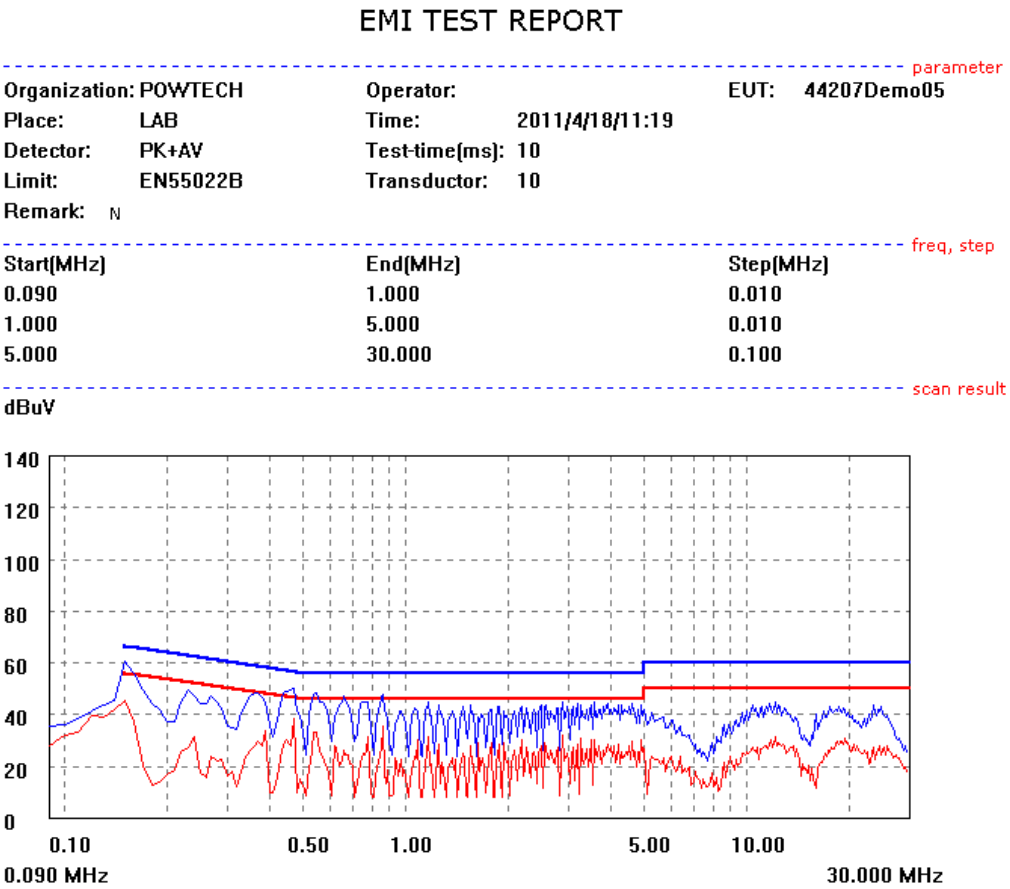
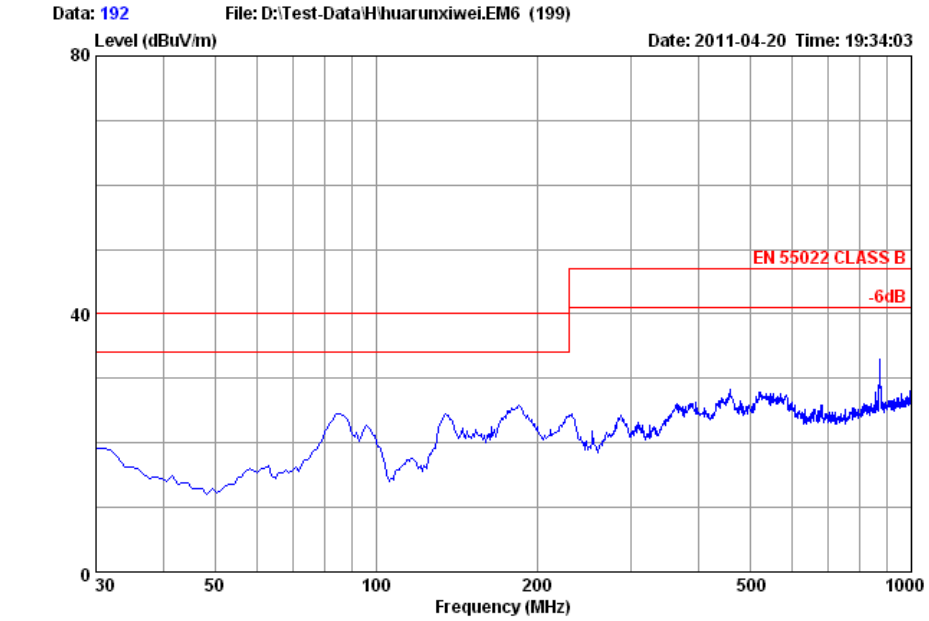


FIGURE 9 EMI CURVE—N

8.10 Radiated EMI

Test Condition: Vin=230VAC, Driving 12 strings of 24pcs LED in series

Audix Technology (Shanghai) Co., Ltd.
3F #34Bldg. No.680 GuiPing Rd.,
CaoHeJing Hi-Tech Park,
Shanghai 200233, China
Tel:+86-21-64955500 Fax:+86-21-64955491
audixaci@audix.com



Site : Audix(Shanghai) Chamber3
Condition : EN 55022 CLASS B HORIZONTAL
Project No. :
Applicant :
EUT :
M/N : 4207-1
S/N :
Power Supply : 230V/50Hz
Ambient : 25'C 55%
Test Mode :
Test Engineer: Raven
Memo :

FIGURE 10 RADIATION HORIZONTAL CURVE

AUDIX®
Audix Technology (Shanghai) Co., Ltd.
3F #34Bldg. No.680 GuiPing Rd.,
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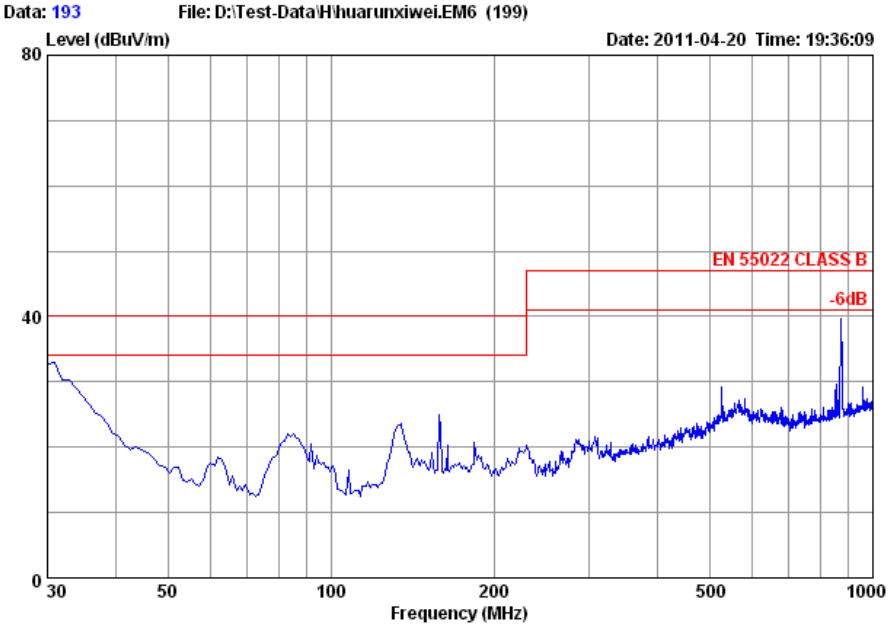
Shanghai 200233, China
Tel:+86-21-64955500 Fax:+86-21-64955491
audixaci@audix.com



Site : Audix(Shanghai) Chamber3
Condition : EN 55022 CLASS B VERTICAL
Project No. :
Applicant :
EUT :
M/N : 4207-1
S/N :
Power Supply : 230V/50Hz
Ambient : 25'C 55%
Test Mode :
Test Engineer: Raven
Memo :

	Freq	Level	ReadAntenna Level	Factor	Cable Loss	Limit Line	Over Limit	Remark
	MHz	dBuV/m	dBuV	dB/m	dB	dBuV/m	dB	
1	30.07	31.74	12.70	18.24	0.80	40.00	-8.26	QP

FIGURE 11 RADIATION HORIZONTAL CURVE

9 KEY DESIGN POINTS

9.1 Efficiency and PF

Resistor R3 can be changed from 100R to 300R to achieve a little higher power factor If lower average efficiency is acceptable (Lower 1% to 2%).

9.2 Spec of C4

Capacitor C4 should be chosen as a low ESR, X7R type ceramic capacitor to offer a high frequency path to lower the output current ripple.

9.3 Tolerance of Resistors

Use 1% tolerance resistors R8/R9/R10 for better output current accuracy.

9.4 Lifetime

It is better to use 105℃ E-capacitors for C1/C2 and 130℃ cure temperature of ferrite core to achieve longer lifetime.

9.5 PCB Layout

Place the BYPASS capacitors C5/C6/C7 and the off-time setting resistor R8 as close as possible to the pins of PT4207 on the PCB. Make sure that pin3 of PT4207, ground pad of C6 and C7 are connected together at the same location on the PCB and away from the area of the switching ground.
Minimize output loop areas (See Figure 12) to reduce EMI.

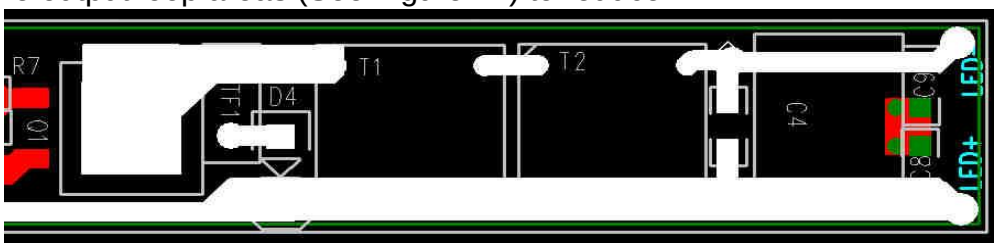


FIGURE 12 OUTPUT LOOP AREAS

U1 should be away from switching loop and the large current paths to minimize noise coupling. See Figure 13.

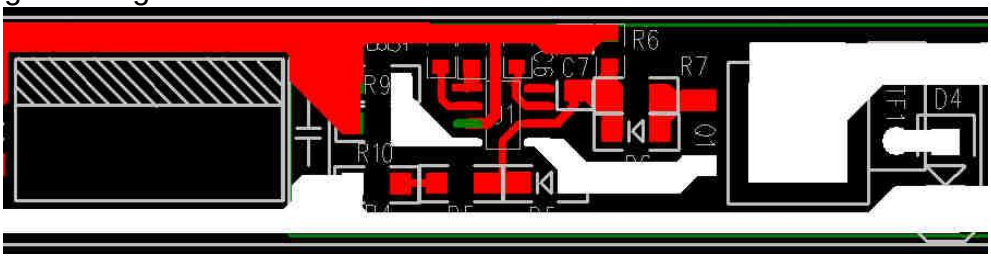


FIGURE 13 U1 PLACING

10 REVISION HISTORY

Date	Author	Revision	Description & changes
2011.6.3	Ou Xuanhong	Ver1.0	Initial Release
2011.9.1	Jin Gaoxian	Ver1.1	Updated performance Evaluation