PT5304

1.25W Mono Full Differential Audio Power Amplifier

GENERAL DESCRIPTION

The PT5304 is a fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.25W of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a 5V power supply.

The PT5304 is designed specifically to provide high quality output power with a minimal amount of external components. The PT5304 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The PT5304 contains advanced pop & click circuitry which virtually eliminates noises which would otherwise occur during turn-on and turn-off transitions.

FEATURES

- 1.25W Into 8Ω Form a 5V Supply at THD=1% (Typ.)
- Low Supply Current: 2.7mA@VDD=5V
- Shutdown Current < 1uA
- Improved PSRR at 217Hz: 80dB (Typ.)
- Fully Differential Design Reduces RF Rectification
- Improved CMRR Eliminates Two Input Coupling Capacitors
- C_{bypass} is Optional Due to Fully Differential Design and High PSRR
- MSOP-8 and DFN-8 packages are available

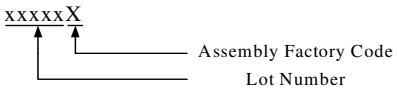
APPLICATION

- Mobile Phones
- PDAs
- Portable electronic devices

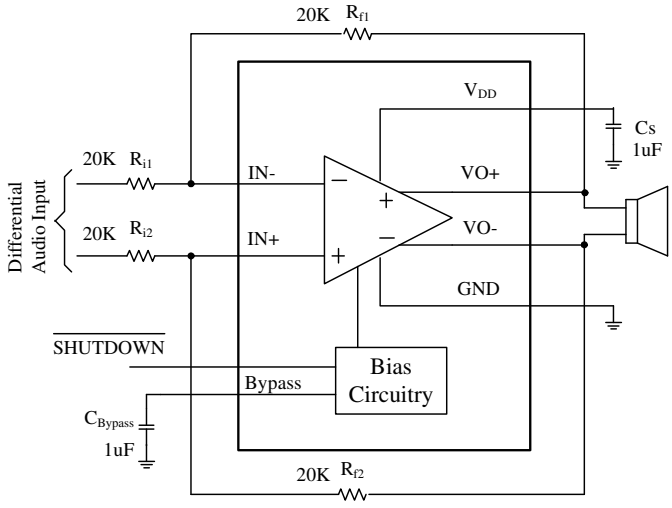
ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART	TRANSPORT MEDIA	MARKING
MSOP-8	-40 °C to 85 °C	PT5304EMSH	Tape and Reel 3000 units	PT5304 xxxxxX
DFN-8	-40 °C to 85 °C	PT5304EQFN	Tape and Reel 5000 units	PT5304 xxxxxX

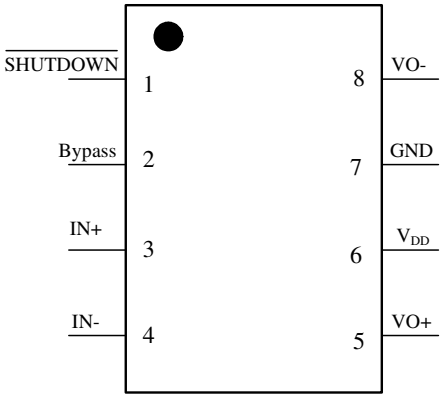
Note:



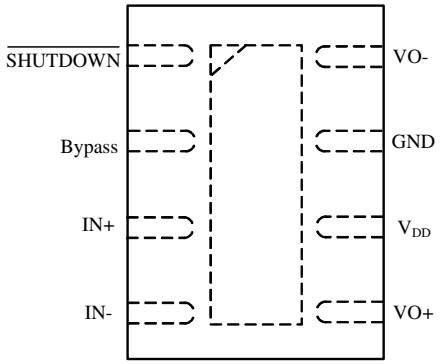
TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT



MSOP-8



DFN-8

PIN DESCRIPTIONS

MSOP8/DFN-8 PIN No.	PIN NAMES	DESCRIPTION
1	$\overline{\text{SHUTDOWN}}$	Shutdown terminal
2	Bypass	Mid-supply voltage. connect a capacitor to GND for Bypass voltage filtering. Bypass capacitor is optional.
3	IN+	Positive differential input
4	IN-	Negative differential input
5	VO+	Positive BTL output
6	V_{DD}	Supply voltage terminal
7	GND	Ground
8	VO-	Negative BTL output

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	ITEMS	VALUE	UNIT
V_{DD}	Supply Voltage	-0.3~6	V
V_{IN}	Input Voltage	-0.3~ V_{DD}+0.3	V
P_{DMAX}	Power Dissipation (Note 2)	Internally Limited	W
P_{TR1}	Thermal Resistance, MSOP-8 θ_{JA}	190	°C /W
P_{TR2}	Thermal Resistance, DFN-8 θ_{JA}	63	°C /W
T_J	Operation Junction Temperature Range	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	°C
	ESD Susceptibility (Note 3)	2	kV

RECOMMENDED OPERATING RANGE

SYMBOL	ITEMS	VALUE	UNIT
V_{DD}	V_{DD} Supply Voltage	+2.5 ~ +5.5	V
V_{IC}	Common-mode input voltage	0.5 ~ V_{DD}-0.8	V
T_{OPT}	Operating Temperature	-40 to +85	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS (VDD=5V) (Note 4, 5)

The following specifications apply for V_{DD}=5V, 8Ω load, and A_{DV}=1V/V, T_A=25 °C, unless specified otherwise.

SYMBOL	ITEMS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load		3	6	mA
		V_{IN} = 0V, R_L=8Ω		5	10	
I_{SD}	Shutdown Current	SHUTDOWN = GND		0.1	1	uA
P_O	Output Power	THD=1%, f=1k Hz, R_L=8Ω		1.25		W
THD+N	Total Harmonic Distortion+Noise	P_O=0.4W, f=1k Hz		0.05		%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine p-p, V_{IN}=0V				
		f = 217 Hz		80		dB
		f = 1k Hz		80		dB
CMRR	Common mode Rejection Ratio	f = 217 Hz, V_{IC} =0.5~V_{DD}-0.8		80		dB
V_{OS}	Output Offset	V_{IN}=0V		2		mV
V_{SDH}	Shutdown Voltage Input High		1.4			V
V_{SDL}	Shutdown Voltage Input Low				1.0	V

ELECTRICAL CHARACTERISTICS (V_{DD}=3V) (Note 4, 5)

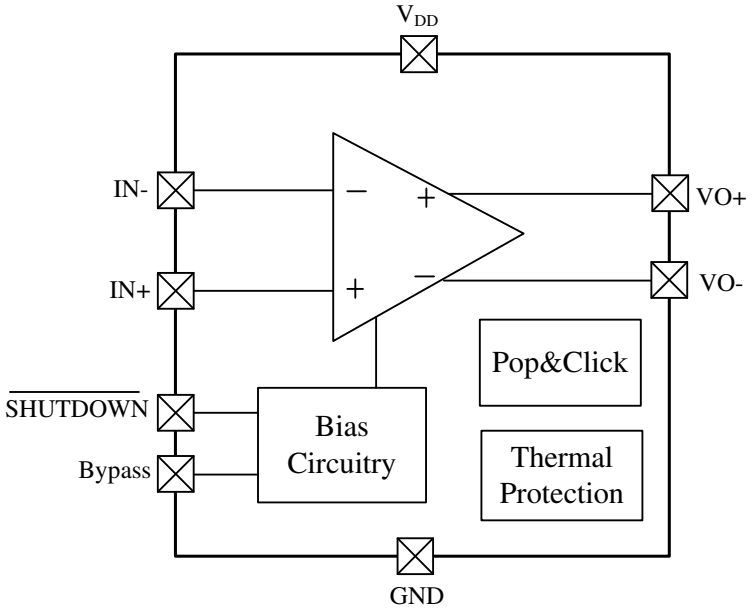
The following specifications apply for V_{DD}=3V, 8Ω load, and A_{DV}=1V/V, T_A=25 °C, unless specified otherwise.

SYMBOL	ITEMS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load		2.5	5.5	mA
		V_{IN} = 0V, R_L=8Ω		4	9	
I_{SD}	Shutdown Current	SHUTDOWN = GND		0.1	1	uA
P_O	Output Power	THD=1%, f=1k Hz, R_L=8Ω		0.35		W
THD+N	Total Harmonic Distortion+Noise	P_O=0.25W, f=1k Hz		0.03		%
PSRR	Power Supply Rejection Ratio	V_{ripple}=200mV sine p-p, V_{IN}=0V				
		f = 217 Hz		80		dB
		f = 1k Hz		75		dB
CMRR	Common mode Rejection Ratio	f = 217 Hz, V_{IC} =0.5~V_{DD}-0.8		80		dB
V_{OS}	Output Offset	V_{IN}=0V		2		mV
V_{SDH}	Shutdown Voltage Input High		0.9			
V_{SDL}	Shutdown Voltage Input Low				0.7	

Note 4: Typicals are measured at 25˚C and represent the parametric norm.

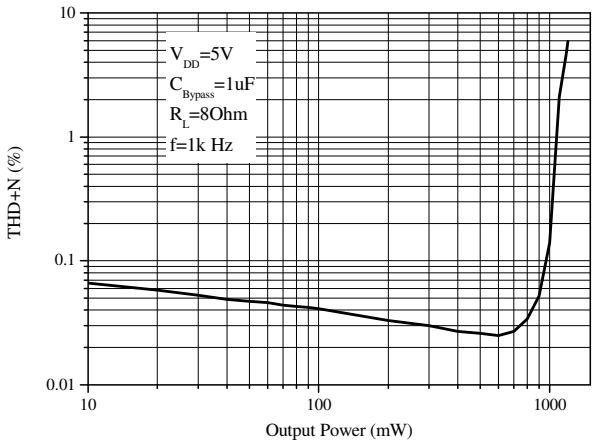
Note 5: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

SIMPLIFIED BLOCK DIAGRAM

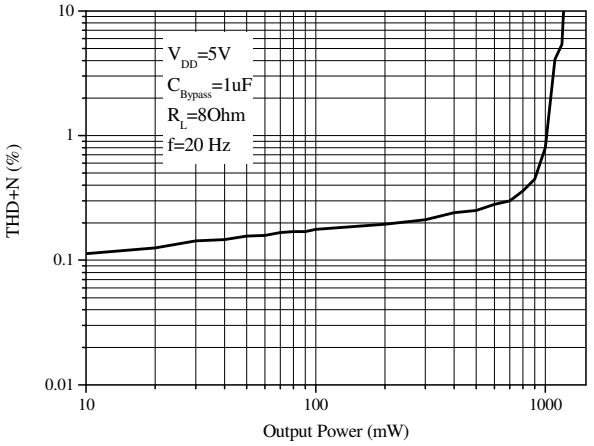


TYPICAL PERFORMANCE CHARACTERISTICS

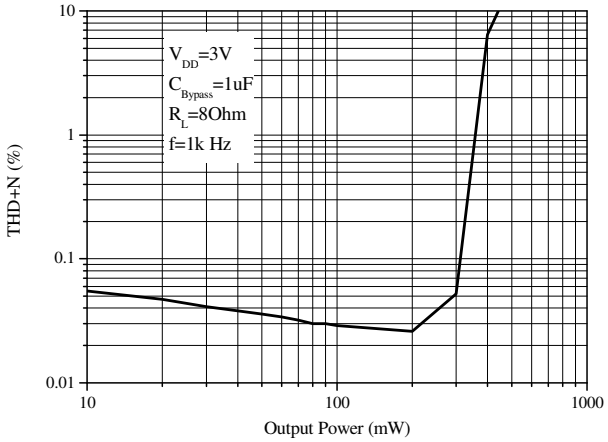
Total Harmonic Distortion+Noise vs. Ouput Power



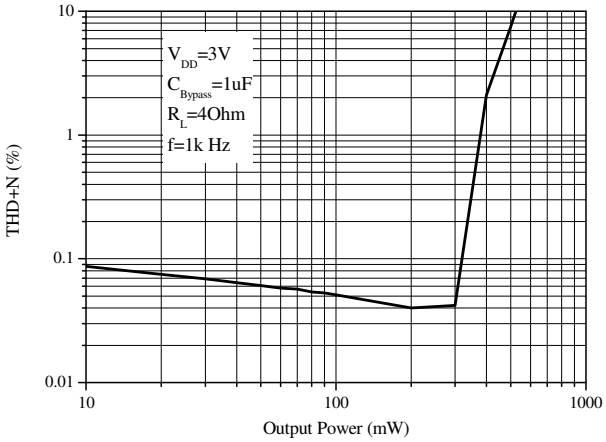
Total Harmonic Distortion+Noise vs. Ouput Power



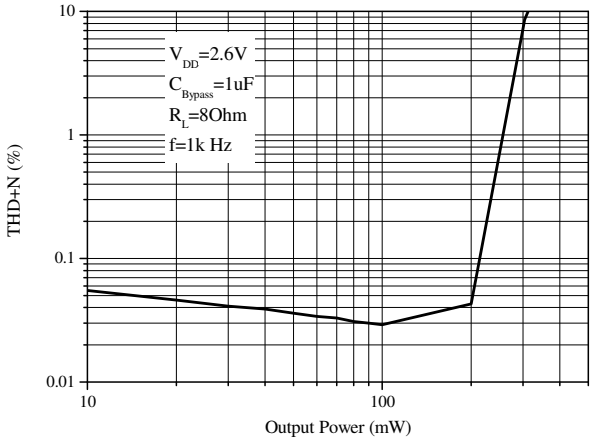
Total Harmonic Distortion+Noise vs. Ouput Power



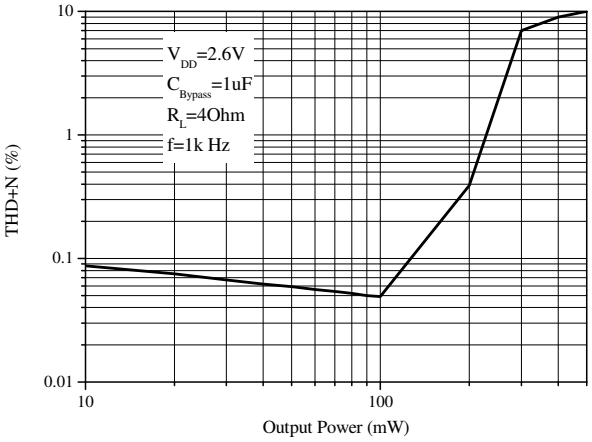
Total Harmonic Distortion+Noise vs. Ouput Power



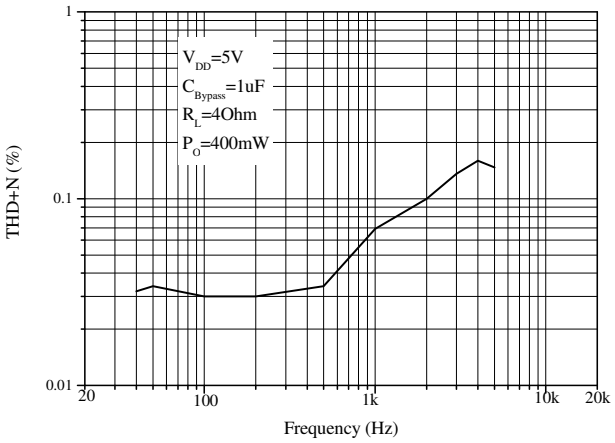
Total Harmonic Distortion+Noise vs. Ouput Power



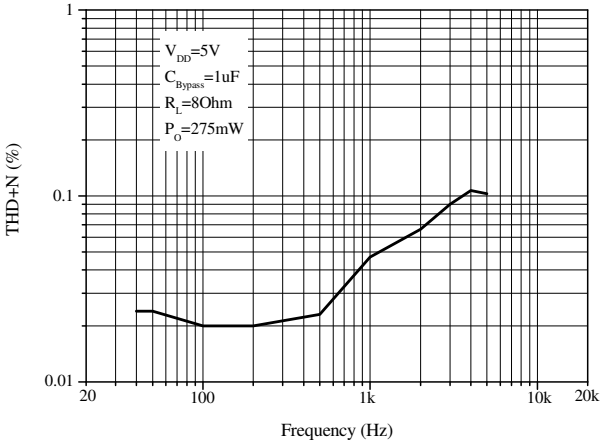
Total Harmonic Distortion+Noise vs. Ouput Power



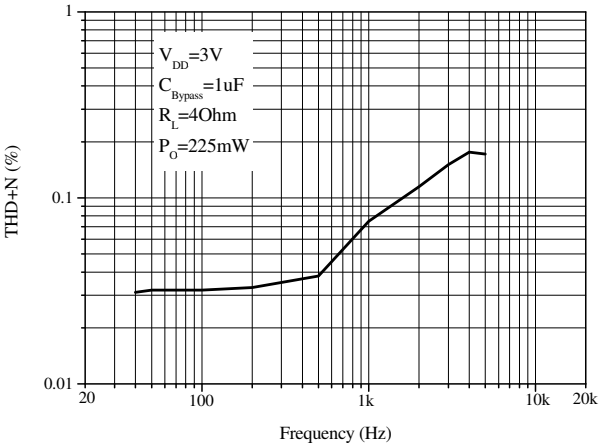
Total Harmonic Distortion + Noise vs. Frequency



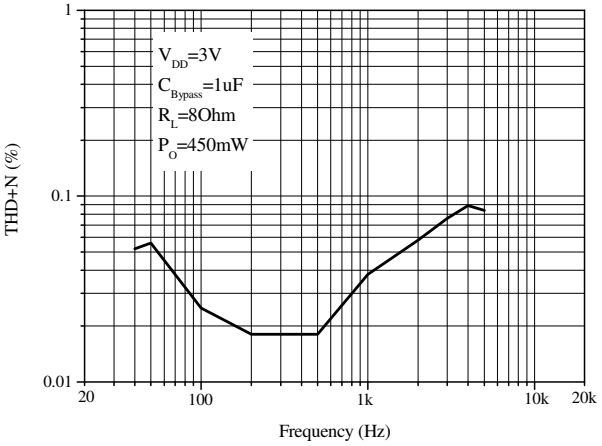
Total Harmonic Distortion+Noise vs. Frequency



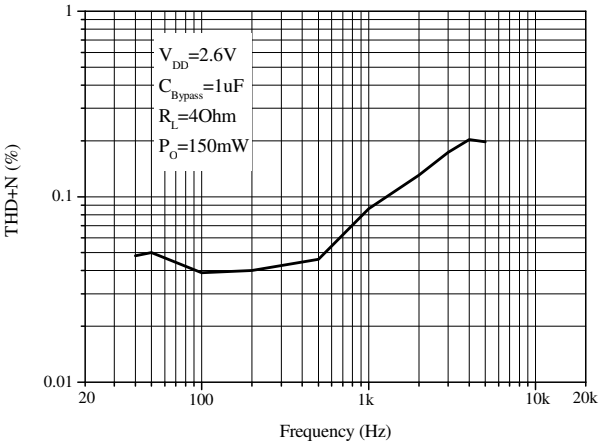
Total Harmonic Distortion+Noise vs. Frequency



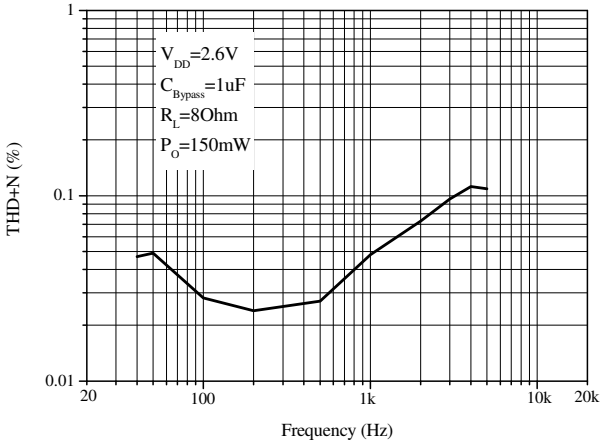
Total Harmonic Distortion+Noise vs. Frequency



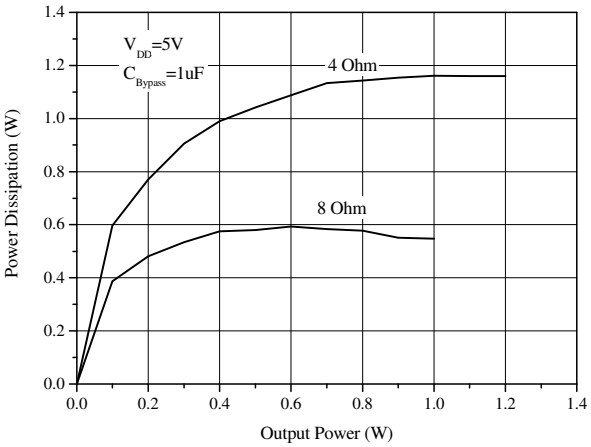
Total Harmonic Distortion+Noise vs. Frequency



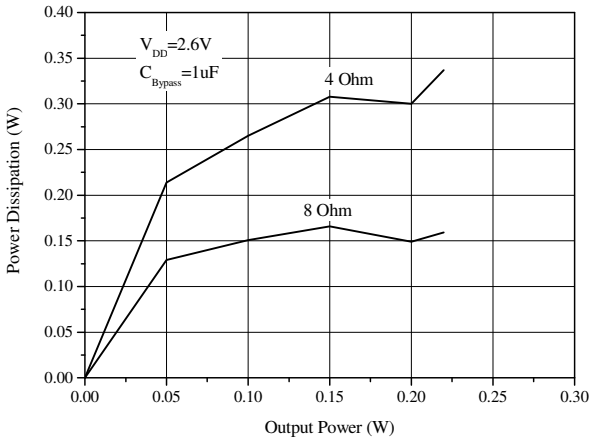
Total Harmonic Distortion+Noise vs. Frequency



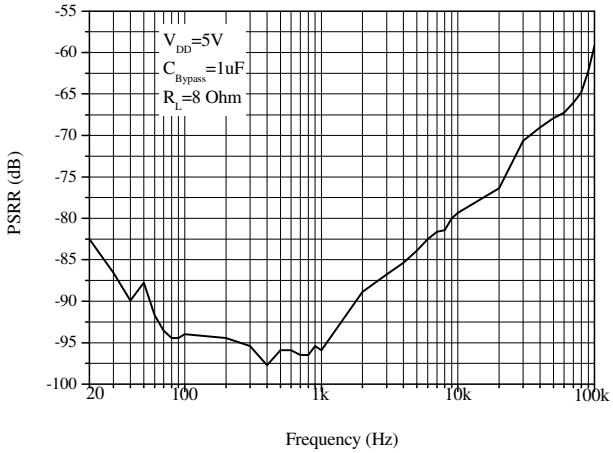
Power Dissipation vs. Output Power



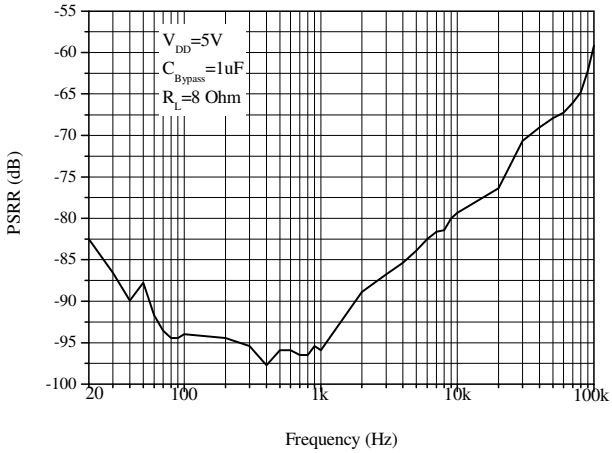
Power Dissipation vs. Output Power



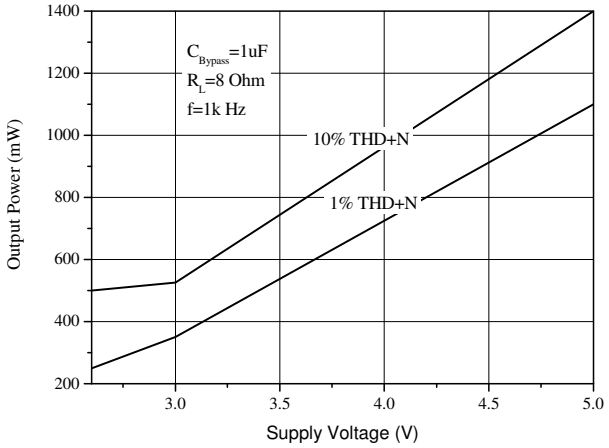
Power Supply Ripple Rejection vs. Frequency



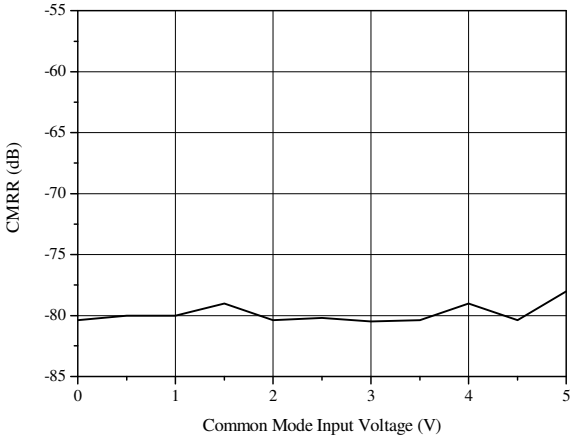
Power Supply Ripple Rejection vs. Frequency



Output Power vs. Supply Voltage



Common Mode Rejection Ratio vs. Common Mode Input Voltage



APPLICATION INFORMATION

DIFFERENTIAL AMPLIFIER EXPLANATION

The PT5304 is a fully differential audio amplifier that features differential input and output stages. Internally this is accomplished by two circuits: a differential amplifier and a common mode feedback amplifier that adjusts the output voltages so that the average value remains $V_{DD}/2$. When setting the differential gain, the amplifier can be considered to have two "halves". Each half uses an input and feedback resistor (R_i and R_f) to set its respective closed-loop gain. With $R_{i1} = R_{i2}$ and $R_{f1} = R_{f2}$, the gain is set at $-R_f/R_i$ for each half. This results in a differential gain of $A_{VD} = -R_f/R_i$.

It is extremely important to match the input resistors to each other, as well as the feedback resistors to each other for best amplifier performance. See the Proper Selection of External Components section for more information. A differential amplifier works in a manner where the difference between the two input signals is amplified. In most applications, this would require input signals that are 180^O out of phase with each other. The PT5304 can be used, however, as a single ended input amplifier while still retaining its fully differential benefits. In fact, completely unrelated signals may be placed on the input pins. The PT5304 simply amplifies the difference between them.

All of these applications, either single-ended or fully differential, provide what is known as a "bridged mode" output (BTL). This results in output signals at VO+ and VO- that are 180^O out of phase with respect to each other. Bridged mode operation is different from the single-ended amplifier configuration that connects the load between the amplifier output and ground. A bridged amplifier design has distinct advantages over the single-ended configuration: it provides differential drive to the load, thus doubling maximum possible output swing for a specific supply voltage. Four times the output power is possible compared with a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excess clipping, please refer to the Audio Power Amplifier Design section.

A bridged configuration, such as the one used in the PT5304, also creates a second advantage over single-ended amplifiers. Since the differential outputs, VO+ and VO-, are biased at half-supply, no net DC voltage exists across the load. This assumes that the input resistor pair and the feedback resistor pair are properly matched (see Proper Selection of External Components). BTL configuration eliminates the output coupling capacitor required in single supply, single-ended amplifier configurations. If an output coupling capacitor is not used in a single-ended output configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage. Further advantages of bridged mode operation specific to fully differential amplifiers like the PT5304 include increased power supply rejection ratio, common-mode noise reduction, and click and pop reduction.

APPLICATION SCHEMATICS

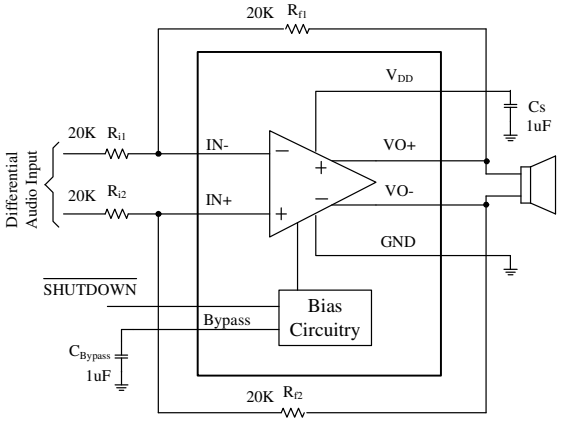


Figure 1. Typical Differential Input Application Schematic

APPLICATION SCHEMATICS

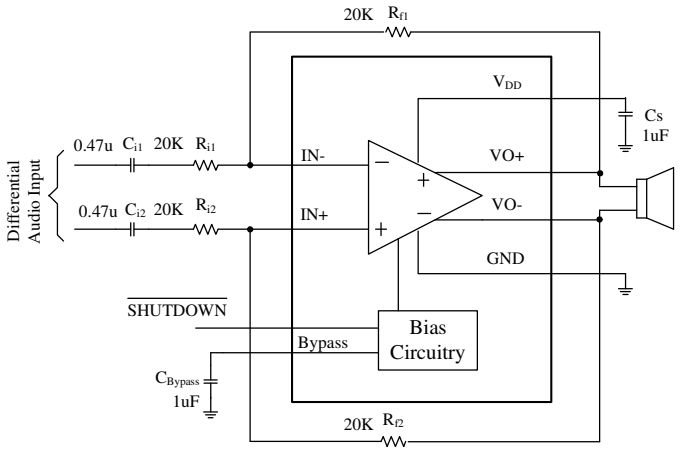


Figure 2. Typical Differential Input Application Schematic with Optimized Input Capacitors

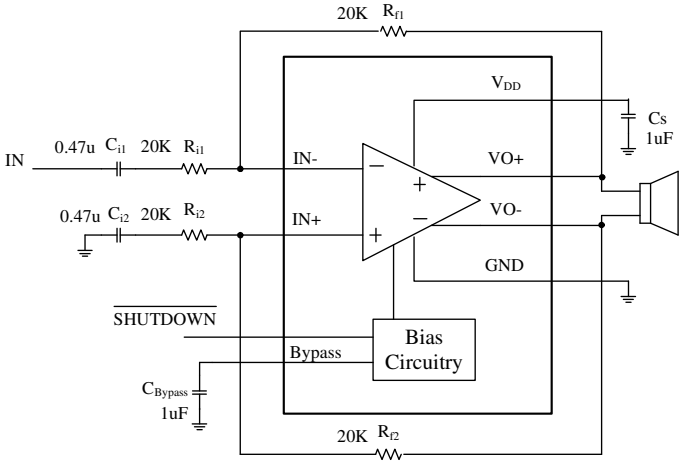


Figure 3. Single-End Input Application Schematic

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect resistance (PCB trace and wire) between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4 load from 1.4W to1.37W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \qquad (1)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation versus a single-ended amplifier operating at the same conditions.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \text{ Bridge Mode} \qquad (2)$$

Since the PT5304 has bridged outputs, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the PT5304 does not require additional heatsinking under most operating conditions and output loading. From Equation 2, assuming a 5V power supply and an 8Ω load, the

maximum power dissipation point is 625mW. The maximum power dissipation point obtained from Equation 2 must not be greater than the power dissipation results from Equation 3:

$P_{DMAX} = (T_{JMAX}-T_A)/\theta_{JA}$ (3)

Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased, the ambient temperature reduced, or the θ_{JA} reduced with heatsinking. In many cases, larger traces near the output, V_{DD} and GND pins can be used to lower the θ_{JA}. The larger areas of copper provide a form of heatsinking the allowing higher power dissipation. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 30˚C provided that device operation is around the maximum power dissipation point. Recall that internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the PT5304 can operate at higher ambient temperatures. Refer to the Typical Performance Characteristics curves for power dissipation information.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection ratio (PSRR). The capacitor location on both the bypass and power supply pins should be as close to the device as possible. A larger half-supply bypass capacitor improves PSRR because it increases half-supply stability. Typical applications employ a 5V regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. This, however, does not eliminate the need for bypassing the supply nodes of the PT5304. Although the PT5304 will operate without the bypass capacitor C_{Bypass}, the PSRR may decrease. A 1µF capacitor is recommended for C_{Bypass}. This value maximizes PSRR performance. Lesser values may be used, but PSRR decreases at frequencies below 1k Hz. The issue of C_{Bypass} selection is thus dependant upon desired PSRR and click and pop performance as explained in the section Proper Selection of External Components.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical when optimizing device and system performance. Although the PT5304 is tolerant to a variety of external component combinations, consideration of component values must be made when maximizing overall system quality.

The PT5304 is unity-gain stable, giving the designer maximum system flexibility. The PT5304 should be used in low closed-loop gain configurations to minimize THD+N values and maximize signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the Audio Power Amplifier Design section for a more complete explanation of proper gain selection. When used in its typical application as a fully differential power amplifier the PT5304 does not require input coupling capacitors for input sources with DC common-mode voltages of less than V_{DD}.

Special care must be taken to match the values of the feedback resistors (R_{f1} and R_{f2}) to each other as well as matching the input resistors (R_{i1} and R_{i2}) to each other. Because of the balanced nature of differential amplifiers, resistor matching differences can result in net DC currents across the load. This DC current can increase power consumption, internal IC power dissipation, reduce PSRR, and possibly damaging the loudspeaker. The chart below demonstrates this problem by showing the effects of differing values between the feedback resistors while assuming that the input resistors are perfectly matched. The results below apply to the application circuit shown in Figure 1, and assumes that V_{DD}=5V, R_L=8Ω, and the system has DC coupled inputs tied to ground.

TOLERANCE	R_{f1}	R_{f2}	VO+-VO-	I_{Load}
20%	0.8R	1.2R	-0.5V	62.5mA
10%	0.9R	1.1R	-0.250V	31.25mA
5%	0.95R	1.05R	-0.125V	15.63mA
1%	0.99R	1.01R	-0.025V	3.125mA
0	R	R	0	0

Similar results would occur if the input resistors were not carefully matched. Adding input coupling capacitors in between the signal source and the input resistors will eliminate this problem, however, to achieve best performance with minimum component count it is highly recommended that both the feedback and input resistors matched to 1% tolerance or better.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W/8Ω Audio Amplifier

Given:

- Power Output 1W
- Load Impedance 8Ω
- Input Level 1Vrms
- Input Impedance 20k
- Bandwidth 100Hz~20kHz±0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. The supply rail can easily be found by extrapolating from the Output Power vs. Supply Voltage graphs in the Typical Performance Characteristics section. Using the Output Power vs. Supply Voltage graph for an 8Ω load, the minimum supply rail just about 5V. Extra supply voltage creates headroom that allows the PT5304 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section. Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{VD} \geq \sqrt{(R_L P_o)} / (V_{IN}) = V_{orms} / V_{inrms} \qquad (4)$$

$R_f / R_i = A_{VD}$

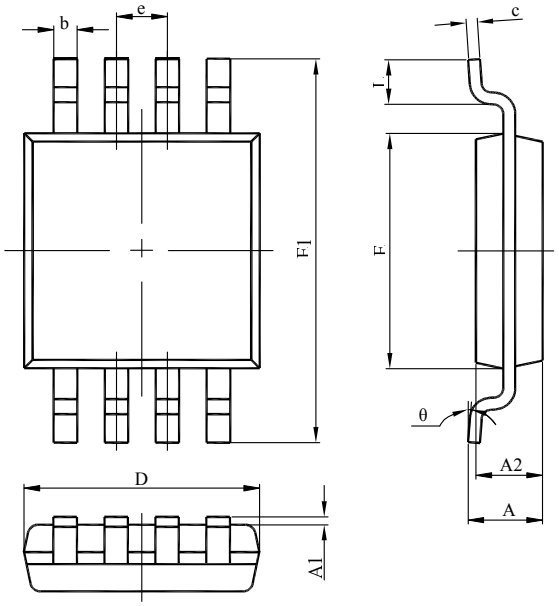
From Equation 8, the minimum A_{VD} is 2.83. Since the desired input impedance was 20kΩ, a ratio of 2.83:1 of R_f to R_i results in an allocation of R_i= 20kΩ for both input resistors and R_f = 60kΩ for both feedback resistors. The final design step is to address the bandwidth requirement which must be stated as a single -3dB frequency point. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_H = 20kHz*5 = 100kHz

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}.With a A_{VD} = 2.83 and f_H, = 100k Hz, the resulting GBWP = 150k Hz which is much smaller than the PT5304 GBWP of 10MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the PT5304 can still be used without running into bandwidth limitations.

PACKAGE INFORMATION

MSOP-8 Package



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

PACKAGE INFORMATION

DFN-8 Package