PT5321

Dual 2.1W Audio Amplifier
Plus Stereo Headphone Function & 3D Enhancement

GENERAL DESCRIPTION

The PT5321 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.1W to a 4Ω load or 2.4W to a 3Ω load with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

The PT5321 has two separate HP (headphone) enable inputs, each having different logic level thresholds. Either HP enable input activates the single ended headphone mode and disables the BTL output mode. The HP Sense input is for use with a normal stereo headphone jack. The remaining input, HP Logic, accepts standard logic level thresholds. The PT5321 provides a user selectable 3D Enhancement mode to enhance stereo imaging. The PT5321 features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce "pop and click" during device turn-on.

FEATURES

- P_O@1% THD+N:
  3Ω, 4Ω loads: 2.4W (typ), 2.1W (typ)
  8Ω load: 1.3W (typ)
- Single-ended mode THD+N@75mW into 32Ω: 0.01% (typ)
- Shutdown current: 0.04μA (typ)
- Supply voltage range: 2.5V to 5.5V
- PSRR@217Hz: 88dB (typ)
- Selectable headphone enable modes
- 3D Enhancement
- Stereo headphone amplifier mode
- "Click and pop" suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- PCB area-saving QFN-24 package

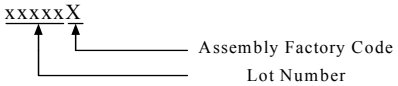
APPLICATIONS

- Cell phones
- Multimedia monitors
- Portable and desktop computers
- Portable audio systems

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
QFN-24	-40 °C to +85 °C	PT5321EQFN	Tape and Reel 5000 units	PT5321 xxxxxX
QFN-24	-40 °C to +85 °C	PT5321EQFN	Tape and Reel 5000 units	PT5321 xxxxxX

Note:



TYPICAL APPLICATION CIRCUIT

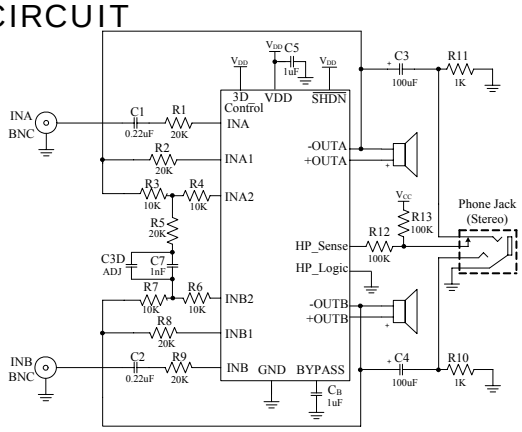
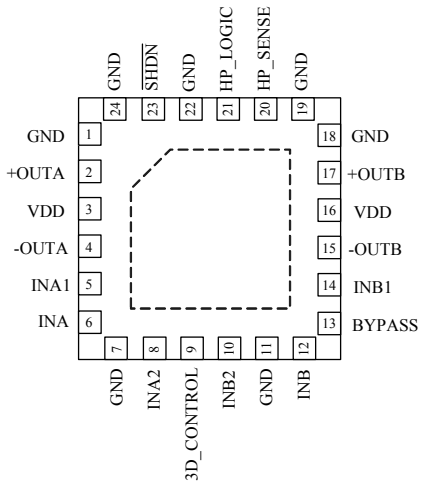


Figure 1. Typical Audio Amplifier Application

PIN ASSIGNMENT



QFN-24 (4x4)

PIN DESCRIPTIONS

QFN-24 PIN NO.	PIN NAMES	DESCRIPTION
1,7,11,18,19 ,22,24	GND	Ground
2	+OUTA	The non-inverting output of channel-A
3,16	VDD	Power Supply
4	-OUTA	The inverting output of channel-A
5	INA1	The 1st input of channel-A
6	INA	The input of channel-A
8	INA2	The 2nd input of channel-A
9	3D_CONTROL	Enable the 3D enhancement when held high
10	INB2	The 2nd input of channel-B
12	INB	The input of channel-B
13	BYPASS	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1uF to 1uF low ESR capacitor for best performance.
14	INB1	The 1st input of channel-B
15	-OUTB	The inverting output of channel-B
17	+OUTB	The non-inverting output of channel-B
20	HP_SENSE	The HP_SENSE input is for use with a normal stereo headphone jack to select the operational output mode.
21	HP_LOGIC	Control the choice of BTL or SE mode. When HP_LOGIC is high, PT5321 operates in SE mode.
22	$\overline{\text{SHDN}}$	Puts the device in shutdown mode when held low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	ITEMS		VALUE	UNIT
V_{DD}	Supply Voltage		6.0	V
T_{STG}	Storage Temperature		-65 ~ +150	°C
V_{INPUT}	Input Voltage		-0.3 ~ V_{DD}+0.3	V
P_{MAX}	Power Dissipation (Note 2)		Internally Limited	W
	ESD Susceptibility (Note 3)		2	KV
T_J	Junction Temperature		150	°C
T_{Solder}	Solder Temperature		160 °C, 10 sec.	
θ_{JA}	Thermal Resistance	QFN-24	42	°C/W

RECOMMENDED OPERATING RANGE

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage	+2.5 ~ +5.5	V
T_{OPT}	Operational Temperature	-40 ~ +85	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Range indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS (V_{DD}=5V) (Note 4, 5, 9)

The following specifications apply for V_{DD}=5V, T_A=25 °C, unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		2.5		5.5	V
I_{DD}	Quiescent Power Supply Current (Note 6)	V_{IN}=0, I_O=0A, BTL mode V_{IN}=0, I_O=0A, SE mode		5.2 2.6	8 4.5	mA
I_{SD}	Shutdown Current	$V_{\overline{SHDN}}$=0		0.04	2	uA
V_{IH}	Headphone Sense High Input Voltage		4	3.7		V
V_{IL}	Headphone Sense Low Input Voltage			2.6	0.8	V
V_{IHSD}	Shutdown, Headphone micro, 3D control High Input Voltage		1.4	1.2		V
V_{ILSD}	Shutdown, Headphone micro, 3D control Low Input Voltage			1	0.4	V
T_{WU}	Turn On Time	1uF Bypass Cap		202		ms

Electrical Characteristics for BTL mode operation (V_{DD}=5V) (Note 4, 5, 9)

The following specifications apply for V_{DD}=5V, T_A=25 °C, unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OS}	Output Offset Voltage	V_{IN}=0V		5	25	mV
P_O	Output Power (Note 7) (Note 8)	THD+N=1%, f=1KHz				W
		R_L=3Ω		2.4		
		R_L=4Ω		2.1		
		R_L=8Ω	1.0	1.3		
		THD+N=10%, f=1KHz				
		R_L=3Ω		3.0		
		R_L=4Ω		2.5		
		R_L=8Ω		1.7		
THD+N	Total Harmonic Distortion + Noise	1KHz, A_{VD}=2				%
		R_L=4Ω, P_O=1W		0.05		
		R_L=8Ω, P_O=1W		0.03		
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		88		dB
		Input Unterminated, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		80		dB
		Input grounded, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		81		dB
		Input grounded, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		75		dB
X_{TALK}	Channel Separation	f=1KHz, C_B=1uF, 3D_Control = Low		103		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		11		uV

Electrical Characteristics for Single-Ended mode operation (V_{DD}=5V)

(Note 4, 5, 9)

The following specifications apply for V_{DD}=5V, T_A=25 °C, unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	Output Power (Note 7)	THD+N=0.05%, f=1KHz, R_L=32Ω	75	90		mW
THD+N	Total Harmonic Distortion + Noise	1KHz, R_L=32Ω, P_O=20mW		0.012		%
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		84		dB
		Input Unterminated, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		85		dB
		Input grounded, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		81		dB
		Input grounded, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		86		dB
X_{TALK}	Channel Separation	f=1KHz, C_B=1uF, 3D_Control = Low		100		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		5		uV

ELECTRICAL CHARACTERISTICS (V_{DD}=3V) (Note 4, 5, 9)

The following specifications apply for V_{DD}=3V, T_A=25 °C, unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	Quiescent Power Supply Current (Note 6)	V_{IN}=0, I_O=0A, BTL mode V_{IN}=0, I_O=0A, SE mode		5.0 2.4		mA
I_{SD}	Shutdown Current	$V_{\overline{SHDN}}$=0		0.01	2	uA
V_{IH}	Headphone Sense High Input Voltage			2.2		V
V_{IL}	Headphone Sense Low Input Voltage			1.5		V
V_{IHSD}	Shutdown, Headphone micro, 3D control High Input Voltage		1.4	1		V
V_{ILSD}	Shutdown, Headphone micro, 3D control Low Input Voltage			0.8	0.4	V
T_{WU}	Turn On Time	1uF Bypass Cap		198		ms

Electrical Characteristics for BTL mode operation (V_{DD}=3V) (Note 4, 5, 9)

The following specifications apply for V_{DD}=3V, T_A=25 °C, unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OS}	Output Offset Voltage	V_{IN}=0V		5		mV
P_O	Output Power (Note 7) (Note 8)	THD+N=1%, f=1KHz				W
		R_L=3Ω		0.82		
		R_L=4Ω		0.70		
		R_L=8Ω		0.43		
		THD+N=10%, f=1KHz				
		R_L=3Ω		1.0		
		R_L=4Ω		0.85		
		R_L=8Ω		0.53		
THD+N	Total Harmonic Distortion + Noise	1KHz				%
		R_L=4Ω, P_O=280mW		0.04		
		R_L=8Ω, P_O=200mW		0.03		
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		90		dB
		Input Unterminated, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		80		dB
		Input grounded, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		79		dB
		Input grounded, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=8Ω		75		dB
X_{TALK}	Channel Separation	f=1KHz, C_B=1uF, 3D_Control = Low		104		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		11		uV

Electrical Characteristics for Single-Ended mode operation (V_{DD}=3V)

(Note 4, 5, 9) The following specifications apply for V_{DD}=3V, T_A=25 °C, unless specified otherwise.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	Output Power (Note 7)	THD+N=0.05%, f=1KHz, R_L=32Ω		35		mW
THD+N	Total Harmonic Distortion + Noise	1KHz, R_L=32Ω, P_O=20mW		0.015		%
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		81		dB
		Input Unterminated, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		83		dB
		Input grounded, 217Hz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		81		dB
		Input grounded, 1KHz V_{ripple}=200mV_{p-p} C_B=1uF, R_L=32Ω		83		dB
X_{TALK}	Channel Separation	f=1KHz, C_B=1uF, 3D_Control = Low		100		dB
V_{NO}	Output Noise Voltage	1KHz, A-weighted		5		uV

Note 4: Typicals are measured at 25˚C and represent the parametric norm.

Note 5: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

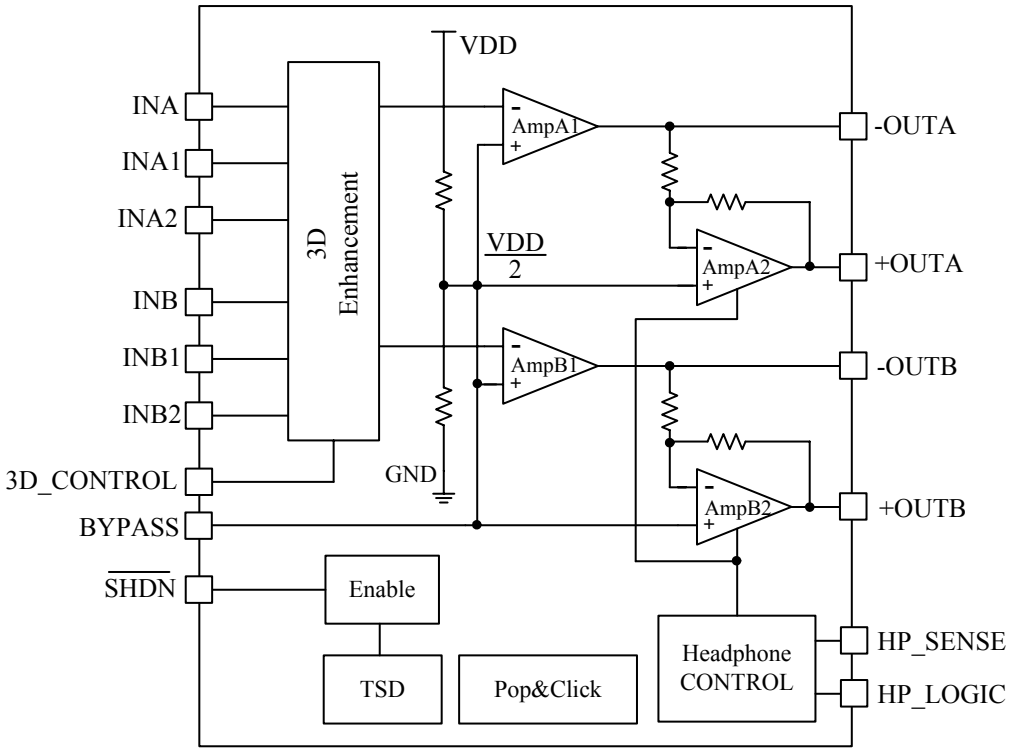
Note 6: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 7: Output power is measured at the device terminals.

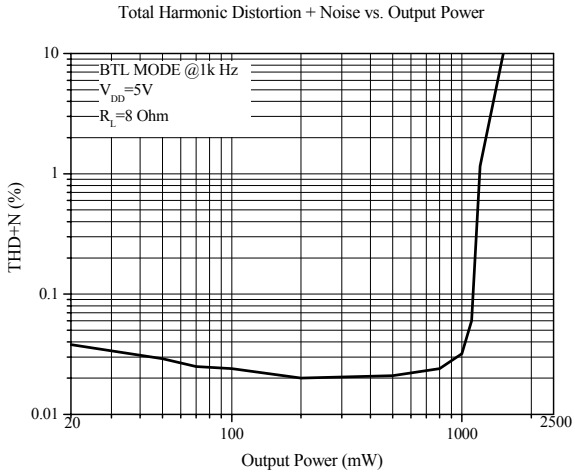
Note 8: When driving 3Ω or 4Ω loads and operating on a 5V supply, the PT5321EQFN must be mounted to a circuit board that has a minimum of 2.5in^2 of exposed, uninterrupted copper area connected to the QFN package's exposed-PAD.

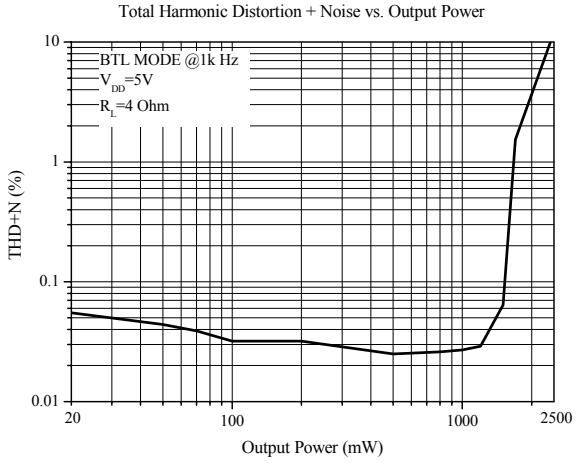
Note 9: All measurements taken from Applications Diagram (*Figure 1*).

SIMPLIFIED BLOCK DIAGRAM

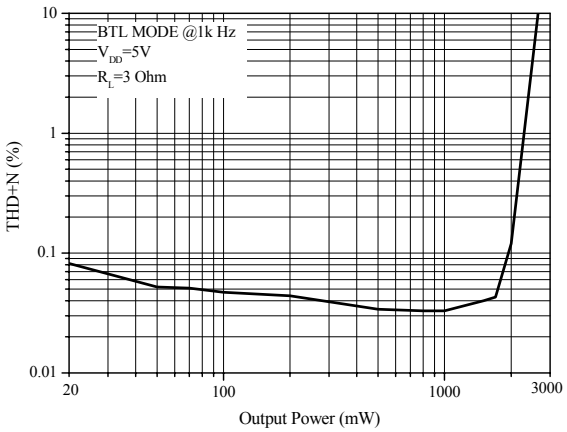


TYPICAL PERFORMANCE CHARACTERISTICS

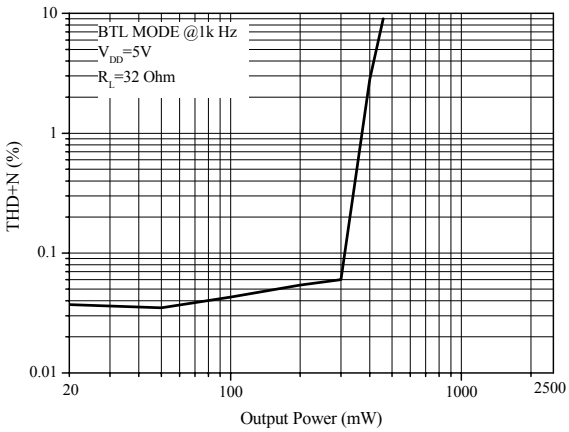




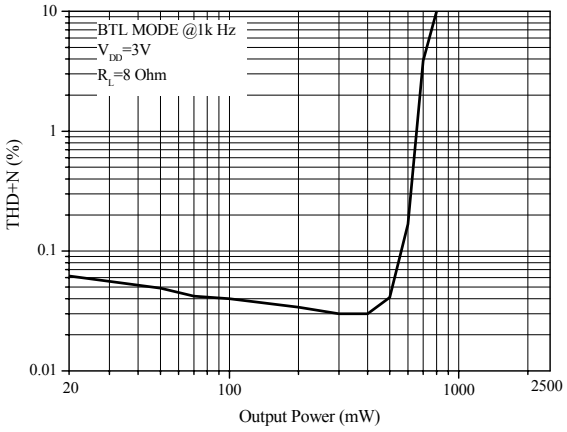
Total Harmonic Distortion + Noise vs. Output Power



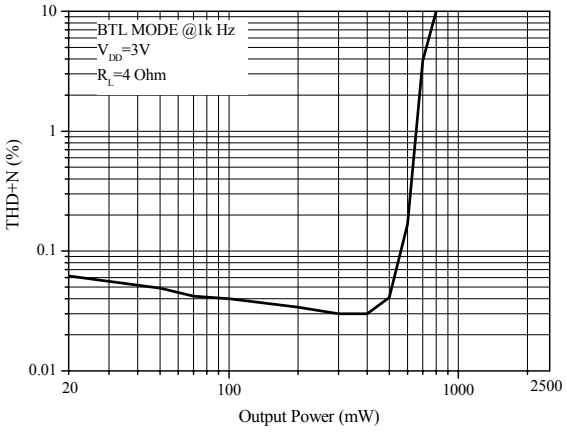
Total Harmonic Distortion + Noise vs. Output Power



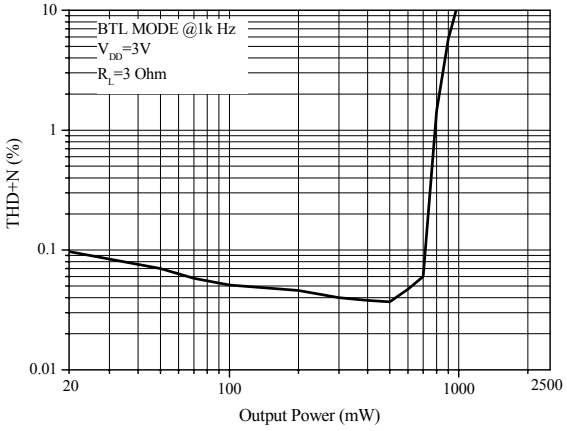
Total Harmonic Distortion + Noise vs. Output Power



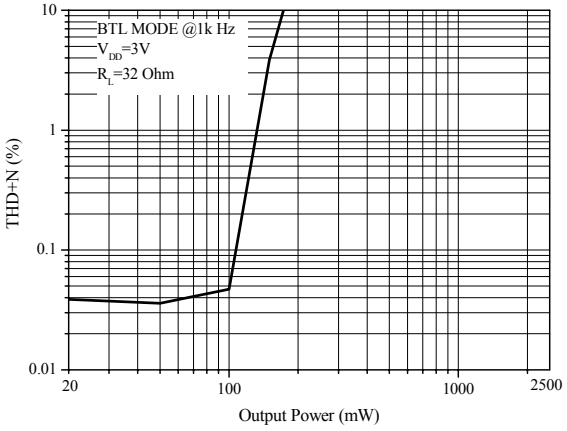
Total Harmonic Distortion + Noise vs. Output Power



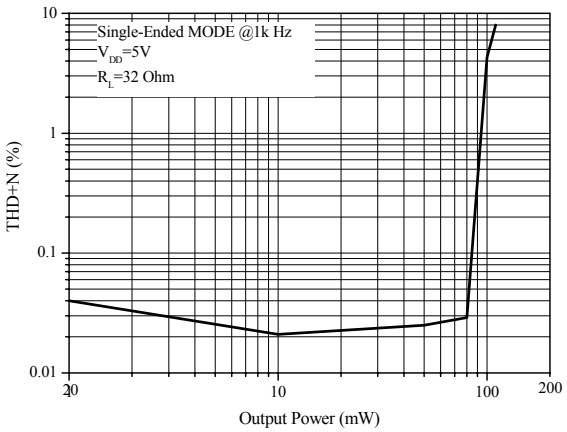
Total Harmonic Distortion + Noise vs. Output Power



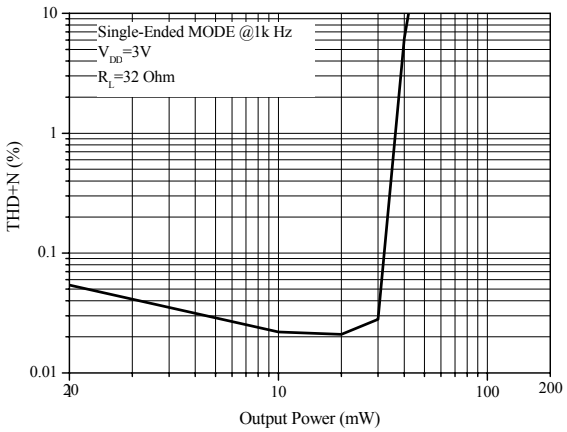
Total Harmonic Distortion + Noise vs. Output Power



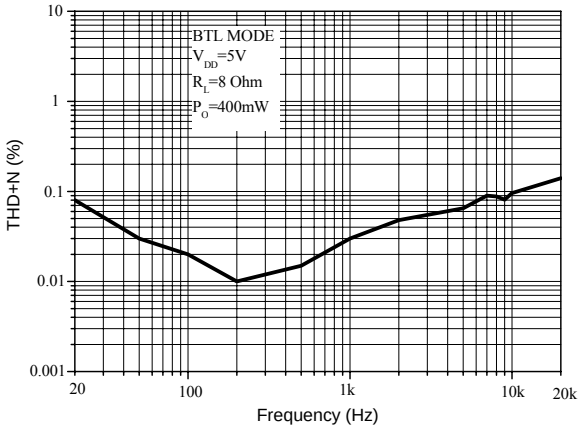
Total Harmonic Distortion + Noise vs. Output Power



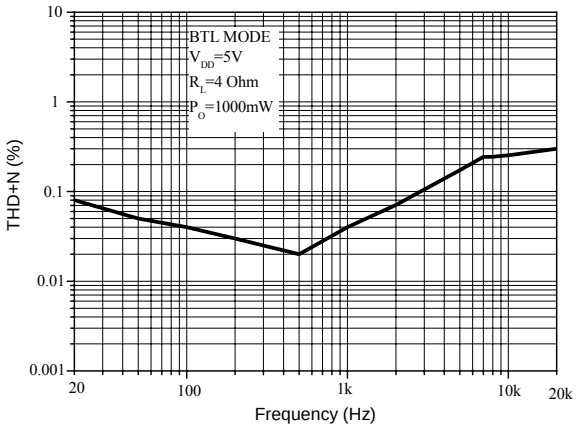
Total Harmonic Distortion + Noise vs. Output Power



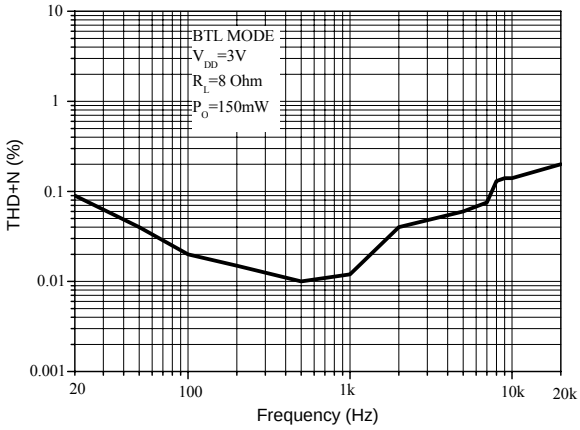
Total Harmonic Distortion + Noise vs. Frequency



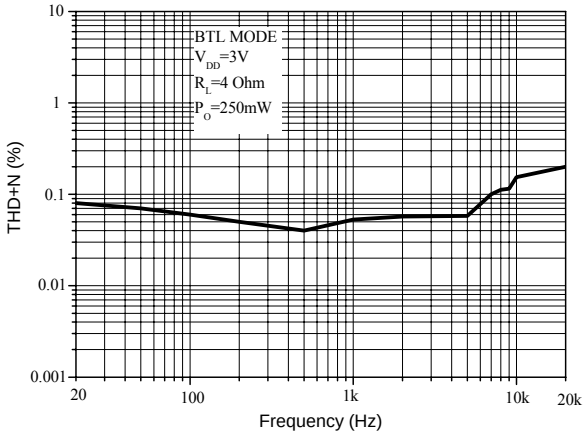
Total Harmonic Distortion + Noise vs. Frequency



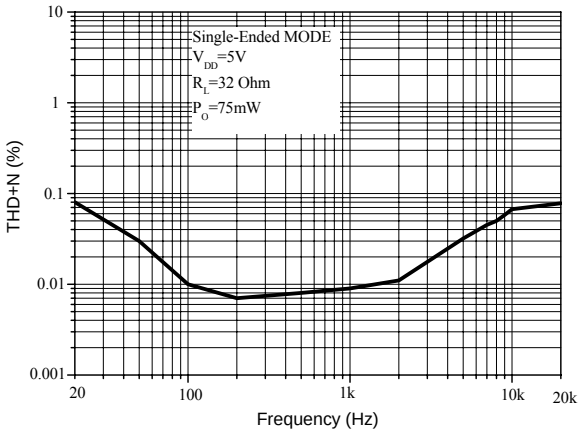
Total Harmonic Distortion + Noise vs. Frequency



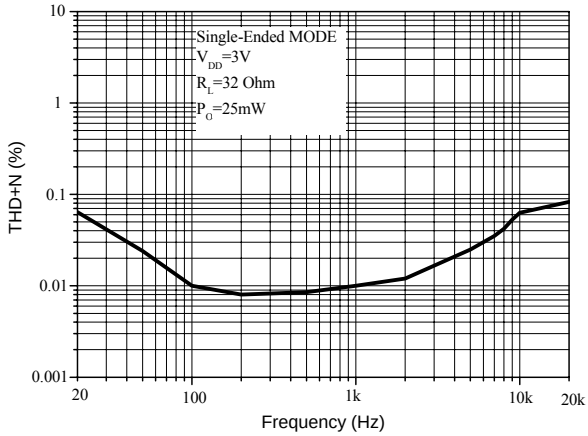
Total Harmonic Distortion + Noise vs. Frequency



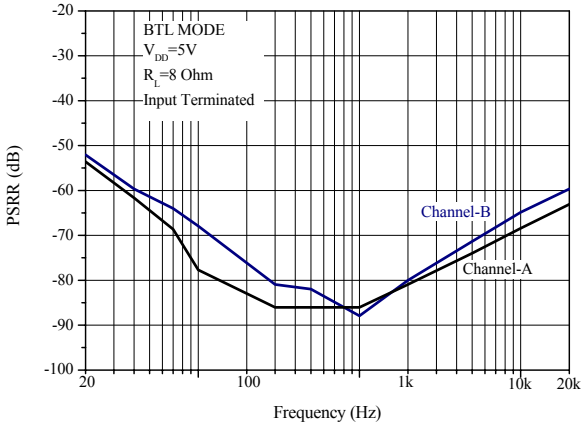
Total Harmonic Distortion + Noise vs. Frequency



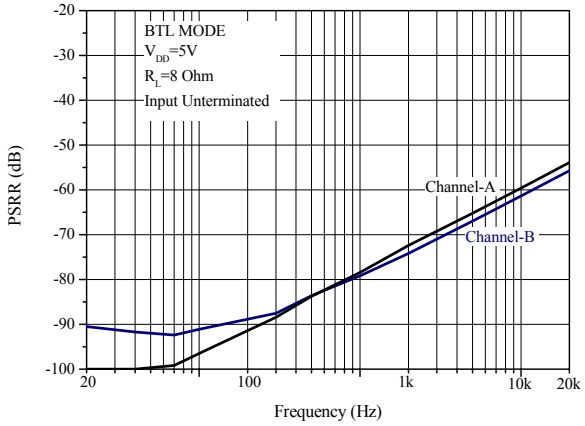
Total Harmonic Distortion + Noise vs. Frequency



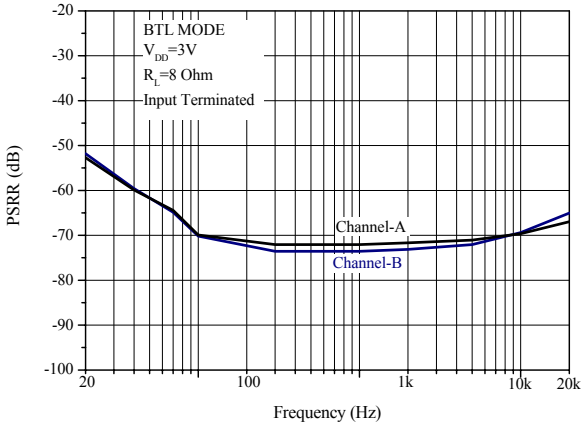
Power Supply Rejection vs. Frequency



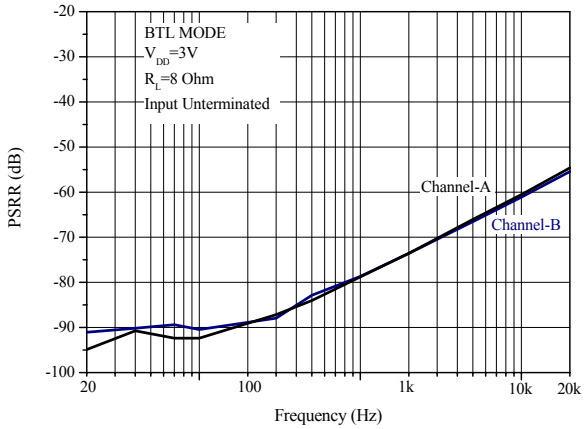
Power Supply Rejection vs. Frequency



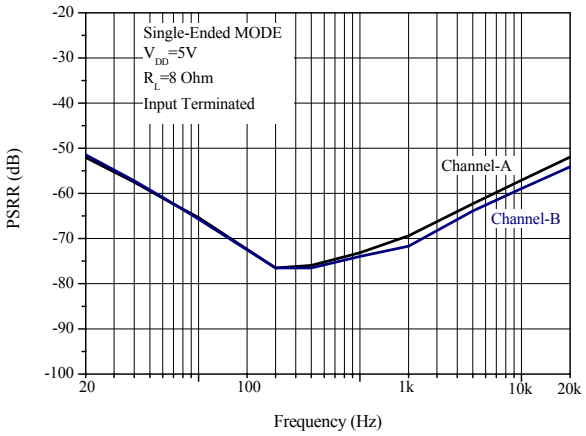
Power Supply Rejection vs. Frequency



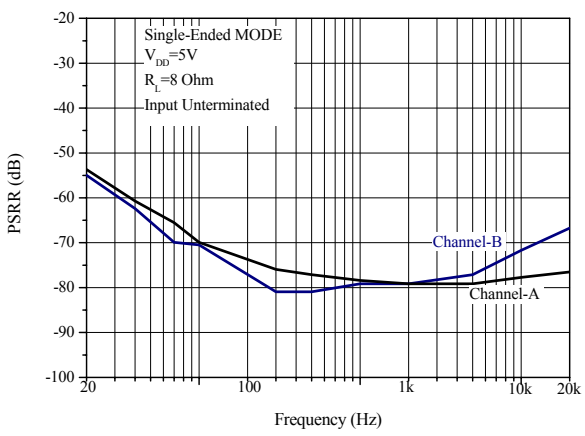
Power Supply Rejection vs. Frequency



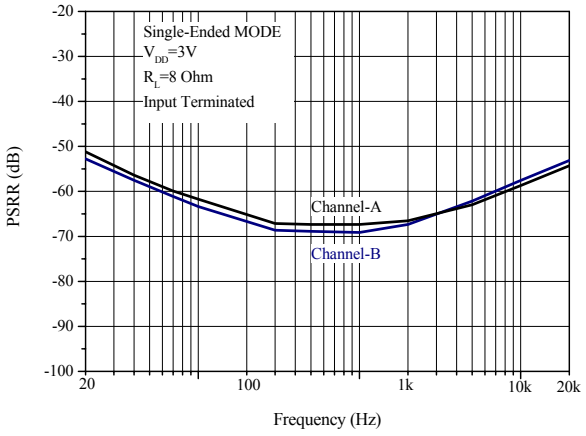
Power Supply Rejection vs. Frequency



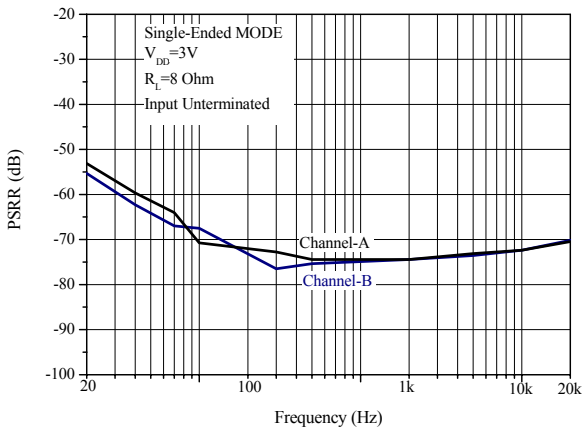
Power Supply Rejection vs. Frequency



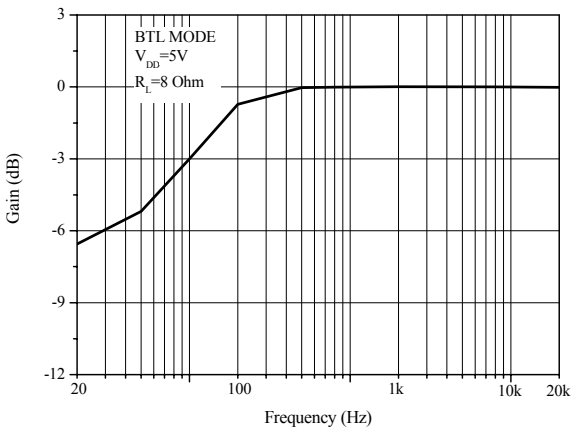
Power Supply Rejection vs. Frequency



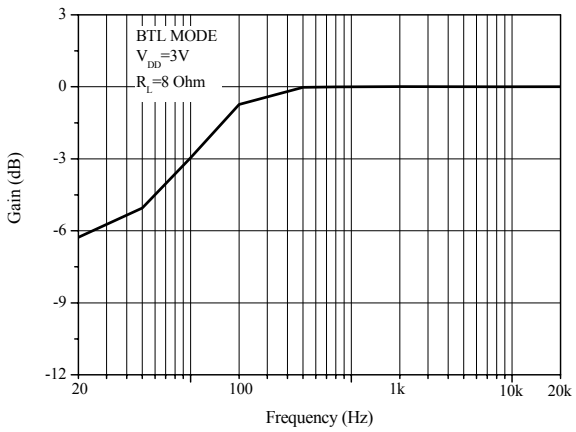
Power Supply Rejection vs. Frequency



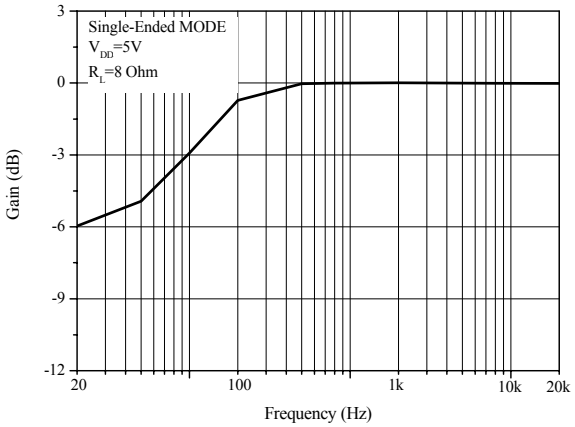
Frequency Response



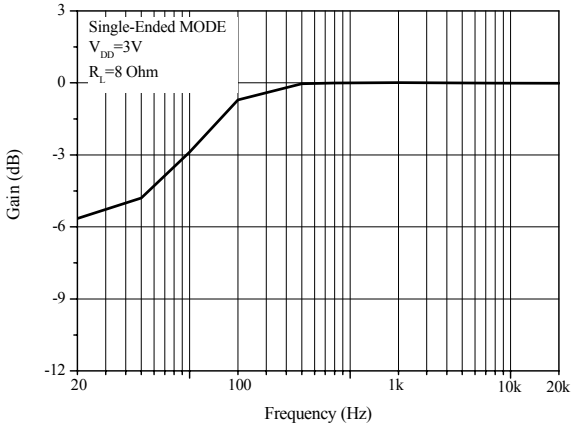
Frequency Response



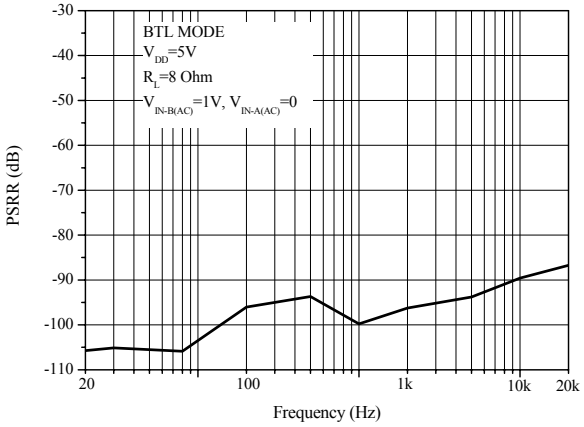
Frequency Response



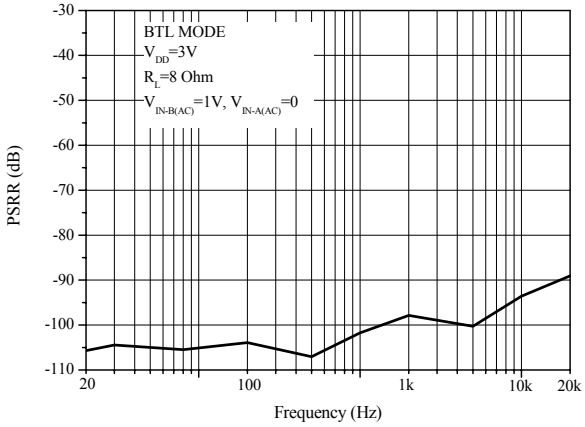
Frequency Response



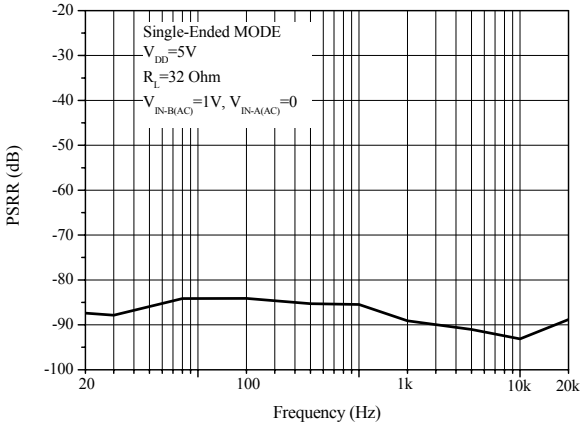
Crosstalk vs. Frequency



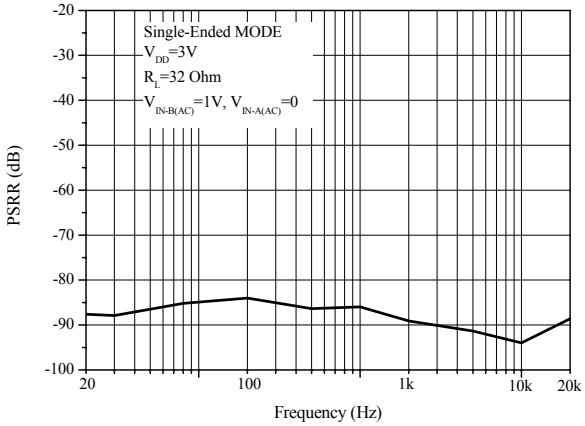
Crosstalk vs. Frequency



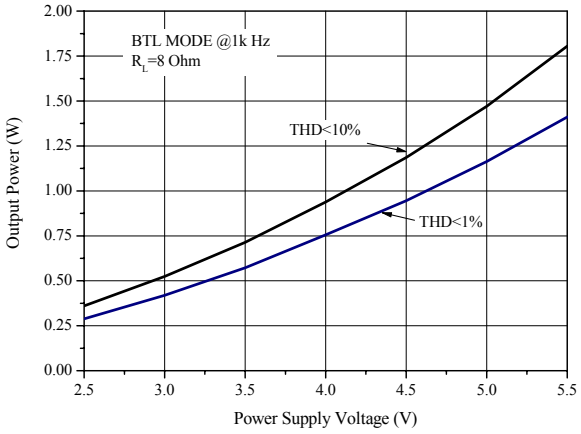
Crosstalk vs. Frequency



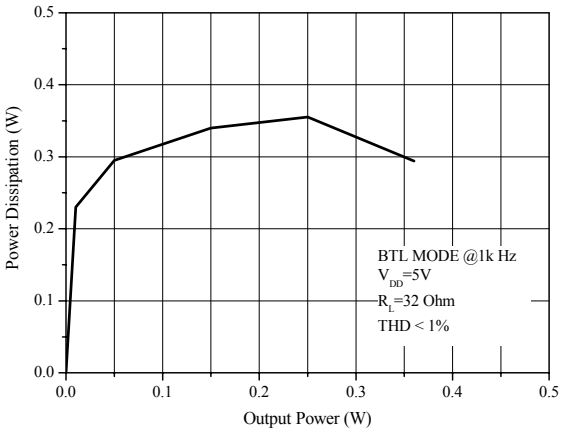
Crosstalk vs. Frequency



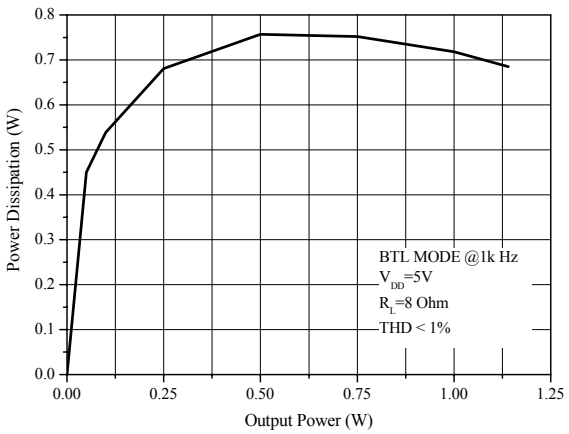
Power Supply Voltage vs. Output Power



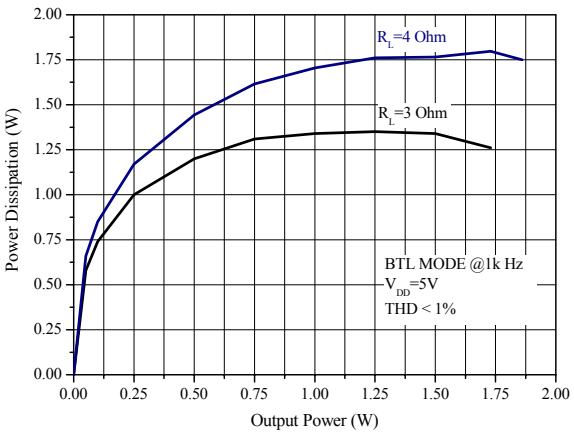
Power Dissipation vs. Output Power



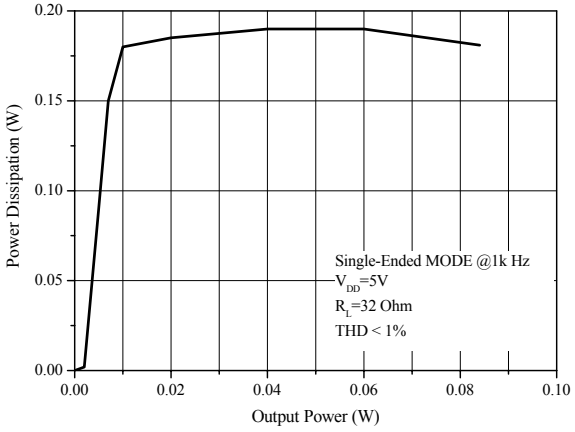
Power Dissipation vs. Output Power



Power Dissipation vs. Output Power



Power Dissipation vs. Output Power



APPLICATION INFORMATION

Bridge Configuration Explanation

As shown in Figure1, the PT5321 has two internal operational amplifiers per channel. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure1shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180˚. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f/Ri) \qquad (1)$$

or $A_{VD} = 2 * (R2/R1)$

or $A_{VD} = 2 * (R9/R8)$

By driving the load differentially through outputs +OUTA and –OUTA (or +OUTB, -OUTB), an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in PT5321, also creates a second advantage over single-ended amplifiers. Since the differential outputs, +OUTA and –OUTA (or +OUTB, -OUTB), are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation (2) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad \text{Single-Ended} \qquad (2)$$

A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the PT5321 has two operational amplifiers per channel in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 3.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad \text{Bridge Mode} \qquad (3)$$

The PT5321's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$PDMAX' = (TJMAX - TA)/\theta JA \qquad (4)$$

The PT5321's TJMAX = 150°C. In the QFN package soldered to a Exposed-PAD that expands to a copper area of 5in^2 on a PCB, the PT5321's θJA is 20°C/W. At any given ambient temperature TA, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting PDMAX for PDMAX' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the PT5321's maximum junction temperature.

$$TA = TJMAX - 2*PDMAX *\theta JA \qquad (5)$$

For a typical application with a 5V power supply and a 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the QFN package.

$$T_{JMAX} = P_{DMAX} *\theta_{JA} + T_A \qquad (6)$$

Equation (6) gives the maximum junction temperature TJMAX. If the result violates the PT5321's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures. The above examples assume that a device is a surface mount part operating around the maximum power dissipation point.

Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θJA. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation.

When adding a heat sink, the θJA is the sum of θJC, θCS, and θSA. (θJC is the junction-to-case thermal impedance, θCS is the case-to-sink thermal impedance, and θSA is the sink-to-ambient thermal impedance.) Refer to the **Typical Performance Characteristics** curves for power dissipation information at lower output power levels.

Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10μF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. However, their presence does not eliminate the need for bypassing the supply nodes of the PT5321. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

Shutdown Function

In order to reduce power consumption while not in use, the PT5321 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry whenever the Shutdown pin is put at logical "low". While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1μA. Therefore, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

Table 1. Logic Level Truth Table

$\overline{SHDN}$ PIN	HP_Logic PIN	HP_Sense PIN	Operational Mode
High	High	Don't Care	Single-Ended amplifiers
High	Low	Low	Bridged amplifiers
High	Don't Care	High	Single-Ended amplifiers
Low	Don't Care	Don't Care	Shutdown

Headphone Sense and Headphone Logic in Functions

Applying a logic level to the PT5321's HP_Sense headphone control pin turns off AmpA2 (+OUTA) and AmpB2 (+OUTB) muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

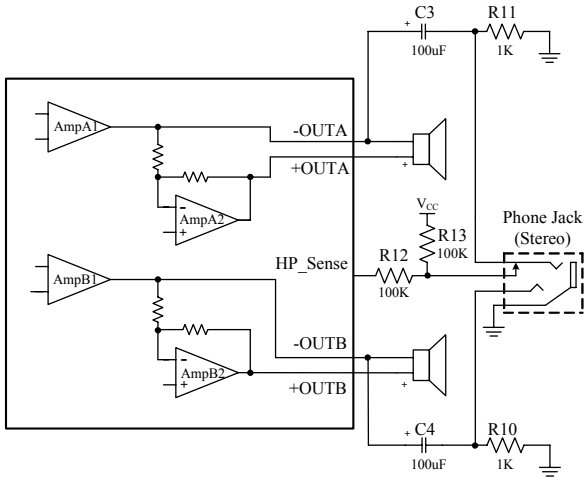


Figure 2. Headphone Circuit

Figure 2 shows the implementation of the PT5321's headphone control function. With no headphones connected to the headphone jack, the R11-R13 voltage divider sets the voltage applied to the HP_Sense pin (pin 20) at approximately 50mV. This 50mV enables AmpA2 (+OUTA) and AmpB2 (+OUTB) placing the PT5321 in bridged mode operation. While the PT5321 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from −OUTA and allows R13 to pull the HP_Sense pin up to VDD. This enables the headphone function, turns off AmpA2 (+OUTA) and AmpB2 (+OUTB) which mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistors R10 and R11. These resistors have negligible effect on the PT5321's output drive capability since the typical impedance of headphones is 32Ω. *Figure 2* also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP Sense pin when connecting headphones.

There is also a second input circuit that can control the choice of either BTL or SE modes. This input control pin is called the HP (Headphone) Logic Input. When the HP Logic input is high, PT5321 operates in SE mode. When HP_Logic is low (& the HP_Sense pin is low), the PT5321 operates in the BTL mode. In the BTL mode (HP_Logic low and HP_Sense Low) if the Headphones are connected directly to the Single Ended outputs (not using the HP_Sense pin on the HP Jack) then both the Speaker (BTL) and Headphone (SE) will be functional. In this case the inverted op amp outputs drive the Speaker as well as the HP load, i.e. 8 ohms in parallel with 32 ohms. As the PT5321 is capable of driving up to a 3 ohm load driving the Speakers and the Headphones at the same time will not be a problem as long as the parallel resistance of each Speaker and each Headphone driver are more than 3 ohms. As outlined above driving the Speaker (BTL) and Headphone (SE) loads simultaneously using PT5321 is simple and easy. However this configuration will only work if the HP_Logic pin is used to control the BTL/SE operation and HP_Sense pin is connected to GND.

Proper Selection of External Components

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the PT5321 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The PT5321 is unity-gain stable which gives the designer maximum system flexibility. The PT5321 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Input Capacitor Value Selection

Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure1*. The input resistors (R1, R9) coupling capacitor, C_i (C1, C2), forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. Equation (7) states the -3dB cutoff frequency of the input high pass filter.

$$f_{-3dB} = \frac{1}{2\pi RiCi} = \frac{1}{2\pi Rl C1} \qquad (7)$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_i (C1, C2). A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally $V_{DD}/2$). The amplifier's output charges the input capacitor through the feedback resistors, R2 and R8. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the PT5321 turns on. The slower the PT5321's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually pop&click free shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0µF is recommended in all but the most cost sensitive designs.

Audio Power Amplifier Design

A 1W/8Ω Audio Amplifier

Given:

Power Output:	$1W_{rms}$
Load Impedance:	8Ω
Input Level:	$1V_{rms}$
Input Impedance:	20kΩ
Bandwidth:	100Hz–20kHz ± 0.25dB

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the PT5321 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 8.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \qquad (8)$$

From Equation 8, the minimum A_{VD} is 2.83. For this example, let A_{VD} =3. The amplifier's overall gain (non 3D mode) is set using the input (R1 and R9) and feedback resistors R2 and R8.

$$R_f / R_i = R2/R1 = R8/R9 = A_{VD}/2 \qquad (9)$$

Since the desired input impedance was 20kΩ, with a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20kΩ and R_f = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3dB frequency points. Five times away from a −3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

$$f_L = 100Hz/5 = 20Hz$$

and

$$f_H = 20kHz \times 5 = 100kHz$$

As mentioned in the **External Components** section, R_i in conjunction with C_i create a high-pass filter. Find the coupling capacitor's value using Equation (10).

$$C_i \geq 1/(2\pi R_1 f_L) \qquad (10)$$

This result is

$$C_i \geq 1/(2\pi * 20k\Omega * 20Hz) = 0.397\mu F$$

Use a 0.39µF capacitor, the closest standard value.

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With an A_{VD} = 3 and f_H = 100k Hz, the resulting the closed-loop gain bandwidth product (GBWP) is 300k Hz which is much smaller than the PT5321's GBWP.

3D Enhancement

The PT5321 features a 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement improves the apparent stereo channel separation whenever the left and right speakers are too close to one another, due to system size constraints or equipment limitations.

An external RC network is required to enable the 3D effect. The amount of the 3D effect is set by the R5 and C7 or C3D_ADJ. Decreasing the value of R5 will increase the 3D effect. Increasing the value of the capacitors, C7 or C3D_ADJ, will decrease the low cutoff frequency at which the 3D effect starts to occur as show in Equation (11).

$$f_{3D(-3dB)} = 1/(2\pi * R_{3D} * C_{3D}) \qquad (11)$$

Activating the 3D effect by applying V_{DD} to PIN 3D_CONTROL will cause an increase in gain by a multiplication factor of (1+20k/R5). The amount of perceived 3D is also dependent on many other factors such as speaker placement and the distance to the listener. Therefore, it is recommended that the user try various values of R5 and C3D to get a feel for how the 3D effect works in the application. There is not a "right or wrong" for the effect, it is merely what is most pleasing to the individual user. Take note that R3 and R4 replace R2, and R7 and R6 replace R8 when 3D mode is enabled.

Exposed-PAD Package PCB Mounting Considerations

The PT5321's exposed-PAD QFN package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at ≤1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the PT5321's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The QFN package must have its exposed-PAD soldered to a copper pad on the PCB. The exposed-PAD's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the exposed-PAD's copper pad to the inner layer or backside copper heat sink area with 6(3x2) vias. The via diameter should be 0.012in~0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating through and solder-filling the vias. Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal $2.5in^2$ (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the PT5321 should be $5in^2$ (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the PT5321's thermal shutdown protection.

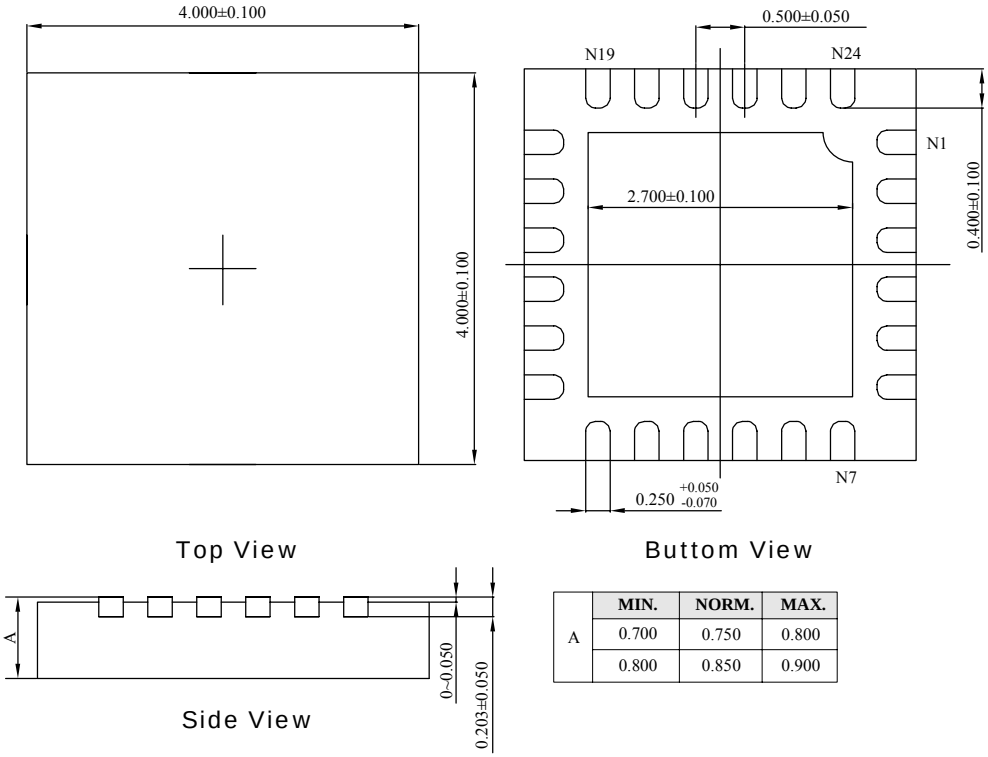
PCB Layout and Supply Regulation Considerations for Driving 3Ωand 4ΩLoads

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

PACKAGE INFORMATION

QFN-24 (4X4)



	MIN.	NORM.	MAX.
A	0.700	0.750	0.800
	0.800	0.850	0.900