PT5326

2.0 W/CH Stereo Filter-free Class-D Audio Power Amplifier

GENERAL DESCRIPTION

The PT5326 is a dual 2.0W high efficiency filterless class D audio power amplifier in a 4mm×4mm QFN-16 and SMD-16 or SOP16 package that requires only five external components.

The PT5326 uses Class D architecture, the device delivers up to 2.0W while offering up to 80% efficiency.

The PT5326 offers a spread-spectrum PWM modulation scheme that reduces EMI-radiated emissions due to the modulation frequency. The device utilizes a fully differential architecture, a full bridged output, and comprehensive click-and-pop suppression.

The PT5326 features high 60dB PSRR, low 0.11% THD+N. Thermal-overload protection prevents the device from being damaged during a fault condition.

The PT5326 is ideal for cellular handsets and PDA applications.

FEATURES

- 2.0 W/Ch into 4 Ω at 5 V , THD<10%
- Selectable Gain of 6, 12, 18, and 24 dB
- 6mA Quiescent Current
- 0.5μA Shutdown Current
- Spread-Spectrum PWM Modulation
- Only Five External Components
- Thermal Protection
- Space Saving Packages: SMD16 QFN16,SOP16

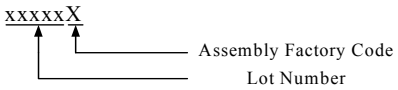
APPLICATIONS

- Wireless or Cellular Handsets
- Portable DVD
- Notebook PC
- Portable Radio
- Portable Gaming
- Educational Toys
- USB Speakers

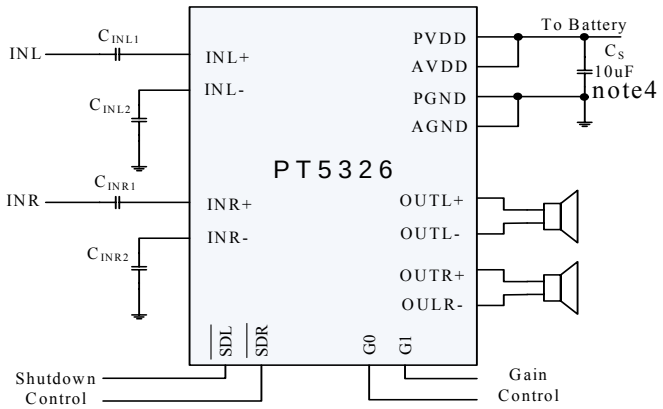
ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORMEDIA	MARKING
QFN16	-40 °C to 85 °C	PT5326EQFN	Tape and Reel 5000units	PT5326 xxxxxX
SOP16	-40 °C to 85 °C	PT5326ESOP	Tape and Reel 2500units	PT5326 xxxxxX

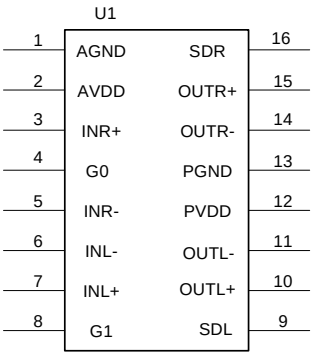
Note:



TYPICAL APPLICATION CIRCUIT

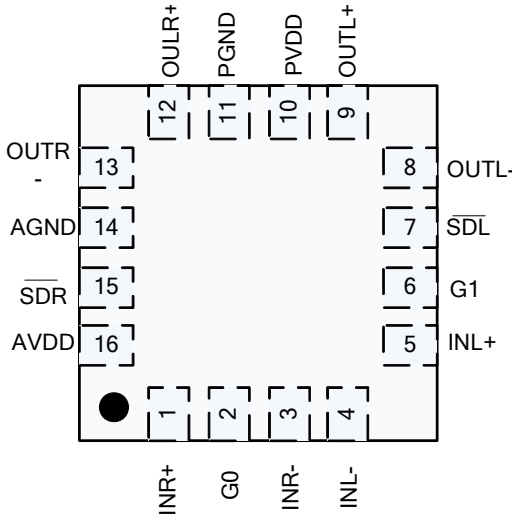


PIN ASSIGNMEN

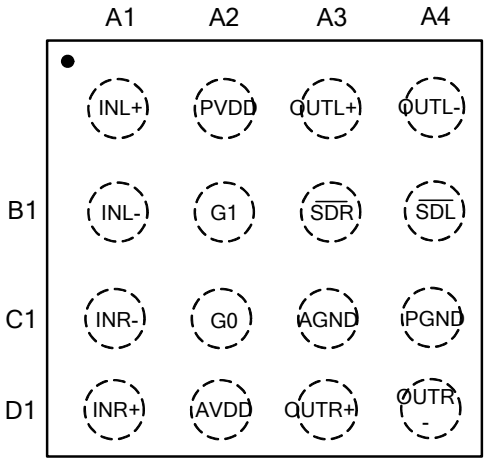


SOP16 (Top View)

PIN ASSIGNMEN



QFN16 (4x4 mm) Top View

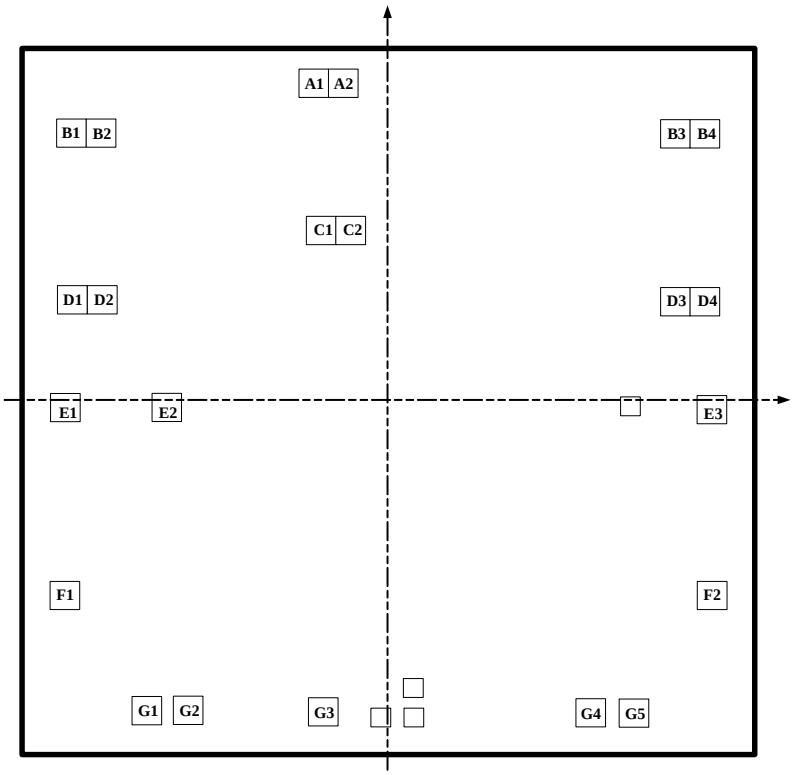


SMD16 Top View

PIN DESCRIPTIONS

QFN16	SMD16	SOP16	NAME	DESCRIPTION
1	D1	3	INR+	Right channel positive input
3	C1	5	INR-	Right channel negative input
5	A1	7	INL+	Left channel positive input
4	B1	6	INL-	Left channel negative input
15	B3	16	$\overline{SDR}$	Right channel shutdown terminal (shutdown at low)
7	B4	9	$\overline{SDL}$	Left channel shutdown terminal (shutdown at low)
2	C2	4	G0	Gain select (LSB)
6	B2	8	G1	Gain select (MSB)
10	A2	12	PVDD	Power supply (Must be same voltage as AVDD)
16	D2	2	AVDD	Analog supply (Must be same voltage as PVDD)
11	C4	13	PGND	Power ground
14	C3	1	AGND	Analog ground
13	D3	15	OUTR+	Right channel positive differential output
12	D4	14	OUTR-	Right channel negative differential output
8	A3	10	OUTL+	Left channel positive differential output
9	A4	11	OUTL-	Left channel negative differential output
			Thermal Pad	Connect the thermal pad of QFN package to PCB GND

PAD ASSIGNMENT



PAD DESCRIPTIONS

PADS	NAMES	POSITION	DESCRIPTION
A1, A2	PGND	(-198,883), (-118,883)	Power ground
B1, B2	OUTR-	(-845,743), (-765,743)	Right channel negative differential output
B3, B4	OUTL-	(765,743), (845,743)	Left channel negative differential output
C1, C2	PVDD	(-180,473), (-100,473)	Power supply (Must be same voltage as AVDD)
D1, D2	OUTR+	(-845,280), (-765,280)	Right channel positive differential output
D3, D4	OUTL+	(765,280), (845,280)	Left channel positive differential output
E1	$\overline{SDR}$	(-862,-21)	Right channel shutdown terminal (High = Enable, Low = Shutdown)
E2	AGND	(-591,-20)	Analog ground
E3	$\overline{SDL}$	(862,-21)	Left channel shutdown terminal (High = Enable, Low = Shutdown)
F1	AVDD	(-863,-544)	Analog supply (Must be same voltage as PVDD)
F2	G1	(863,-536)	Gain select (MSB)
G1	INR+	(-642,-863)	Right channel positive input
G2	G0	(-532,-863)	Gain select (LSB)
G3	INR-	(-173,-863)	Right channel negative input
G4	INL-	(540,-863)	Left channel negative input
G5	INL+	(657,-863)	Left channel positive input

ABSOLUTE MAXIMUM RATINGS (NOTE1)

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage	-0.3 ~ 6.0	V
V_{IN}	Input Voltage	-0.3 ~ V_{DD}+0.3	V
T_{STG}	Storage Temperature	-65 ~ +150	°C
P_{DMAX}	Continuous Power Dissipation (Note2)	Internally Limited	W
T_J	Operating Junction Temperature	-40 ~ +150	°C
PTR1	Thermal Resistance, SMD16: θ_{JA} (Note 3)	100	°C / W
PTR2	Thermal Resistance, QFN16(4x4): θ_{JA}	60	°C / W
PTR3	Thermal Resistance, SOP16: θ_{JA}	90	°C / W
T_{Solder}	Solder Temperature	235 °C, 10s	
	ESD Susceptibility (Note 4)	2	KV

RECOMMENDED OPERATING RANGE（Note 5）

SYMBOL	PARAMETER		VALUE	UNIT
V_{DD}	Supply voltage	AVDD, PVDD	2.5~5	V
V_{IH}	High-level input voltage	$\overline{SDL}$, $\overline{SDR}$, G0, G1	1.4~V_{DD}	V
V_{IL}	Low-level input voltage	$\overline{SDL}$, $\overline{SDR}$, G0, G1	0~0.4	V
T_A	Operating free-air temperature		-40 ~85	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Note 3: All bumps have the thermal resistance and contribute equally when used to lower thermal resistance. All bumps must connected to achieve specified thermal resistance

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits.

ELECTRICAL CHARACTERISTICS （Note 6, Note 7）

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	Inputs ac grounded, AV = 6dB, V_{DD} = 2.5 to 5.5V		5	25	mV
IQ	Supply current	V_{DD} = 5.5V, No load		6	9	mA
		V_{DD} = 3.6V, No load		5	7.5	
		V_{DD} = 2.5V, No load		4	6	
I_{SD}	Shutdown current				1.5	μA
$R_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 2.5V		700		mΩ
		V_{DD} = 3.6V		570		
		V_{DD} = 5.5V		500		

ELECTRICAL CHARACTERISTICS (continued)

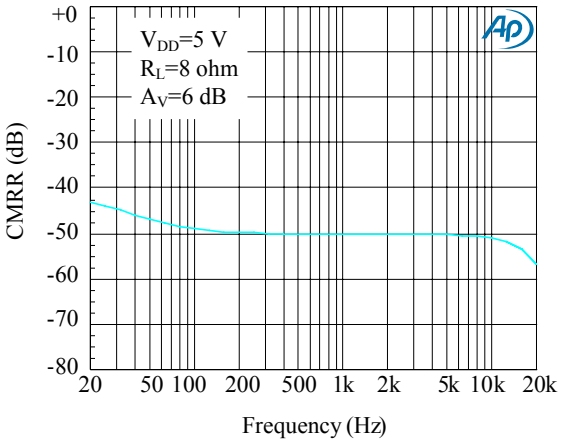
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	V_{DD} = 2.5V to 5.5V		400	500	600	kHz
	Closed-loop voltage gain	G0, G1 = 0.35V		5.5	6	6.5	dB
		G0 = V_{DD}, G1 = 0.35V		11.5	12	12.5	
		G0 = 0.35V, G1 = V_{DD}		17.5	18	18.5	
		G0, G1 = V_{DD}		23.5	24	24.5	
PO	Output power (per channel)	R_L = 8Ω	V_{DD} = 5.0V, f = 1kHz, THD = 10%		1.5		W
			V_{DD} = 3.6V, f = 1kHz, THD = 10%		0.8		
		R_L = 4Ω	V_{DD} = 5.0V, f = 1kHz, THD = 10%		2.0		
THD+N	Total harmonic distortion plus noise	P_O = 1W, V_{DD} = 5V, AV = 6dB, f = 1kHz			0.14 %		
		P_O = 0.5W, V_{DD} = 5V, AV = 6dB, f = 1kHz			0.11 %		
Xtalk	Channel crosstalk	P_O = 0.5 W, f = 1 kHz			-70		dB
PSRR	Supply ripple rejection ratio	V_{DD} = 5V, AV = 6dB, f = 217Hz			-60		dB
		V_{DD} = 3.6V, AV = 6dB, f = 217Hz			-60		
CMRR	Common mode rejection ratio	V_{DD} = 3.6V, VIC = 1Vpp, f = 217Hz			-60		dB
	Input impedance	Av = 6dB			28.2		kΩ
		Av = 12dB			17.76		
		Av = 18dB			11.15		
		Av = 24dB			5.89		
	Start-up time from shutdown	V_{DD} = 3.6V			1.5		ms
SNR	Signal to Noise Ratio	V_{DD} = 5V, P_O = 1W			90		dB
en	Output voltage noise	V_{DD} = 3.6V, f = 20 to 20 kHz, Inputs are ac grounded, AV = 6dB	No weighting		80		μV
			A weighting		50		

Note 6: Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

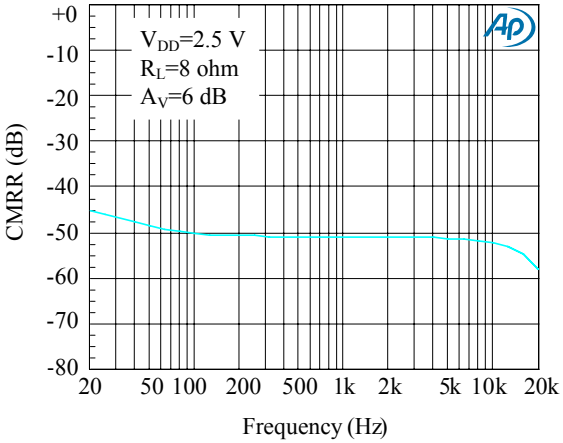
Note 7: Bypass capacitor Cs can't be smaller than 10uF and closes to the chip to prevent the vdd's glitch from exceeding 6.5V. Selecting 0805 or larger volume package type's capacitor is preferable.

TYPICAL PERFORMANCE CHARACTERISTICS

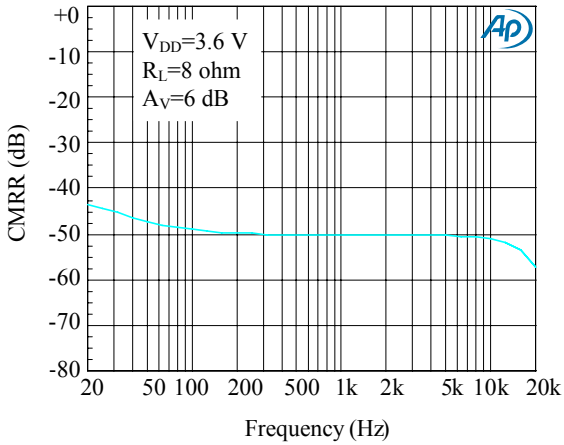
CMRR vs Freqency



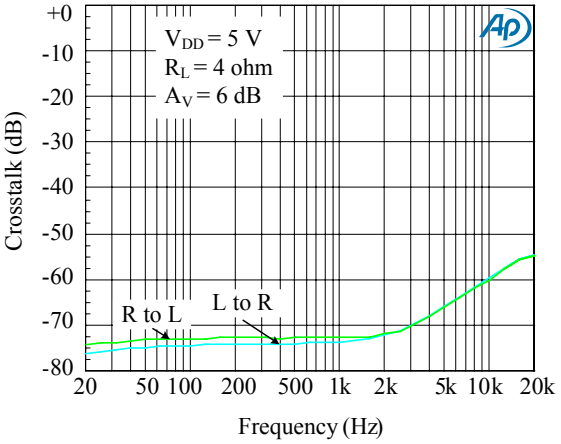
CMRR vs Freqency



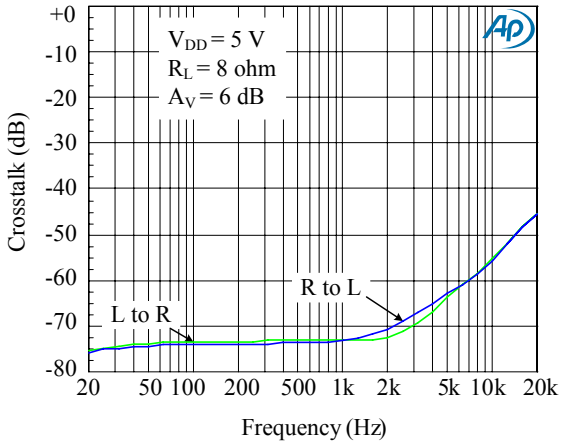
CMRR vs Freqency



Crosstalk vs Frequency



Crosstalk vs Frequency



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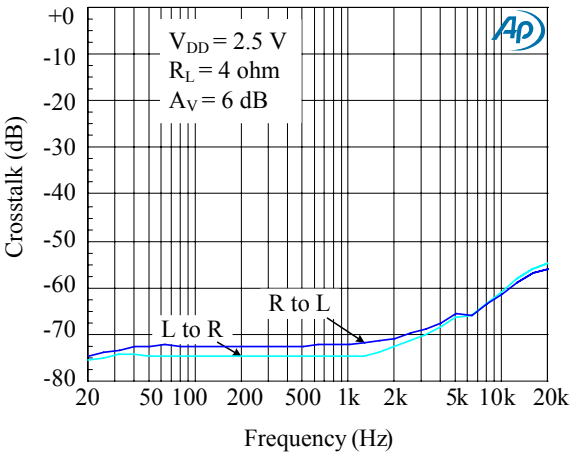
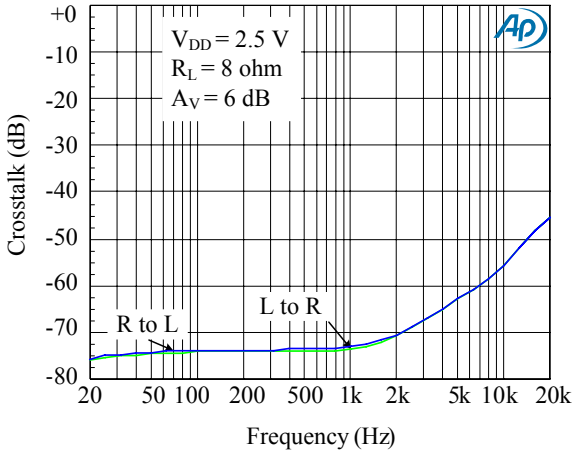
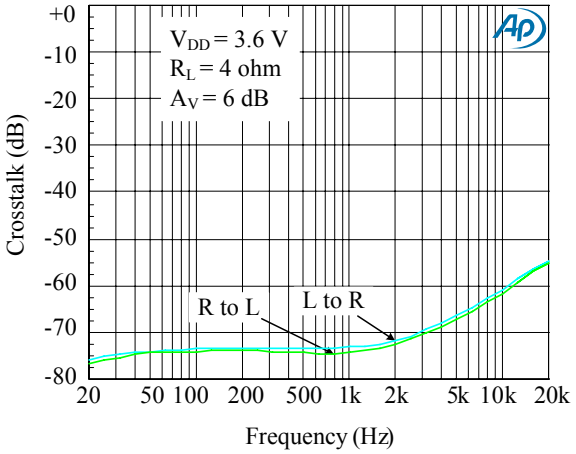


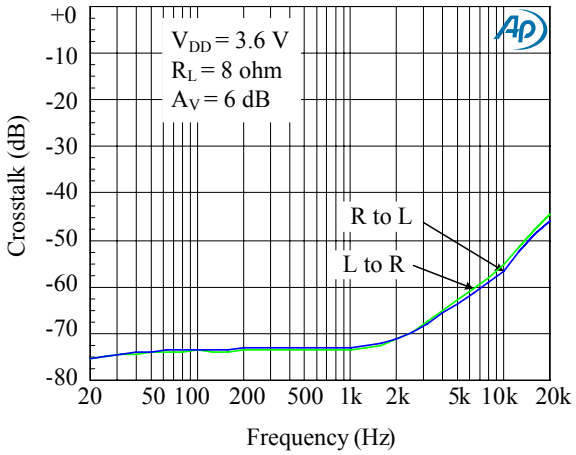
Crosstalk vs Frequency



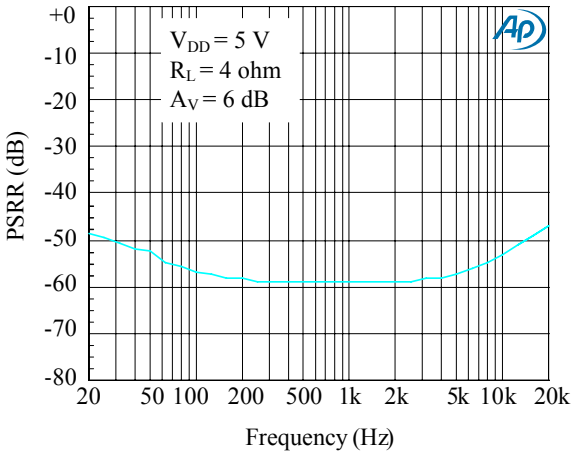
Crosstalk vs Frequency



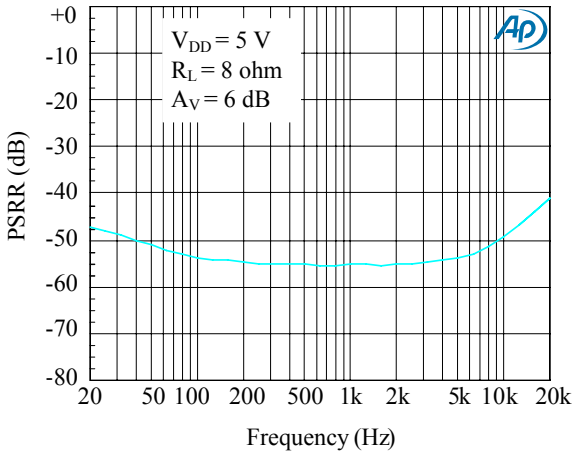
Crosstalk vs Frequency



PSRR vs Frequency



PSRR vs Frequency



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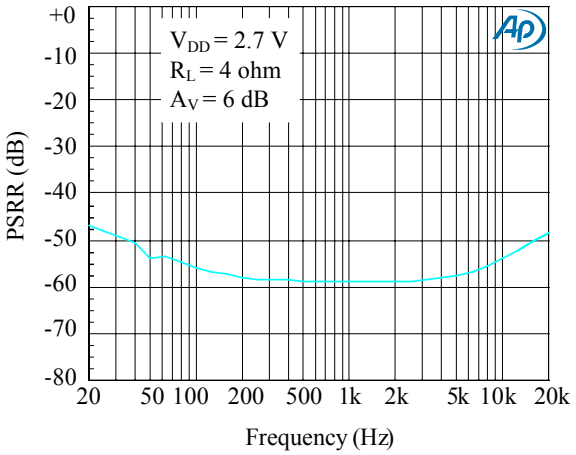

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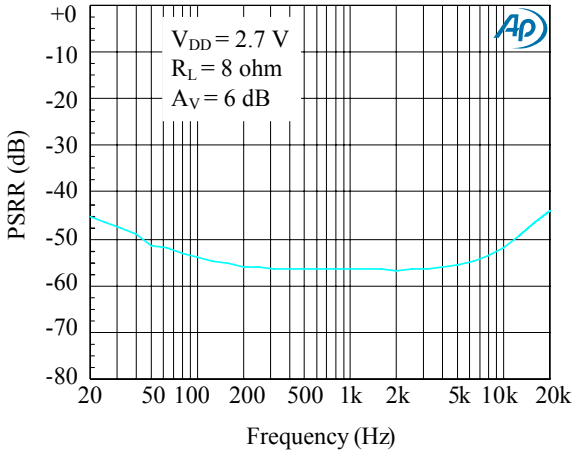

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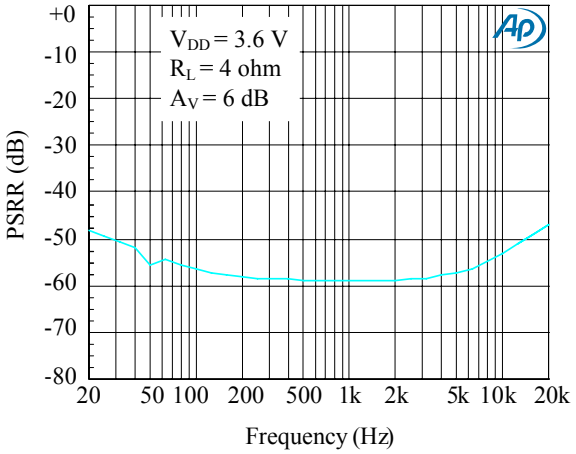
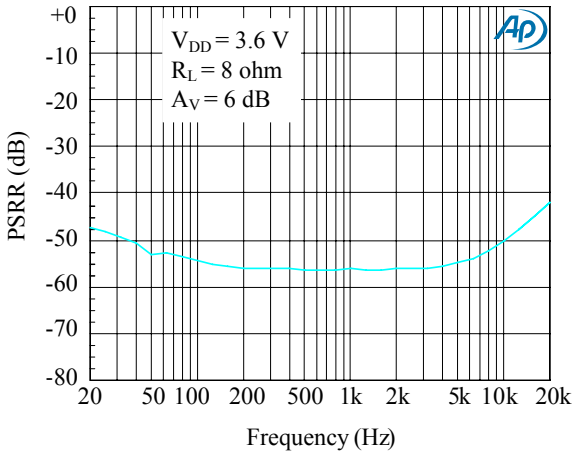
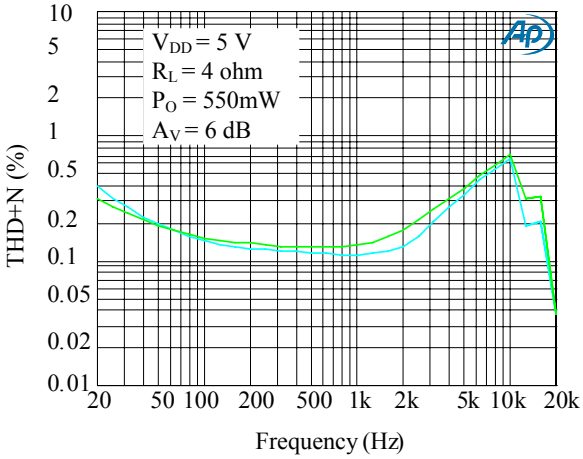


PSRR vs Frequency



THD+N vs Frequency



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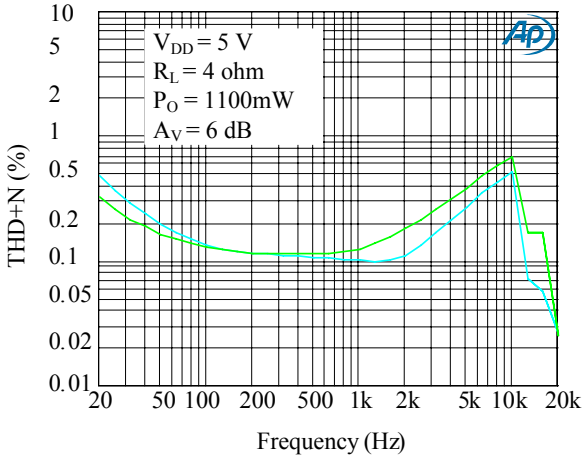

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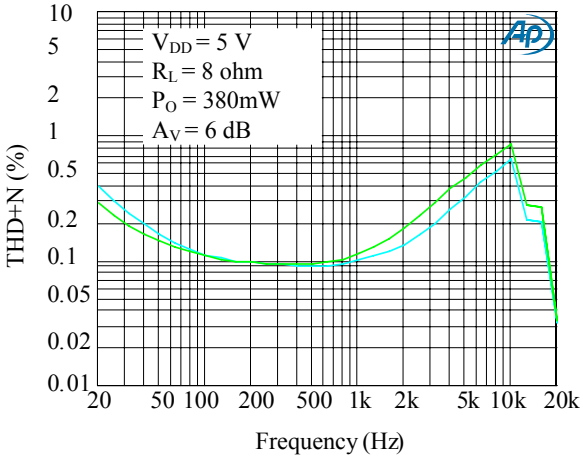
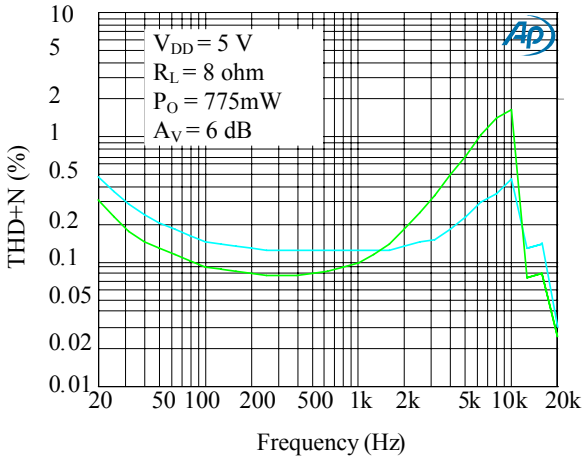


THD+N vs Frequency



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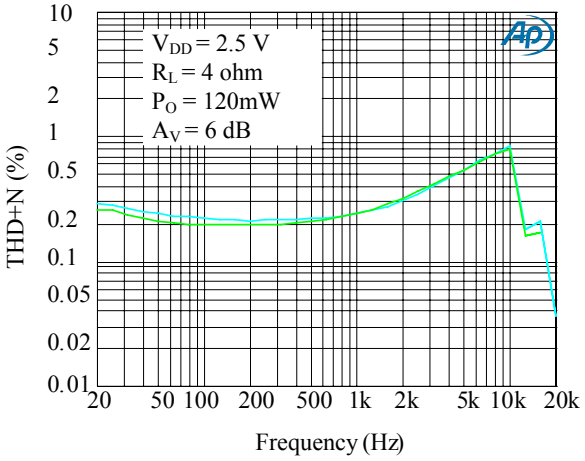

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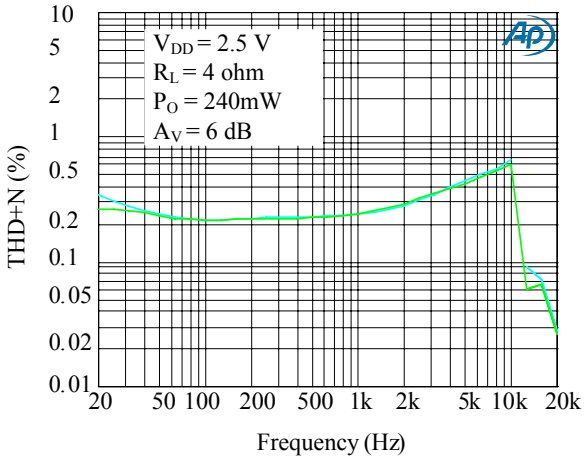

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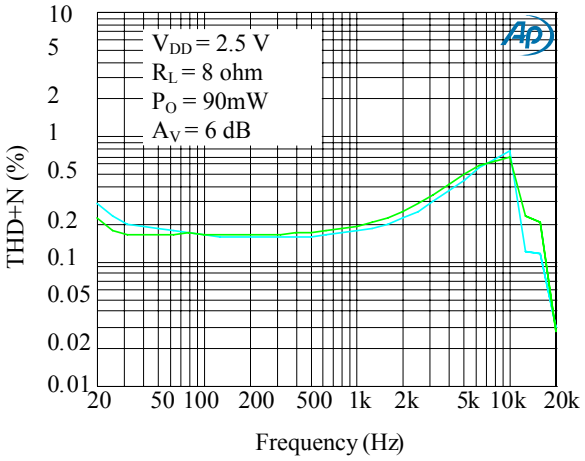

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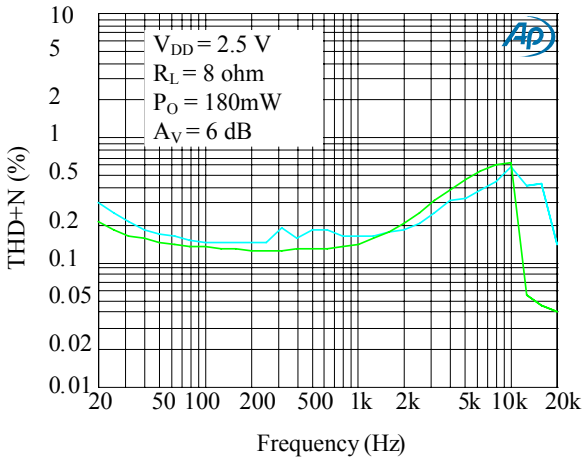

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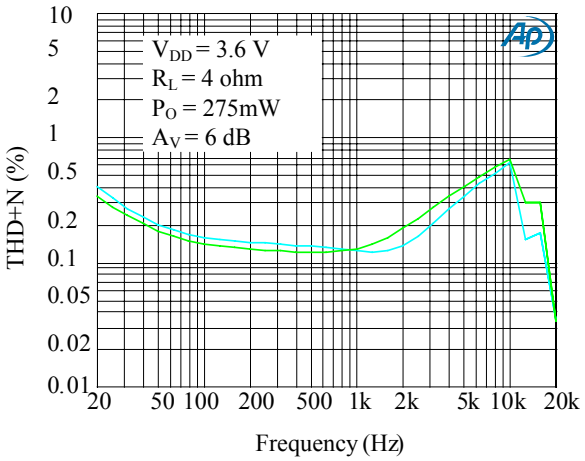

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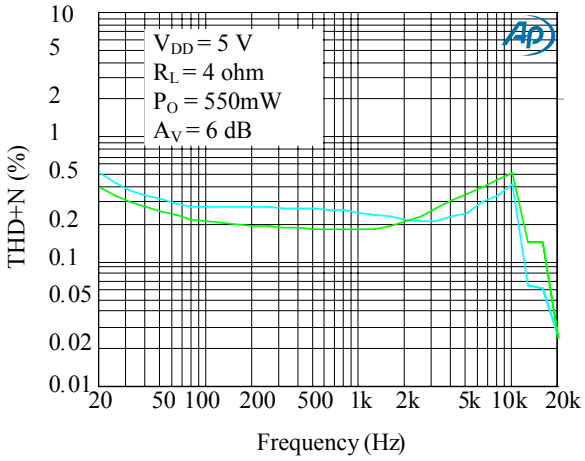

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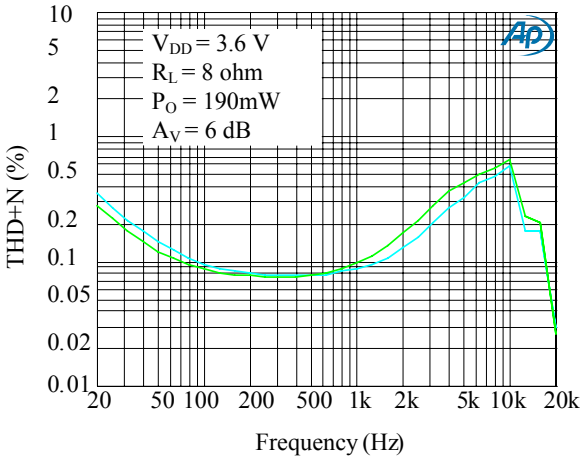

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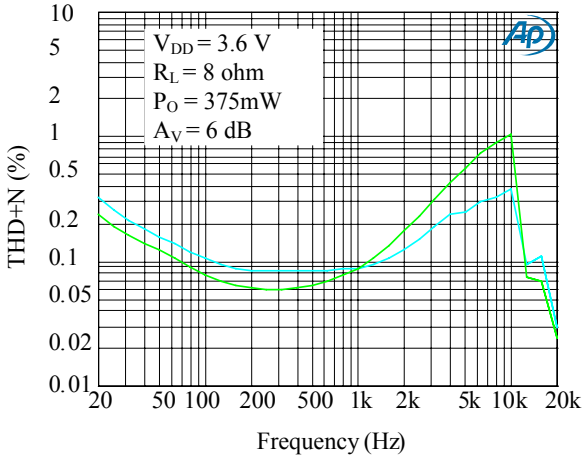
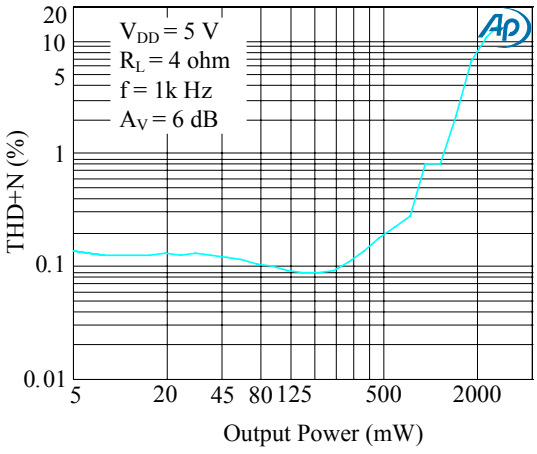
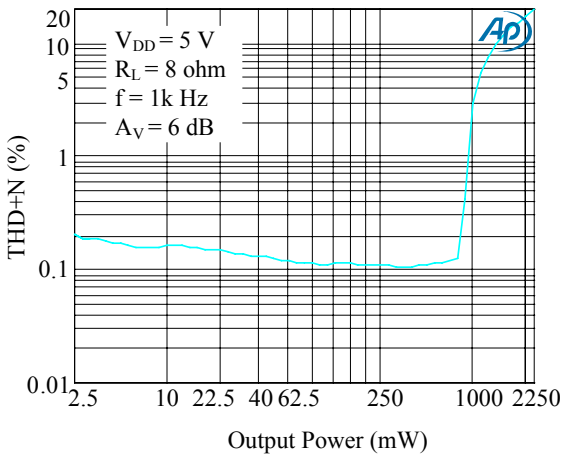


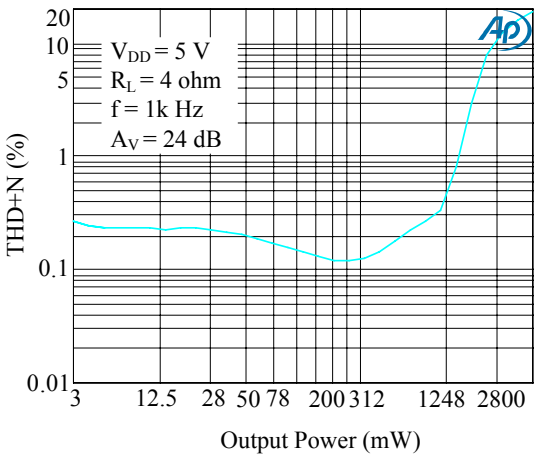
THD+N vs Output Power



THD+N vs Output Power



THD+N vs Output Power



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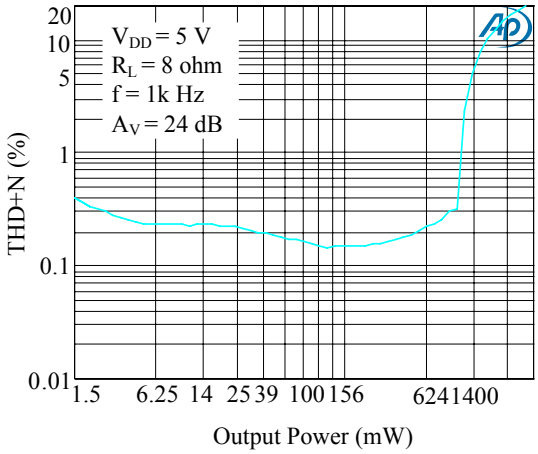
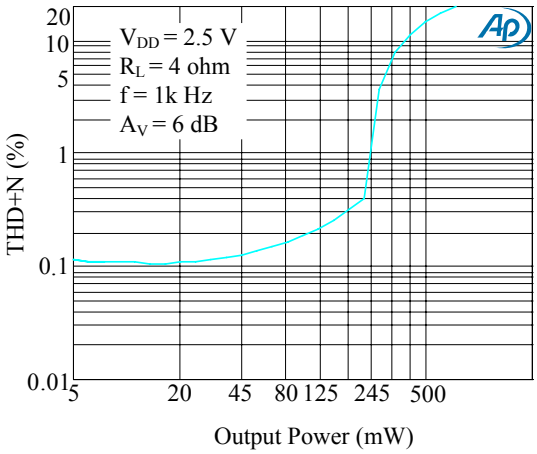
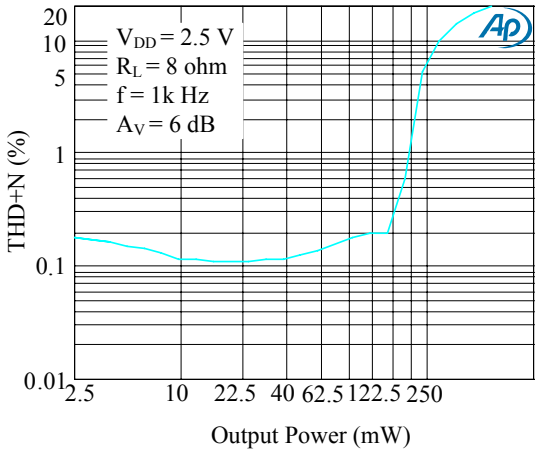


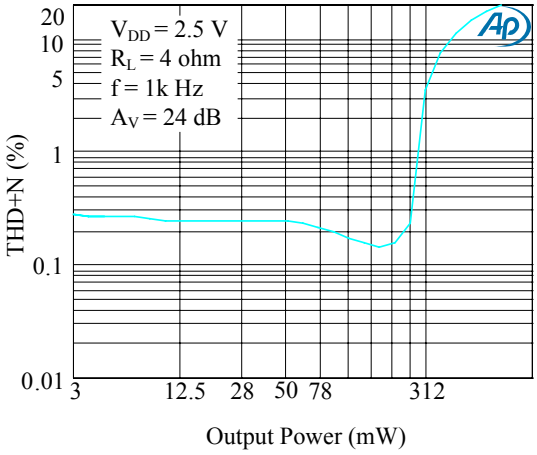
THD+N vs Output Power



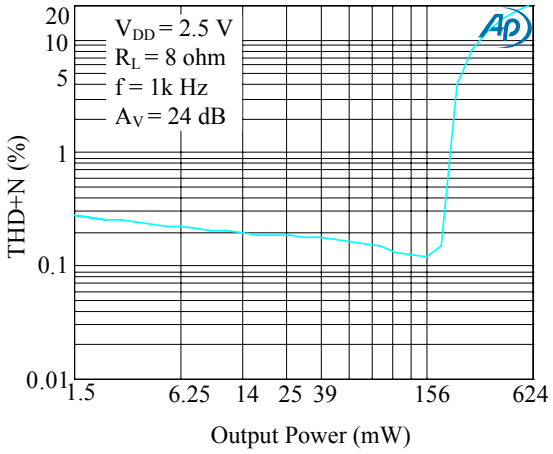
THD+N vs Output Power



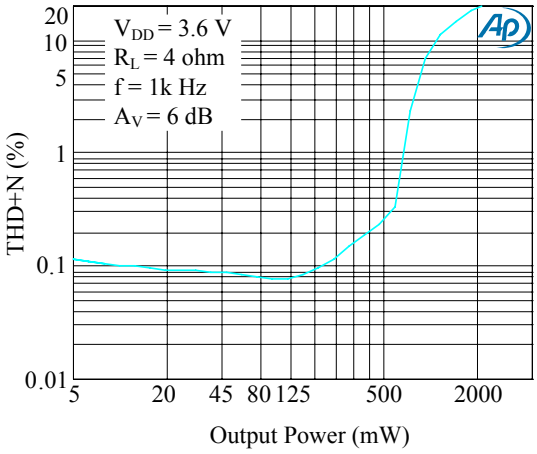
THD+N vs Output Power



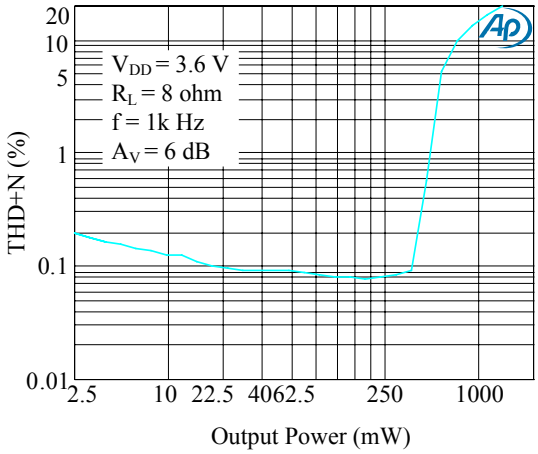
THD+N vs Output Power



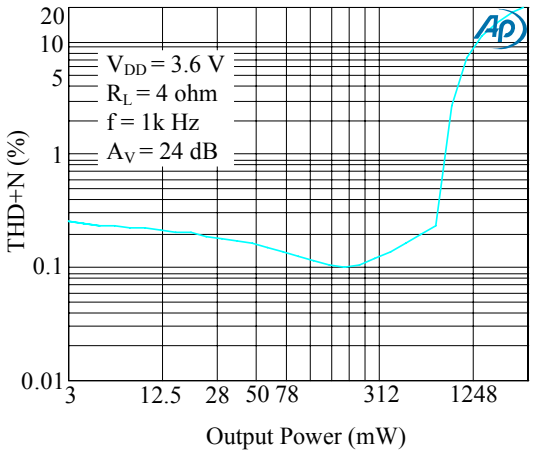
THD+N vs Output Power



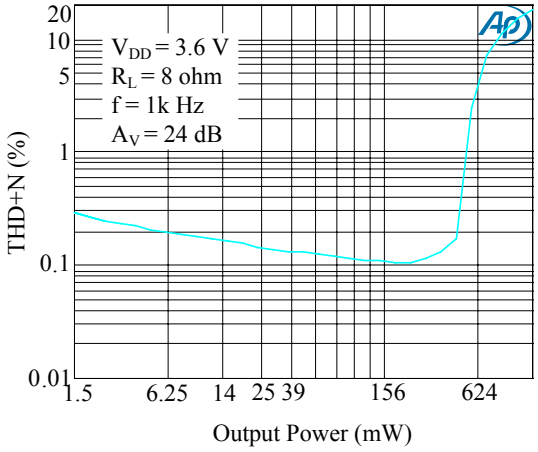
THD+N vs. Output Power



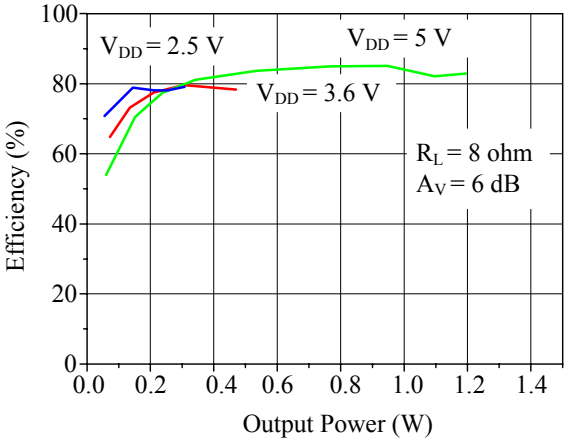
THD+N vs. Output Power



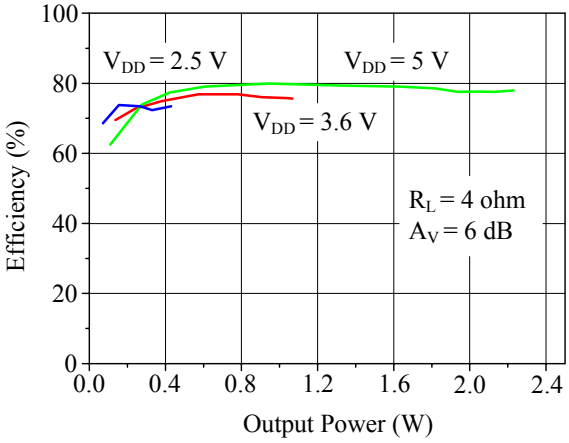
THD+N vs. Output Power



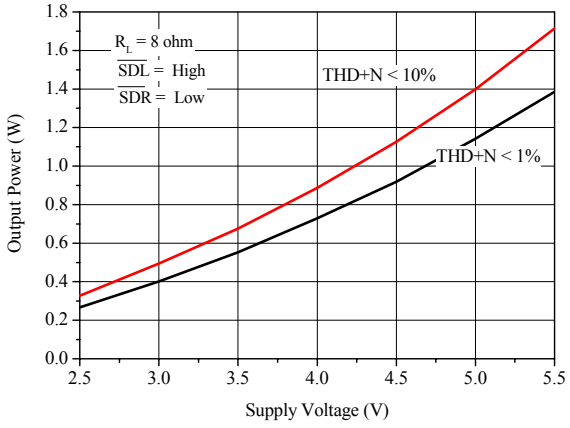
Output Power vs Efficiency



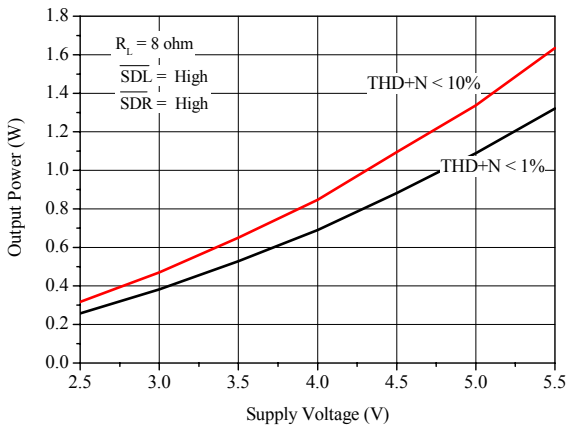
Output Power vs Efficiency



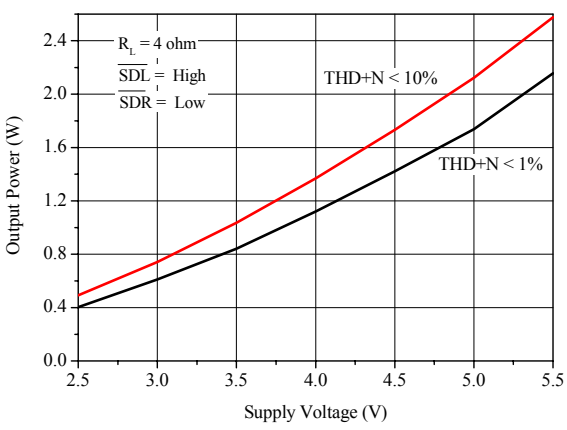
Supply Voltage vs Output Power



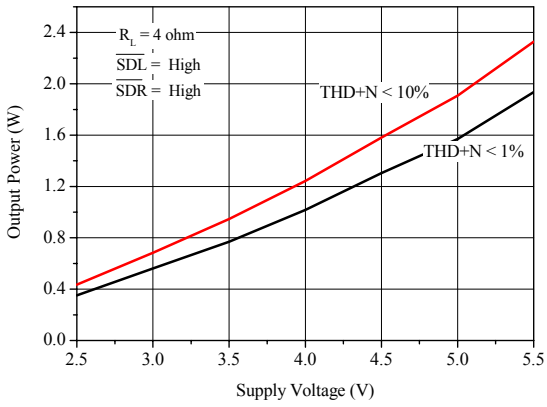
Supply Voltage vs Output Power



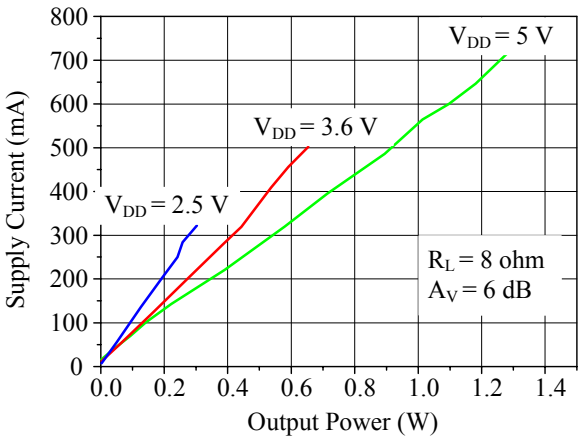
Supply Voltage vs Output Power



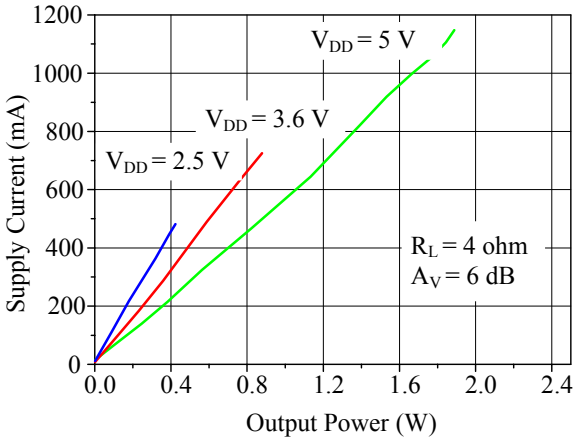
Supply Voltage vs Output Power



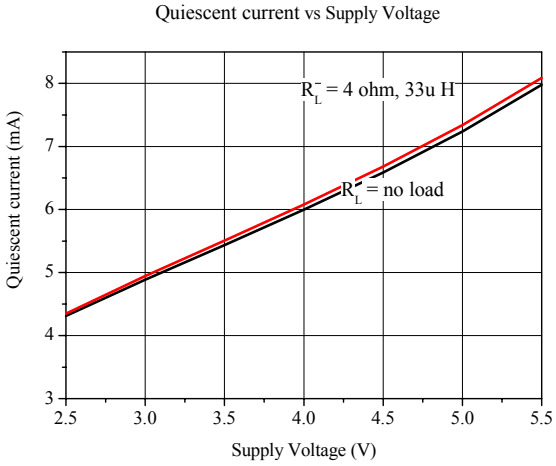
Supply Current vs Output Power



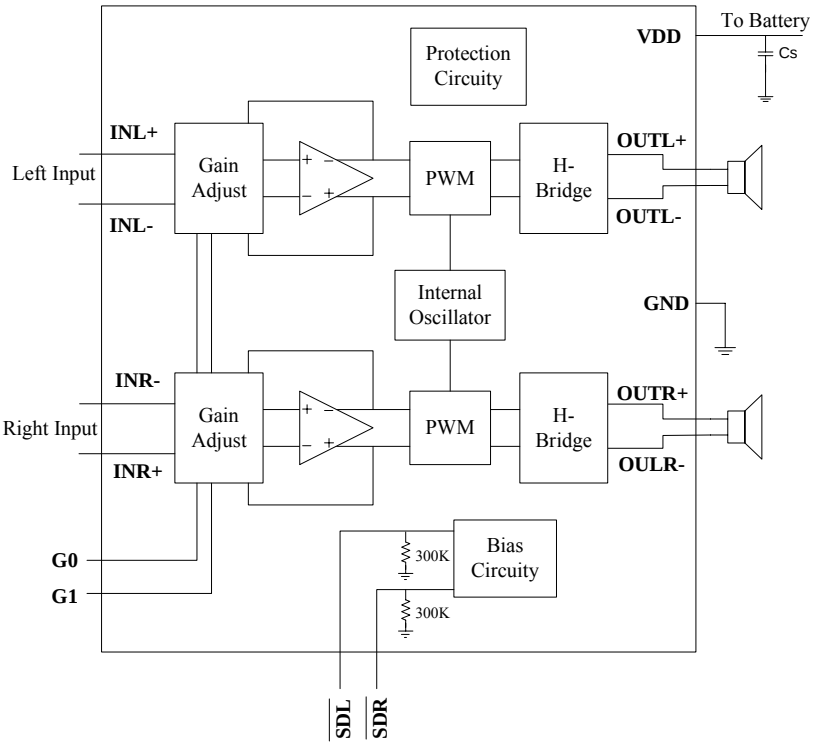
Supply Current vs Output Power



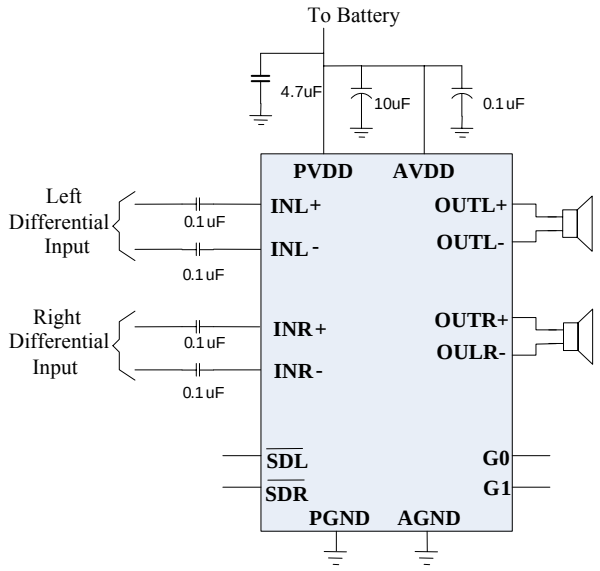
Quiescent current vs Supply Voltage



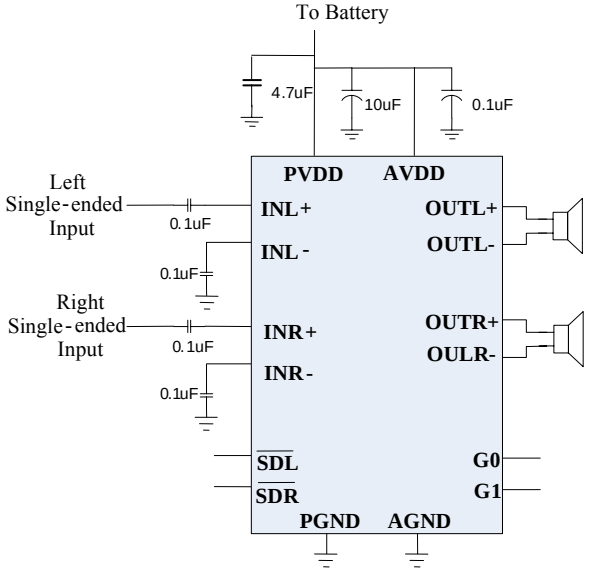
Block Diagram



APPLICATION INFORMATION



PT 5326 Application Schematic with Differential input and input Capacitors



PT 5326 Application Schematic with Single - Ended input Capacitors

DECOUPLING CAPACITOR (C_S)

The PT5326 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor or tantalum capacitor, typically 10μF, placed as close as possible to the device PV_{DD} lead works best. Placing this decoupling capacitor close to the PT5326 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10μF or greater 0805 capacitor placed near the audio power amplifier would also help.

INPUT CAPACITORS (CI)

The PT5326 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to VDD -0.8 V. If the input signal is not biased within the recommended common-mode input range, if high pass filtering is needed (see Figure above), or if using a single-ended source (see Figure above), input coupling capacitors CI are required.

The input capacitors and input resistors R_I form a high-pass filter with the corner frequency, fc, determined in Equation1.

$$f_c = \frac{1}{2\pi R_I C_I} \qquad (1)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Equation 2 is used to solve for the input coupling capacitance.

$$C_I = \frac{1}{2\pi R_I f_c} \qquad (2)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

COMPONENT LOCATION

Place all the external components very close to the PT5326. Placing the decoupling capacitor, C_S, close to the PT5326 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

PCB LAYOUT CONSIDERATIONS

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the PT5326 and the load results is lower output power and decreased efficiency. Higher trace resistance between the supply and the PT5326 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasite capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI standpoint, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the PT5326 and the speaker increase, the amount of EMI radiation will increase

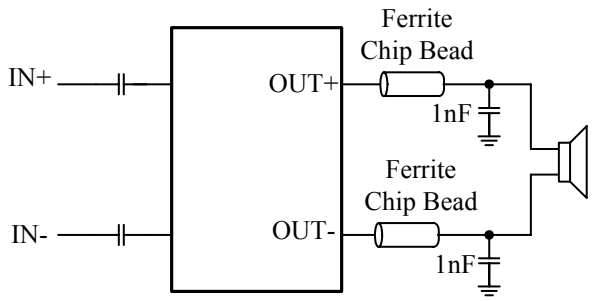
since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.
Ferrite chip inductors placed close to the PT5326 may be needed to reduce EMI radiation. The value of the ferrite chip is very application specific.

WHEN TO USE AN OUTPUT FILTER

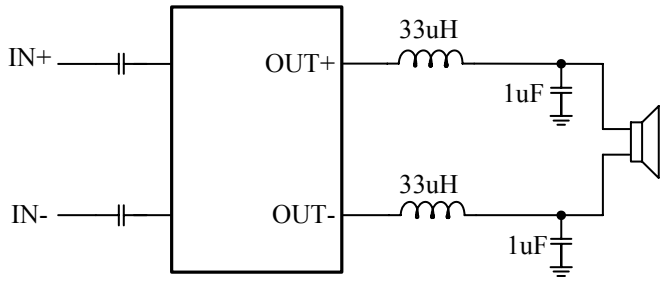
Design the PT5326 without an output filter if the traces from amplifier to speaker are short. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter often can be used if the design is failing radiated emissions without an LC filter, and the frequency-sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an LC output filter if there are low-frequency (<1 MHz) EMI-sensitive circuits and/or there are long leads from amplifier to speaker.



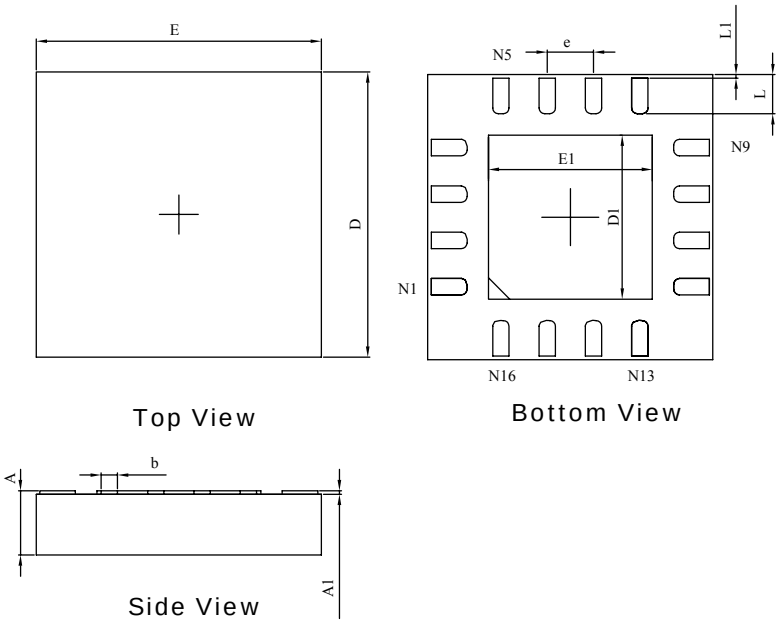
Ferrite Chip Bead Filter



Typical LC Output Filter, Cut-Off Frequency of 27k Hz

PACKAGE INFORMATION

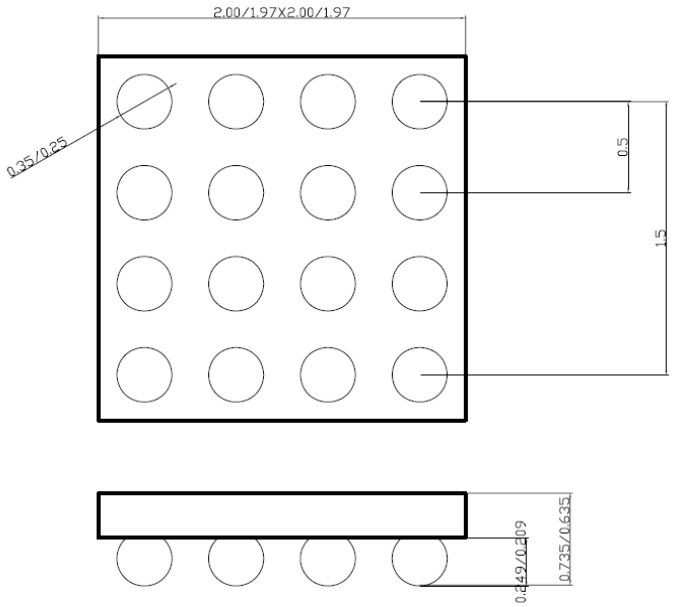
QFN16 (4X4):



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.010	0.090	0.000	0.004
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.300 REF.		0.091 REF.	
E1	2.300 REF.		0.091 REF.	
b	0.180	0.280	0.007	0.011
e	0.650 BSC.		0.026 BSC.	
L	0.500	0.600	0.020	0.024
L1	0.000	0.050	0.000	0.002

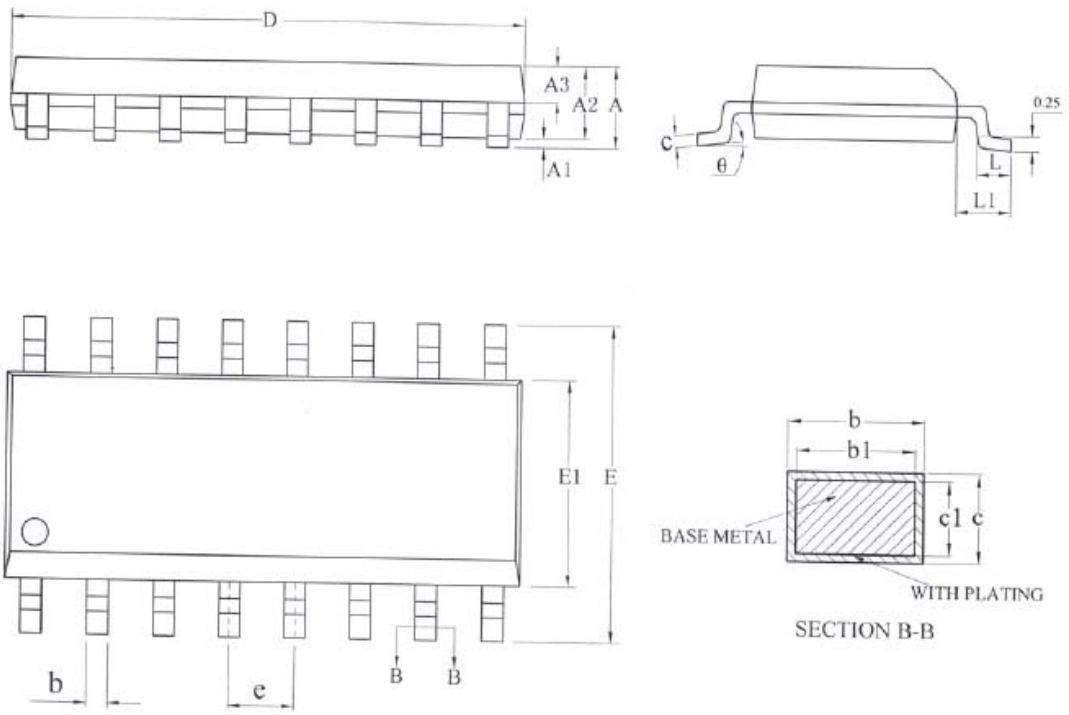
PACKAGE INFORMATION

SMD16 (2X2)



PACKAGE INFORMATION

SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°