18W Stereo Class-D Audio Amplifier

Features

- Dual supply voltage
  12 ~ 24V for loudspeaker driver
  3.3V for others
- Loudspeaker power from 24V supply
  8 W/ch into 8Ω @ 1% THD+N for stereo
  10 W/ch into 8Ω @ 10% THD+N for stereo
- Loudspeaker power from 24V supply
  15 W/ch into 4Ω @ 1% THD+N for stereo
  18 W/ch into 4Ω @ 10% THD+N for stereo
- Single-ended analog inputs
- Single-ended outputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-circuit protection with auto recovery
- Thermal protection with auto recovery
- Under-voltage detection
- Pop noise and click noise reduction

Applications

- TV audio
- Boom-Box
- Powered speaker

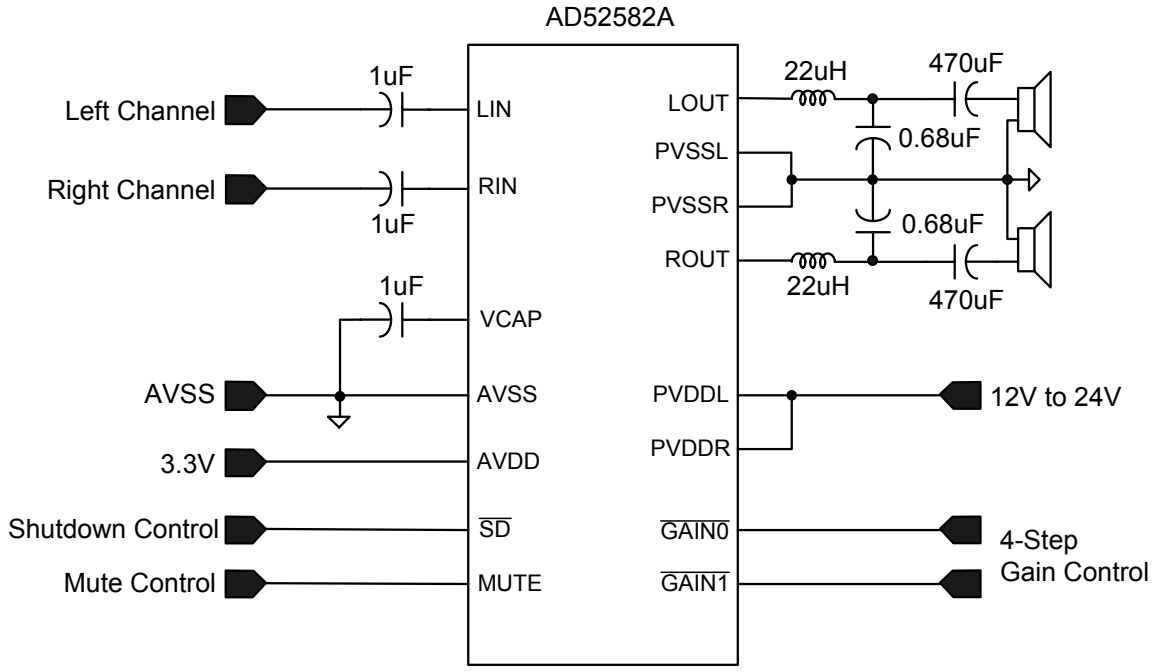
Description

The AD52582A is a high efficiency stereo class-D audio amplifier. The loudspeaker driver operates from 12~24V supply voltage and analog circuit operates at 3.3V supply voltage. It can deliver 20W/ch output power into 4Ω loudspeaker within 10% THD+N and without external heat sink.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20, 26, 32, 36 dB.

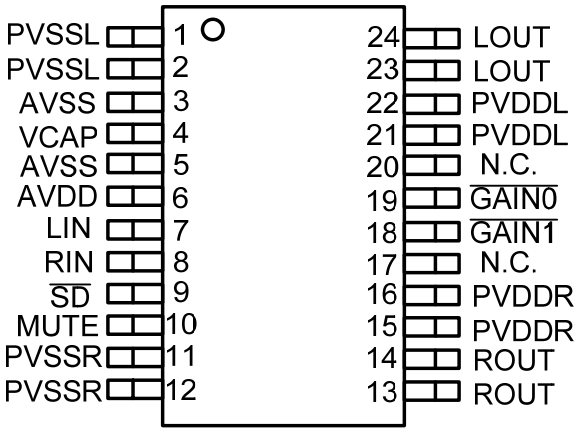
The AD52582A packaged as E-TSSOP 24L is a stereo audio amplifier with high efficiency and low thermal resistance which leads to no external heat sink requirement under 18.5W/ch output power.

Simplified Application Circuit



Pin Assignments

TSSOP PACKAGE
(TOP VIEW)



Pin Description

PIN	NAME	TYP	DESCRIPTION	CHARACTERISTIC
1,2	PVSSL	P	High-voltage ground for left channel	
3	AVSS	P	Low-voltage analog ground	
4	VCAP	O	Reference for amplifier inputs	Biased at PVDD/14.6
5	AVSS	P	Low-voltage analog ground	
6	AVDD	P	Low-voltage analog power supply	
7	LIN	I	Audio input for left channel	
8	RIN	I	Audio input for right channel	
9	$\overline{SD}$	I	Shutdown signal. Active low	Schmitt trigger TTL input buffer, internally pull low.
10	MUTE	I	Mute signal.	Schmitt trigger TTL input buffer, internally pull low.
11,12	PVSSR	P	High-voltage ground for right channel	
13,14	ROUT	O	Right channel output	
15,16	PVDDR	P	High-voltage power supply for right channel	
17	N.C.		Not connected	
18	$\overline{GAIN1}$	I	Gain select most-significant bit. Active low	Schmitt trigger TTL input buffer, internally pull high.
19	$\overline{GAIN0}$	I	Gain select least-significant bit. Active low	Schmitt trigger TTL input buffer, internally pull high.
20	N.C.		Not connected	
21,22	PVDDL	P	High-voltage power supply for left channel	
23,24	LOUT	O	Left channel output	
Thermal Pad		P	Must be soldered to PCB's ground plane	