Class-D Audio Power Amplifier with USB / I²S Interface and Recording function

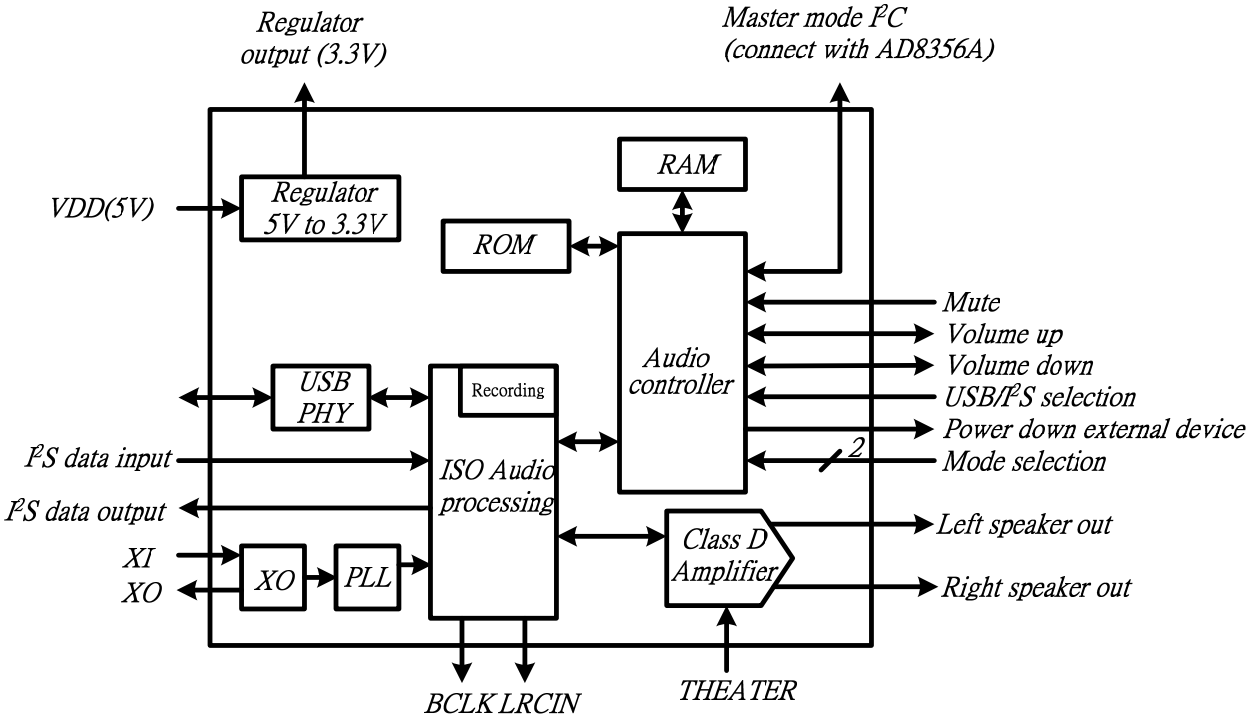
Features

- Compliant with USB Specification v1.1, and USB 2.0 full speed
- Embedded high efficiency, high performance class D stereo amplifier
- Support I²S input and I²S output interface of master mode
  Sampling frequencies(Fs)：48kHz
- +6dB enhancement(Theater function)
- Support recording function
- Support both bus-powered and self-powered operation
- Supports Win Me//2000/XP and MacOS
- True plug-and-play application, no driver is required for basic USB speaker application
- Support volume/mute control with external button
- Built-in 5V to 3.3V regulator for internal device operation
- Total efficiency
  80% for 8Ω load @ -1dB 1kHz sine wave input
- Loudspeaker PSNR & DR (A-weighting)
  80dB (PSNR), 78dB (DR) with Bead filter
  82dB (PSNR), 78dB (DR) with Chock filter
- Anti-pop design
- Over-temperature protection
- Under-voltage shutdown
- Short-circuit detection
- 12 MHz Crystal Input
- 32-pin LQFP(Pb free)

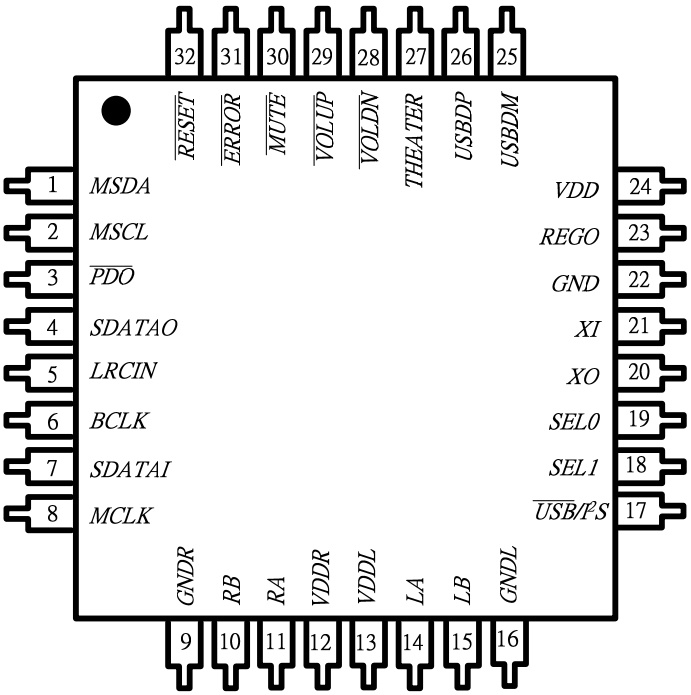
Description

AD6255A is a single chip of Class-D audio amplifier with USB/I²S interface and supports recording function. When using the power supplied from the USB port, AD6255A can drive a pair of up to 1W speakers due to the built-in, high efficiency and high performance class D amplifiers. The device also has an I²S input port and I²S output port. The I²S input port allows other external audio sources to use the class D amplifier to share the speakers. The I²S output port allows other high performance audio device (i.e. AD8356A/AD8256A) to be controlled by AD6255A.

Functional Block Diagram



Pin Assignment



Pin Description

Pin	Name	Type	Description	Characteristics
1	MSDA	I/O	I^2C's SDA of Master mode	Schmitt trigger TTL input buffer
2	MSCL	O	I^2C's SCL of master mode	
3	$\overline{PDO}$	O	Power-down output ***(Note1)***	
4	SDATAO	O	Serial audio output ***(Note1)***	
5	LRCIN	O	L/R clock output(Fs) ***(Note1)***	
6	BCLK	O	BCLK output(64xFs) ***(Note1)***	
7	SDATAI	I	Serial audio data input	Schmitt trigger TTL input buffer
8	MCLK	O	Master clock(256xFs)	
9	GNDR	P	Ground for right channel	
10	RB	O	Right channel output-	
11	RA	O	Right channel output+	
12	VDDR	P	Supply for right channel	
13	VDDL	P	Supply for left channel	
14	LA	O	Left channel output+	
15	LB	O	Left channel output-	