

12W Stereo/Mono Digital Audio Amplifier

Features

- 16/18/20/24-bit input with I²S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
Loudspeaker: 100dB (PSNR), 108dB (DR) @18V
- Multiple sampling frequencies (Fs)
32kHz / 44.1kHz / 48kHz and
64kHz / 88.2kHz / 96kHz and
128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
128x~512x Fs for 64kHz / 88.2kHz / 96kHz
64x~256x Fs for 128kHz/176.4kHz/192kHz
- Supply voltage
3.3V for digital circuit
12V~18V for loudspeaker driver
- Loudspeaker output power for 18V
2x10W into 8Ω@0.32% THD+N for stereo
1x20W into 4Ω@0.22% THD+N for mono
- Loudspeaker output power for 18V with proper cooling method
2x14W into 8Ω@1% THD+N for stereo
1x29W into 4Ω@1% THD+N for mono
- Anti-pop design

- Over-temperature protection
- Internal PLL
- Under-voltage shutdown
- Over-current protection
- I²C control interface

Applications

- CD and DVD
- TV audio
- Car audio
- Boom-box
- MP3 docking systems
- Powered speaker
- Wireless audio
- USB speaker

Description

This is a stereo (8Ω)/mono (4Ω) fully digital audio amplifier with output power which can drive up to 2x12W for stereo or 1x24W for mono at 18V supply voltage, no external heat-sink or fan is requirement.

Using I²C digital control interface, AD82571B provides input format selection, mute and volume control function. Protection circuits are provided to protect AD82571B damage while connection error.

ORDERING INFORMATION

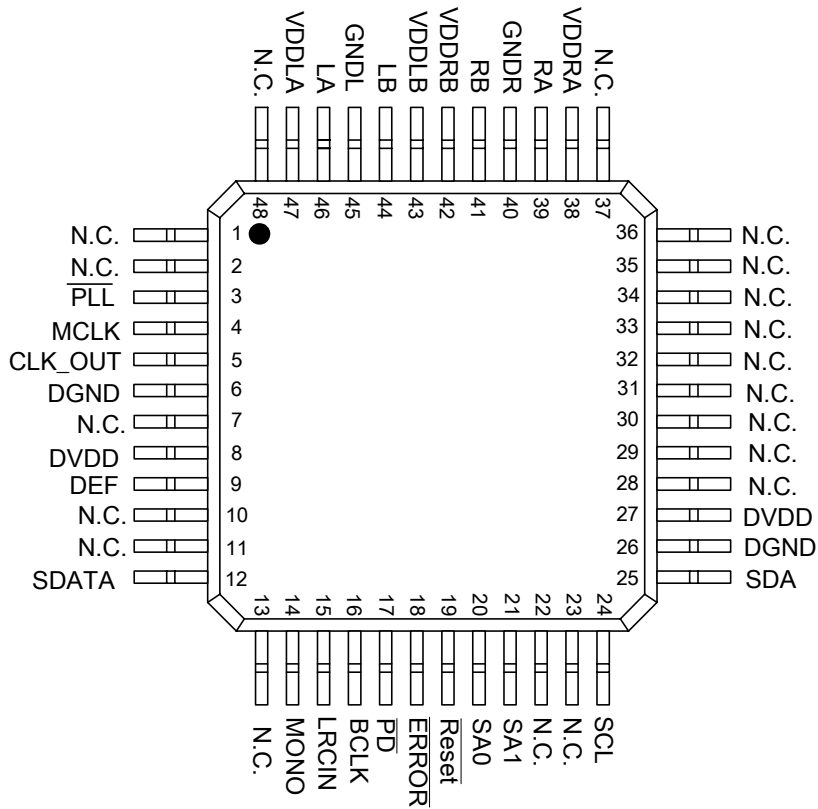
| Product Number | Package | Comments |
|----------------|----------------|----------|
| AD82571B-LEG | 7x7 48L E-LQFP | Pb-free |

MARKING INFORMATION



- Line 1 : LOGO
- Line 2 : Product No
- Line 3 : Tracking Code
- Line 4 : Date Code

Pin Assignment



Pin Description

| PIN | NAME | TYPE | DESCRIPTION | CHARACTERISTICS |
|-----|-------------------------|------|----------------------------------|----------------------------------|
| 1 | N.C. | | | |
| 2 | N.C. | | | |
| 3 | $\overline{\text{PLL}}$ | I | PLL enable, low active | Schmitt trigger TTL input buffer |
| 4 | MCLK | I | Master clock input | Schmitt trigger TTL input buffer |
| 5 | CLK_OUT | O | Clock output from PLL | TTL output buffer |
| 6 | DGND | P | Digital Ground | |
| 7 | N.C. | | | |
| 8 | DVDD | P | Digital Power | |
| 9 | DEF | I | Default volume setting | Schmitt trigger TTL input buffer |
| 10 | N.C. | | | |
| 11 | N.C. | | | |
| 12 | SDATA | I | Serial audio data input | Schmitt trigger TTL input buffer |
| 13 | N.C. | | | |
| 14 | MONO | I | MONO mode enable, high active | Schmitt trigger TTL input buffer |
| 15 | LRCIN | I | Left/Right clock input (F_s) | Schmitt trigger TTL input buffer |
| 16 | BCLK | I | Bit clock input (64 F_s) | Schmitt trigger TTL input buffer |
| 17 | $\overline{\text{PD}}$ | I | Power down, low active | Schmitt trigger TTL input buffer |