2x15W Stereo / 1x30W Mono Digital Audio Amplifier

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting)
  Loudspeaker: 97dB (PSNR), 105dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz/176.4kHz/192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for 24V
  10W x 2CH into 8Ω @0.27% THD+N for stereo
  15W x 2CH into 8Ω @0.35% THD+N for stereo
  20W x 1CH into 4Ω @0.25% THD+N for mono
  30W x 1CH into 4Ω @0.32% THD+N for mono
- Anti-pop design
- Over-temperature protection
- Internal PLL
- Under-voltage shutdown
- Over-current protection
- I^2C control interface
- Zero detection
- Power limit function
- Quaternary and ternary switch

Applications

- CD and DVD
- LCD TV
- Car audio
- Boom-box
- MP3 docking systems
- Powered speaker
- Wireless audio
- USB speaker

Description

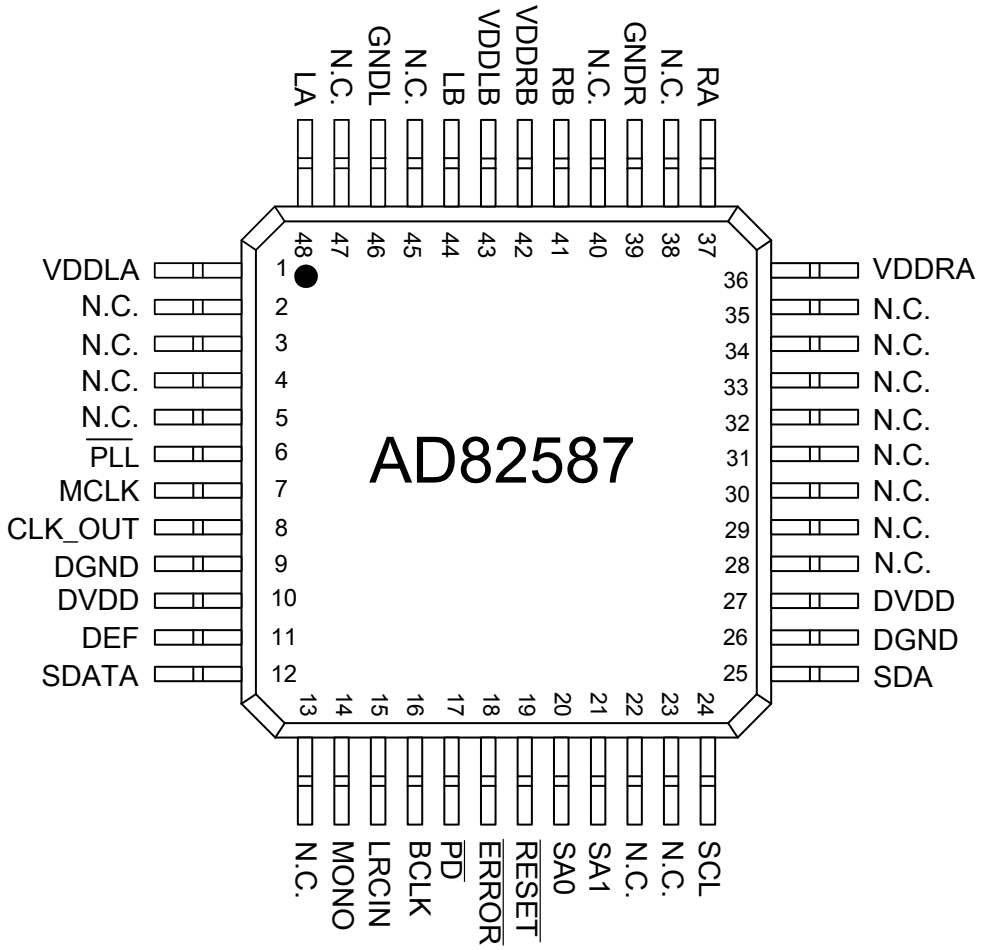
AD82587 is a digital audio amplifier capable of driving a pair of 8Ω,15W or a single 4Ω,30W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587's input format selection, mute and volume control functions. AD82587 has many built-in protection circuits to safeguard AD82587 from connection errors.

ORDERING INFORMATION

Product ID	Package	Packing / MPQ	Comments
AD82587-LE48NAY	E-LQFP-48L 7x7 mm	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box)	Green
AD82587-LE48NAR	E-LQFP-48L 7x7 mm	2K Units Tape and Reel	Green

Pin Assignment

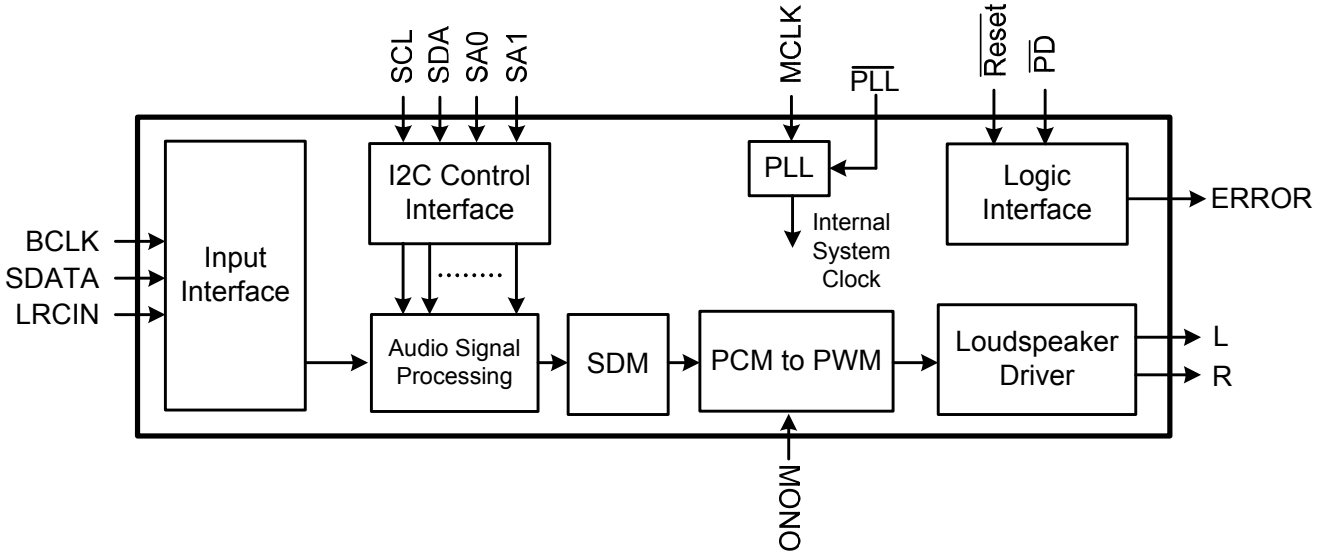


Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	VDDLA	P	Left channel supply A	
2	N.C.	NC		
3	N.C.	NC		
4	N.C.	NC		
5	N.C.	NC		
6	$\overline{PLL}$	I	PLL enable, low active	Schmitt trigger TTL input buffer
7	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
8	CLK_OUT	O	Clock output from PLL	TTL output buffer
9	DGND	P	Digital Ground	
10	DVDD	P	Digital Power	
11	DEF	I	Default volume setting	Schmitt trigger TTL input buffer
12	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
13	N.C.	NC		

14	MONO	I	MONO mode enable, high active	Schmitt trigger TTL input buffer
15	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
16	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
17	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
18	$\overline{ERROR}$	O	Error status, low active	Open-drain output
19	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
20	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
21	SA1	I	I^2C select address 1	Schmitt trigger TTL input buffer
22	N.C.	NC		
23	N.C.	NC		
24	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
25	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
26	DGND	P	Digital Ground	
27	DVDD	P	Digital Power	
28	N.C.	NC		
29	N.C.	NC		
30	N.C.	NC		
31	N.C.	NC		
32	N.C.	NC		
33	N.C.	NC		
34	N.C.	NC		
35	N.C.	NC		
36	VDDRA	P	Right channel supply A	
37	RA	O	Right channel output A	
38	N.C.	NC		
39	GNDR	P	Right channel ground	
40	N.C.	NC		
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	
43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	N.C.	NC		
46	GNDL	P	Left channel ground	
47	N.C.	NC		
48	LA	O	Left channel output A	

Functional Block Diagram



Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jc}(℃/W)	Exposed Thermal Pad
7x7 48L E-LQFP	AD82587	27.4	1.33	6.0	Yes (Note1)
7x7 48L QFN		23.7	0.09	5.1	

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jc} represents the heat resistance for the heat flow between the chip and the package's top surface.

Note 1.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the exposed pad's center.

Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_a	Ambient Operating Temperature	0	70	°C

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_a	Ambient Operating Temperature	0~70	°C

Digital Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
V_{OH}	High-Level Output Voltage	2.4			V
V_{OL}	Low-Level Output Voltage			0.4	V
C_I	Input Capacitance		6.4		pF

General Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V			10	uA
I_{PD}(LV)	DVDD Supply Current during Power Down	DVDD=3.3V			10	uA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		°C
	Temperature Hysteresis for Recovery from Shutdown			40		°C
UV_H	Under Voltage Disabled (For DVDD)			2.8		V
UV_L	Under Voltage Enabled (For DVDD)			2.7		V
Rds-on	Static Drain-to-Source On-state Resistor, PMOS	PVDD=24V, Id=500mA		295		mΩ
	Static Drain-to-Source On-state Resistor, NMOS			185		mΩ
I_{SC}	LI Channel Over-Current Protection (Note 2)	PVDD=24V		5		A
	Mono Channel Over-Circuit Protection (Note 2)	PVDD=24V		10		A

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Marking Information

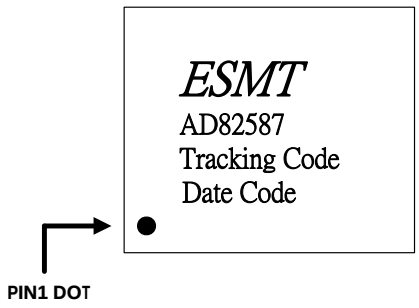
AD82587

Line 1 : LOGO

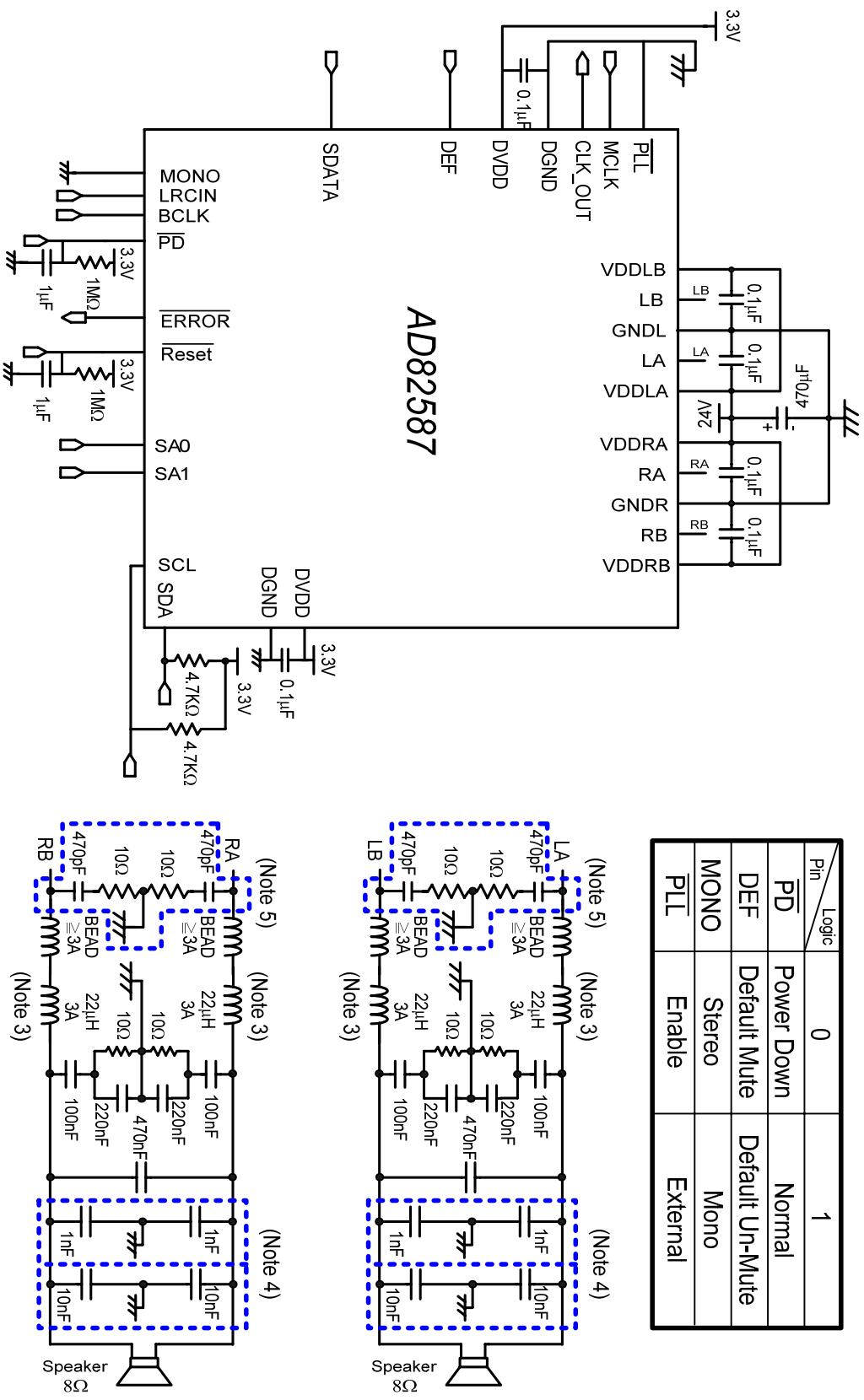
Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code



Application Circuit Example for Stereo



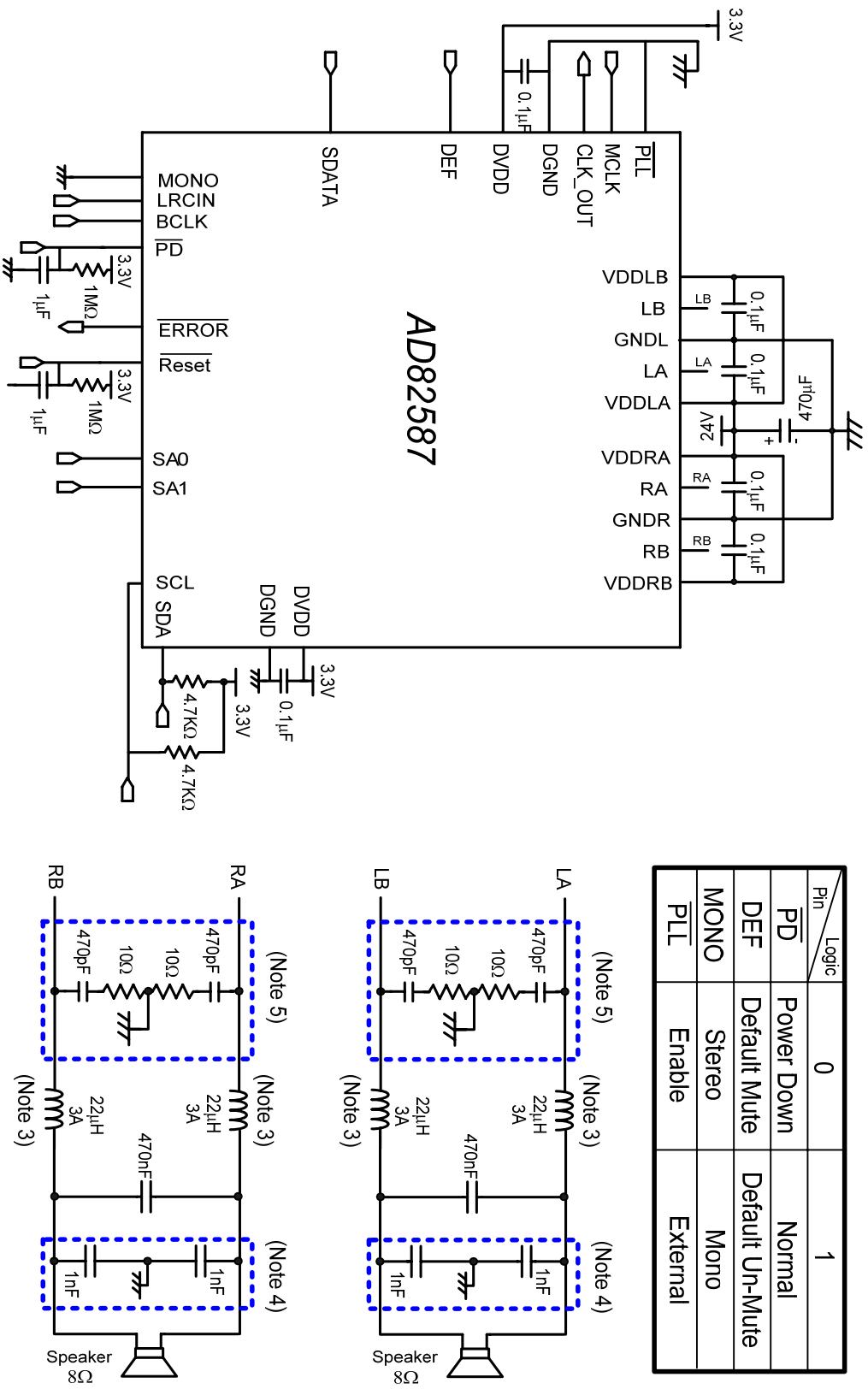
Pin / Logic	0	1
$\overline{PD}$	Power Down	Normal
DEF	Default Mute	Default Un-Mute
MONO	Stereo	Mono
$\overline{PLL}$	Enable	External

Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 4A.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit can be removed while the PVDD <=18V.

Application Circuit Example for Stereo (Economic type, moderate EMI suppression)



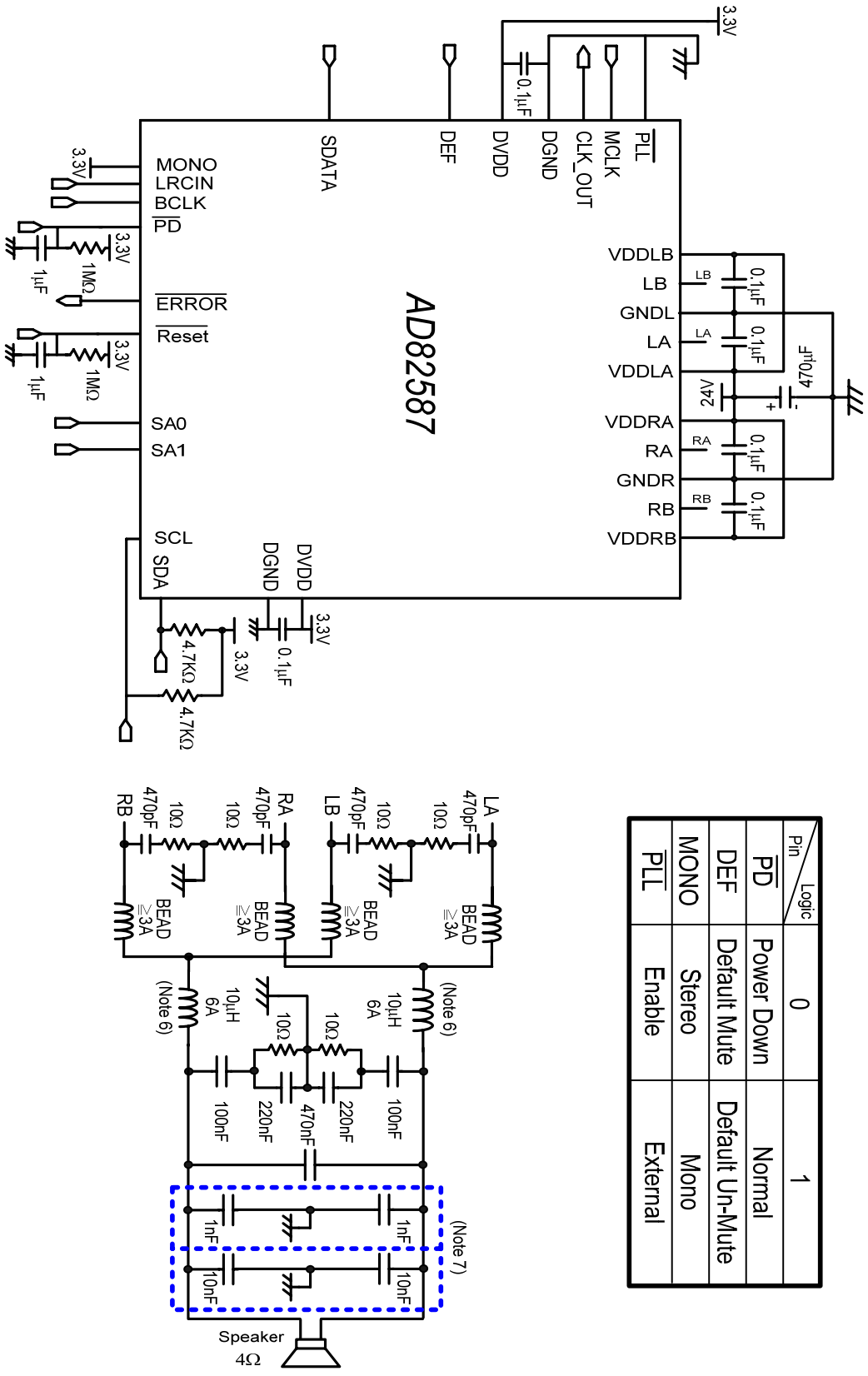
Pin / Logic	0	1
$\overline{PD}$	Power Down	Normal
DEF	Default Mute	Default Un-Mute
MONO	Stereo	Mono
$\overline{PLL}$	Enable	External

Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 4A.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit can be removed while the PVDD <=18V.

Application Circuit Example for Mono



Pin / Logic	0	1
PD	Power Down	Normal
DEF	Default Mute	Default Un-Mute
MONO	Stereo	Mono
PLL	Enable	External

Note 6: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 8A.

Note 7: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Electrical Characteristics and Specifications for Loudspeaker

● Stereo output with 24V supply voltage

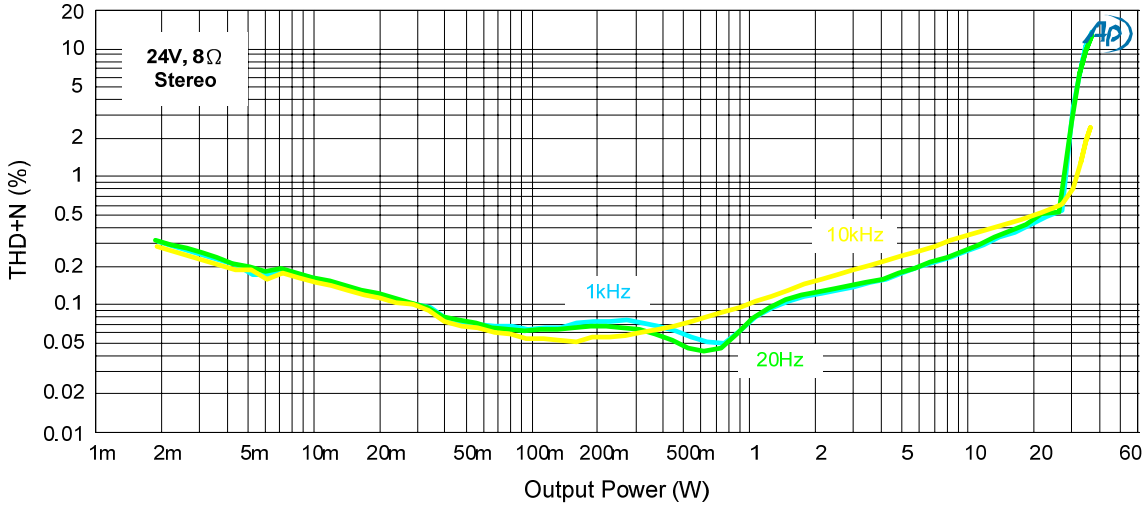
Condition: DVDD=3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=8Ω with passive LC low-pass filter (L=22 μH with R_{DC}=0.12Ω, C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.35%)	+8dB volume			15		W
	RMS Output Power (THD+N=0.27%)	+8dB volume			10		W
THD+N	Total Harmonic Distortion + Noise		-1dB		0.46		%
SNR	Signal to Noise Ratio (Note 8)		-1dB		97		dB
DR	Dynamic Range (Note 8)		-60dB		105		dB
PSRR	Power Supply Rejection Ratio		-60dB		59		dB
	Channel Separation		-1dB		73		dB

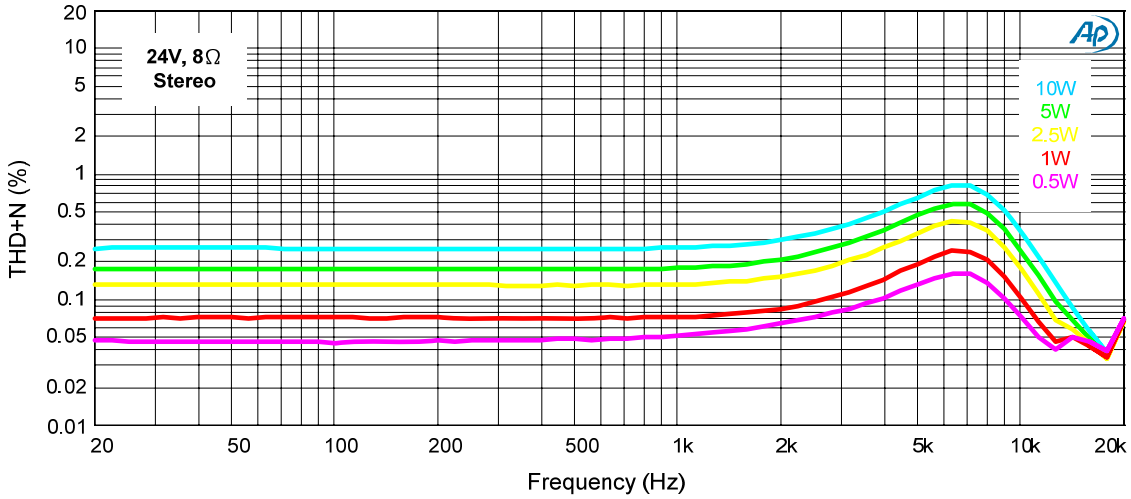
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for the larger RMS output power.

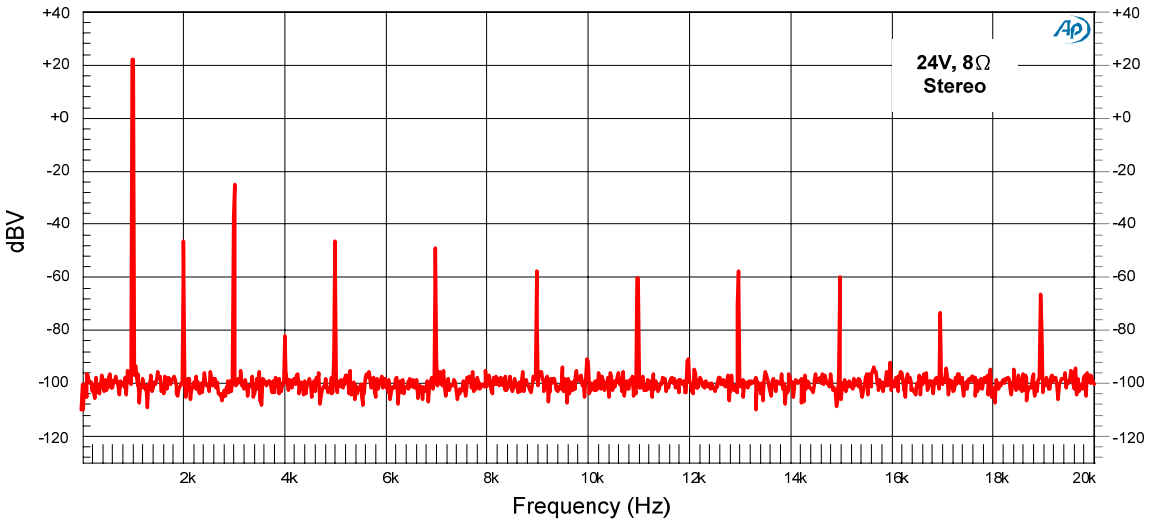
Total Harmonic Distortion + Noise vs. Output Power (Stereo)



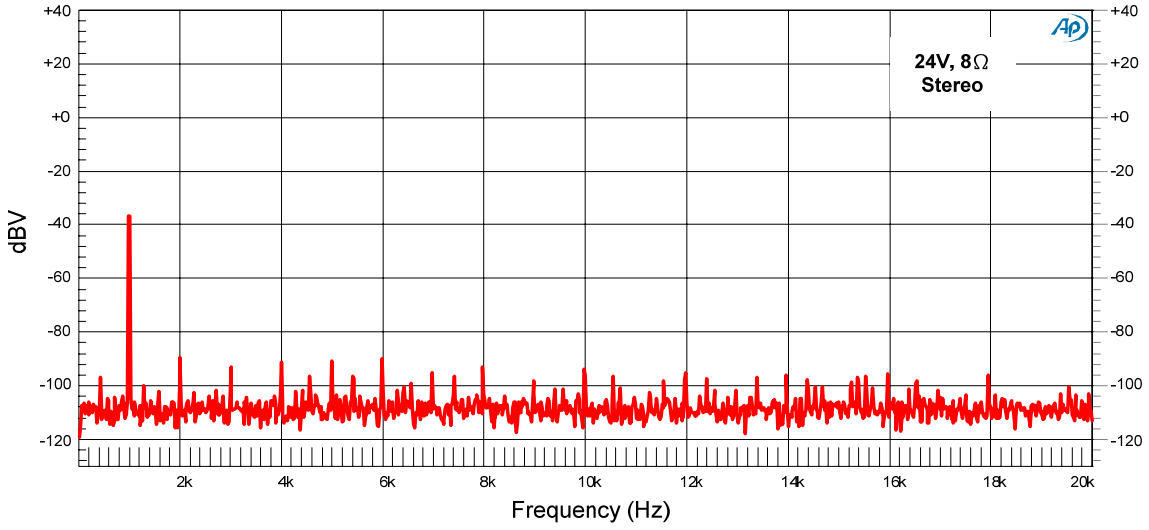
Total Harmonic Distortion + Noise vs. Frequency (Stereo)



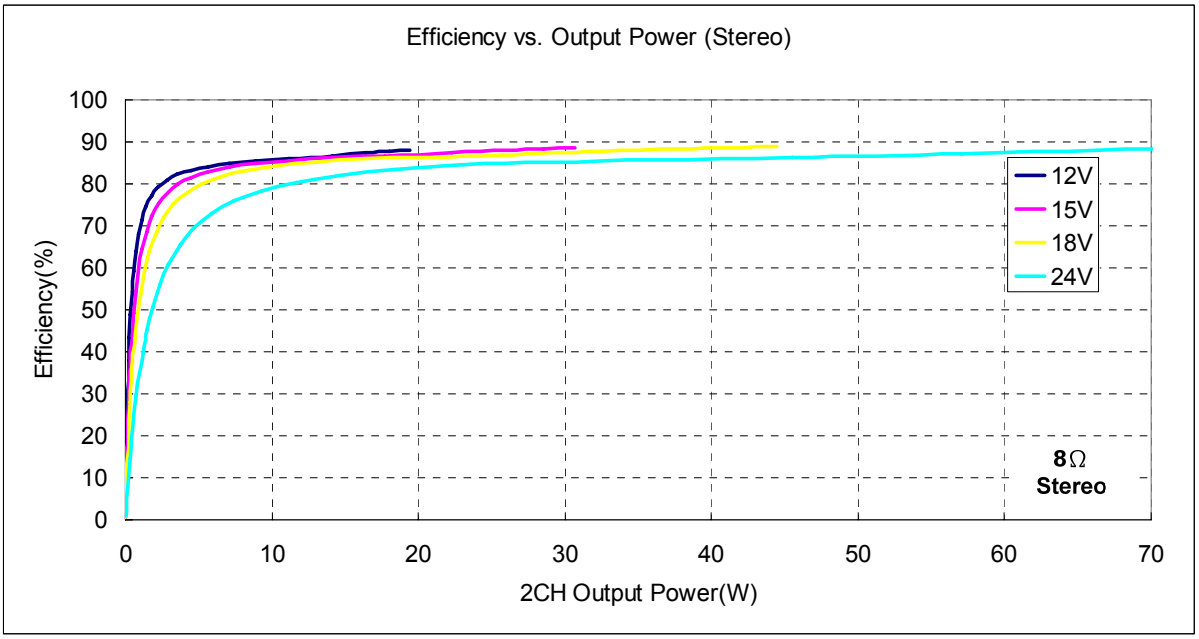
Spectrum at Peak SNR (Stereo)



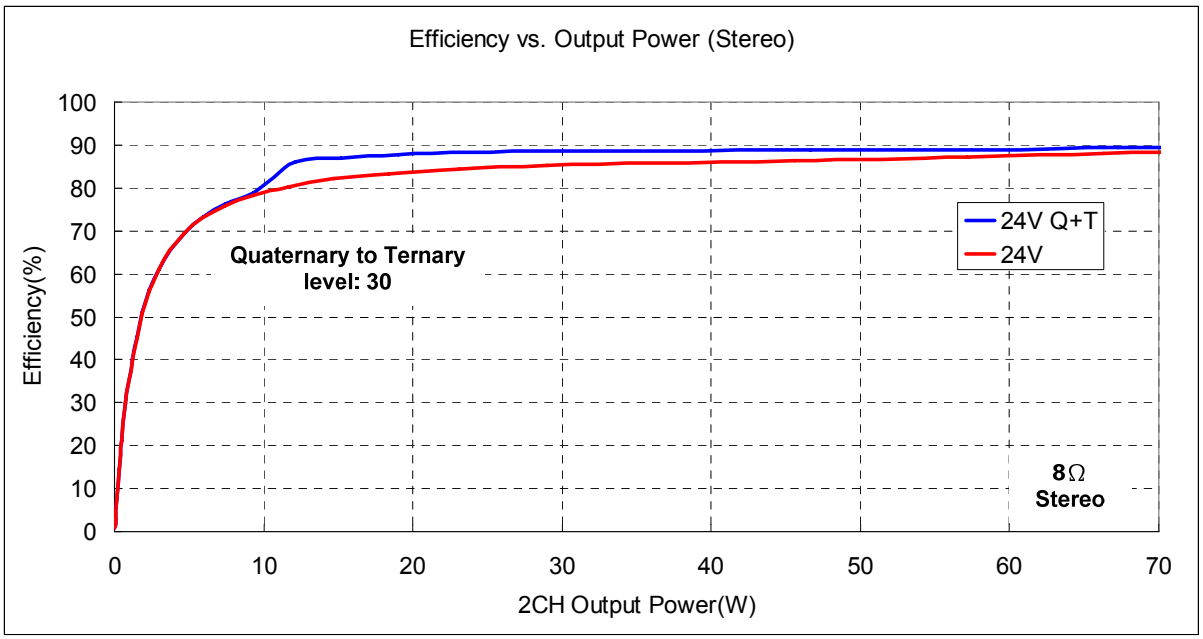
Spectrum at -60dB Signal Input Level (Stereo)



Efficiency (Stereo)



Efficiency (Stereo) for PWM of "Quaternary" and "Q+T" Modulation



Electrical Characteristics and Specifications for Loudspeaker

- **Mono output with 24V supply voltage**

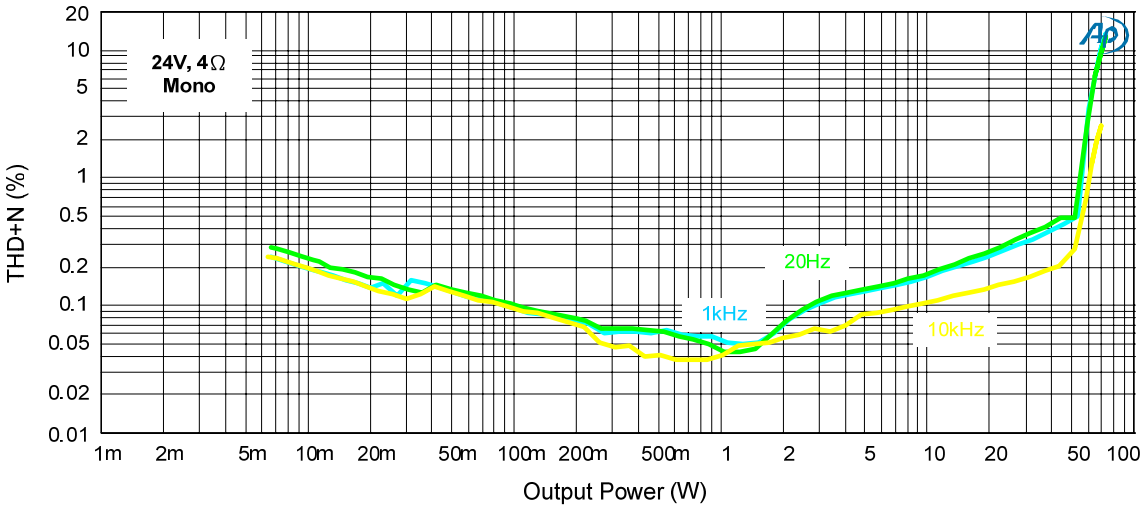
Condition: DVDD=3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=4Ω with passive LC low-pass filter (L=10 μH with R_{DC}=0.12Ω, C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.32%)	+8dB volume			30		W
	RMS Output Power (THD+N=0.25%)	+8dB volume			20		W
THD+N	Total Harmonic Distortion + Noise		-1dB		0.4		%
SNR	Signal to Noise Ratio (Note 8)		-1dB		97		dB
DR	Dynamic Range (Note 8)		-60dB		105		dB
PSRR	Power Supply Rejection Ratio		-60dB		59		dB

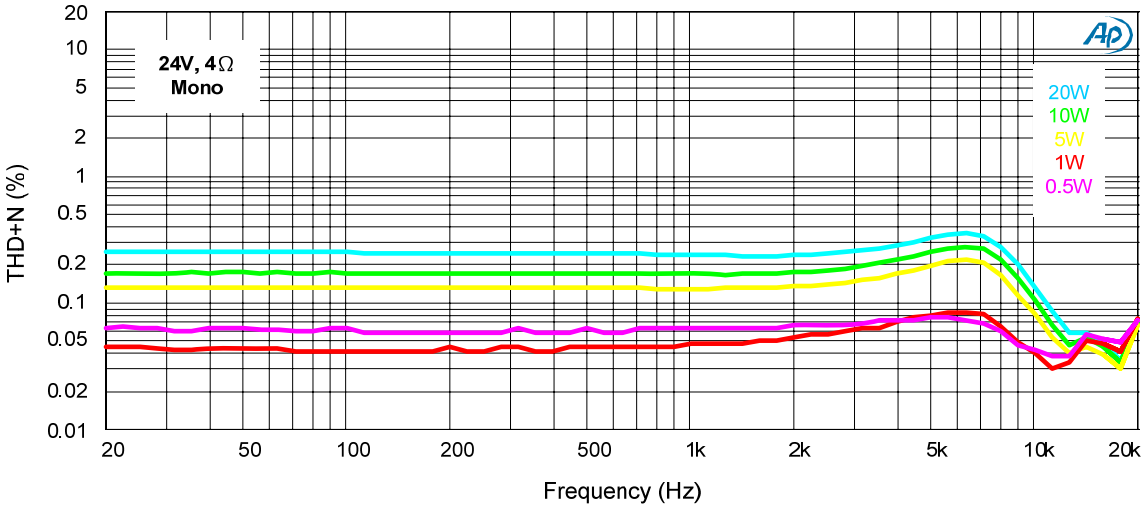
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for the larger RMS output power.

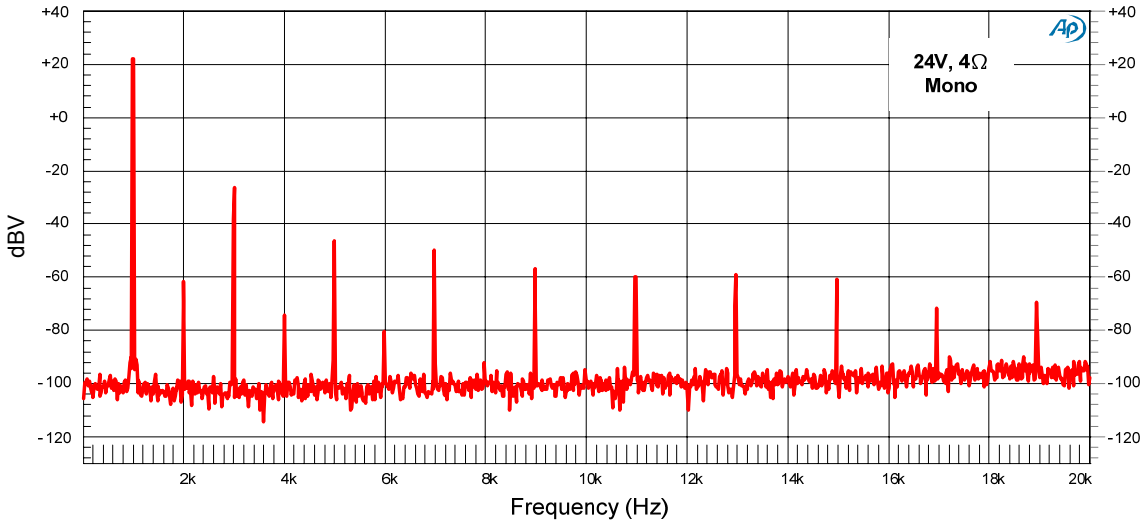
Total Harmonic Distortion + Noise vs. Output Power (Mono)



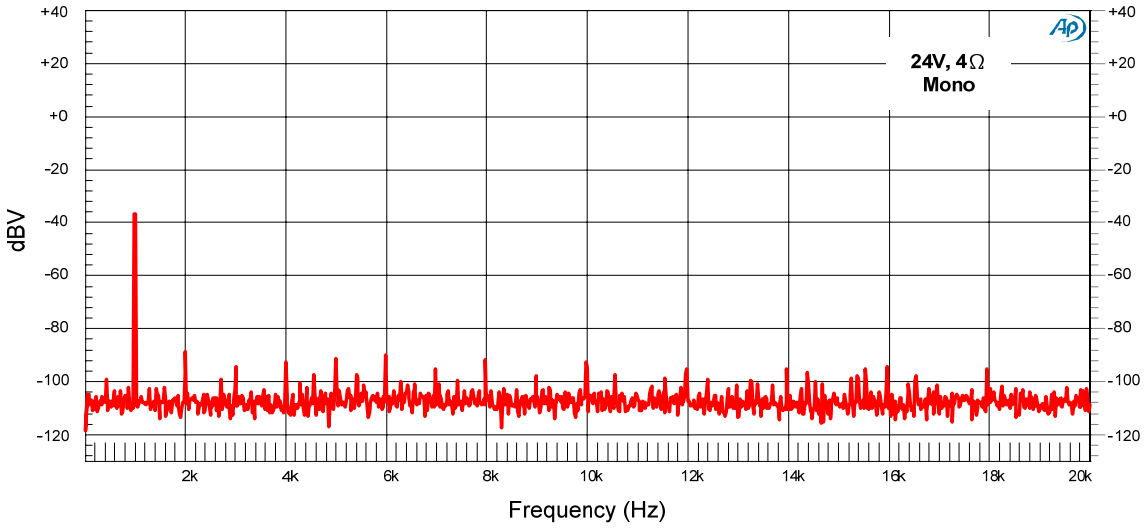
Total Harmonic Distortion + Noise vs. Frequency (Mono)



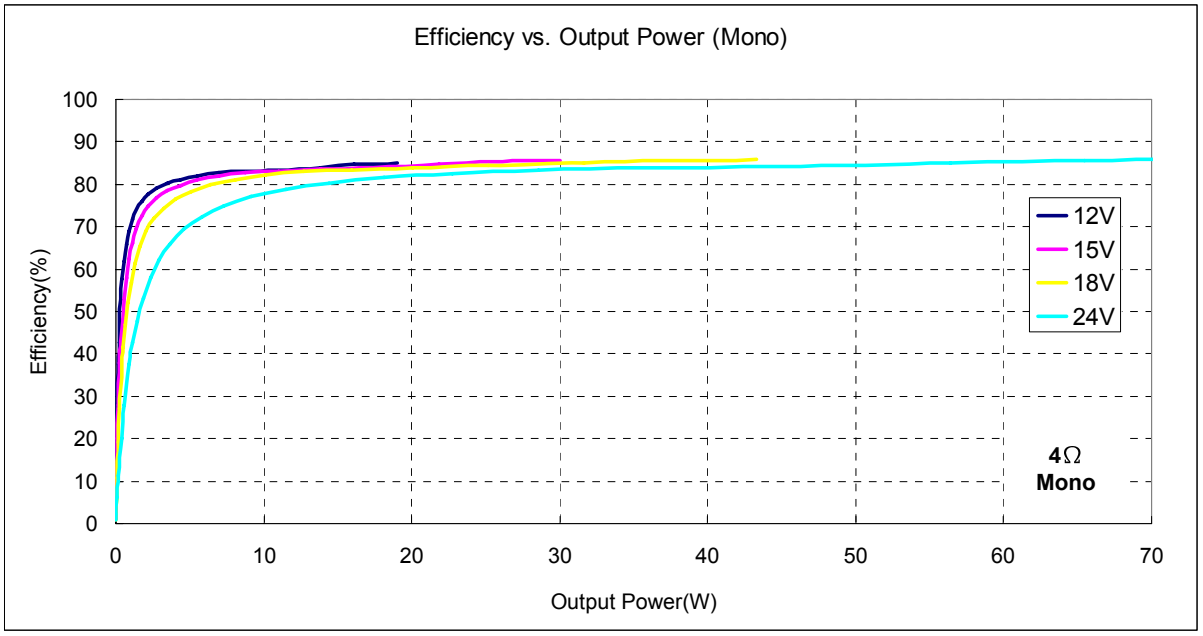
Spectrum at Peak SNR (Mono)



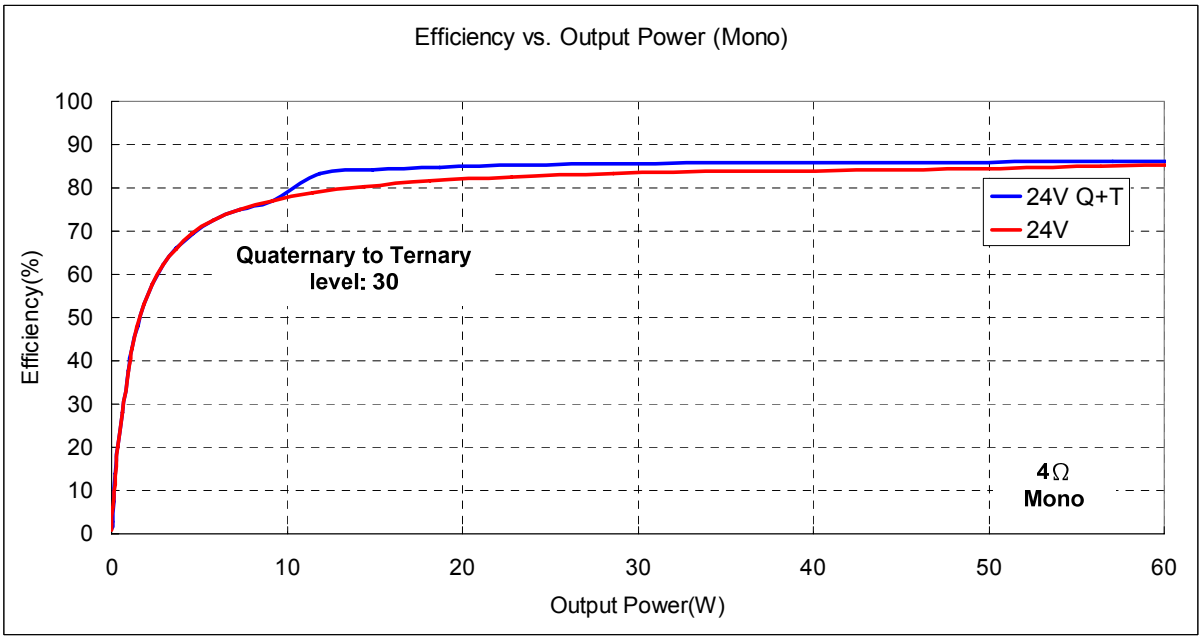
Spectrum at -60dB Signal Input Level (Mono)



Efficiency (Mono)

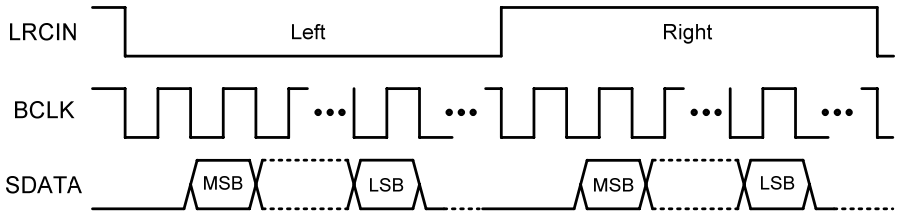


Efficiency (Mono) for PWM of "Quaternary" and "Q+T" Modulation

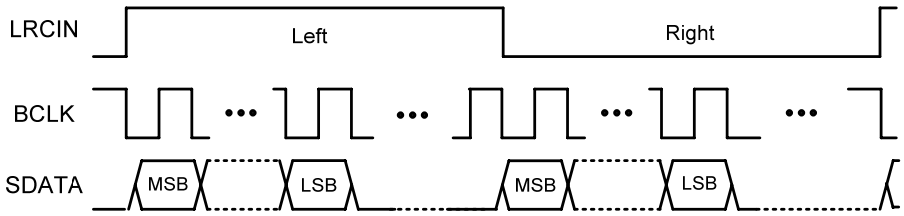


Interface Configuration

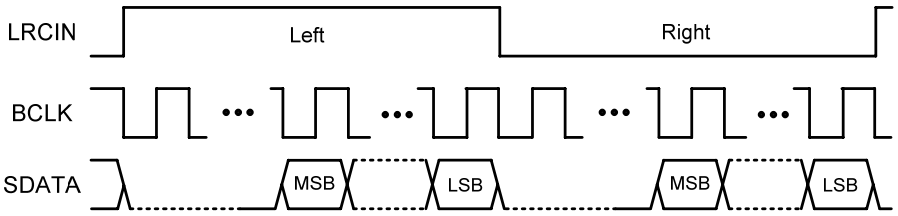
- I^2S



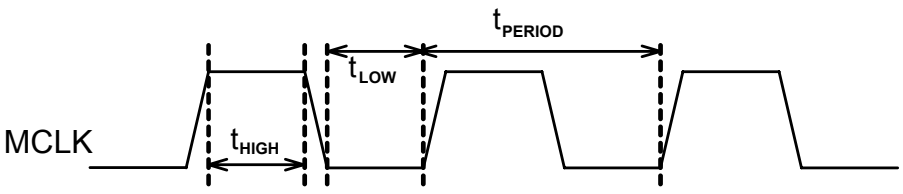
- Left-Alignment



- Right-Alignment

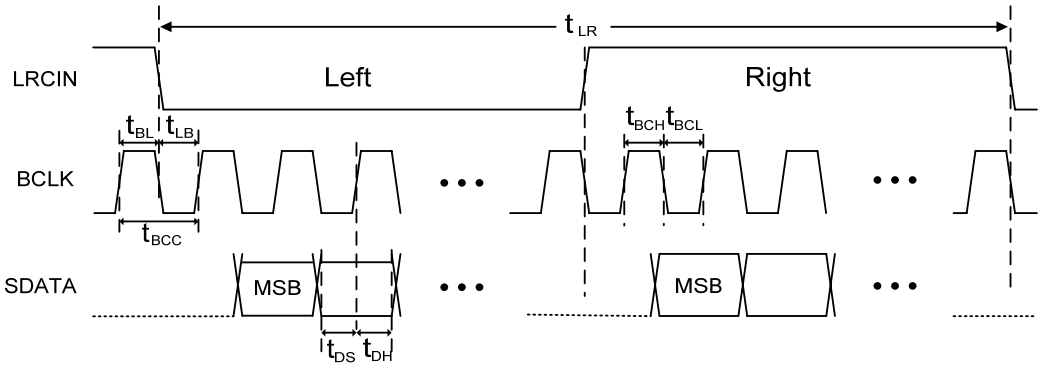


- System Clock Timing



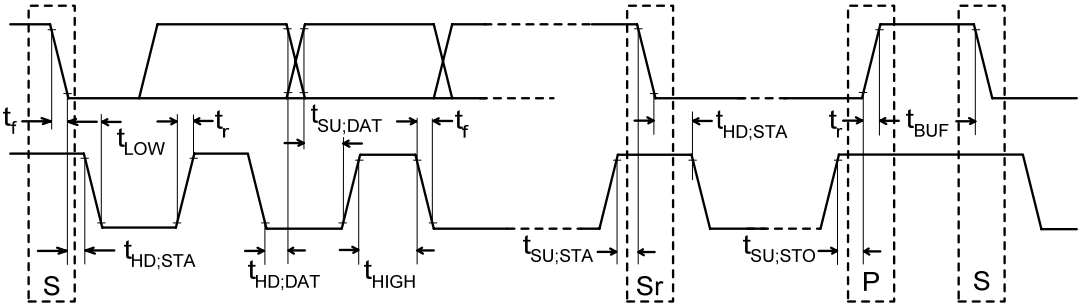
$t_{HIGH} \geqq 10.1ns$, $t_{LOW} \geqq 10.1ns$, $t_{PERIOD} \geqq 20.2ns$

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	81.38		244	ns
t_{BCL}	BCLK Pulse Width Low	81.38		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I_2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SDL signals	t_r	---	1000	20+0.1Cb	300	ns
Fall time of both SDA and SDL signals	t_f	---	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	---	$0.1V_{DD}$	---	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	---	$0.2V_{DD}$	---	V

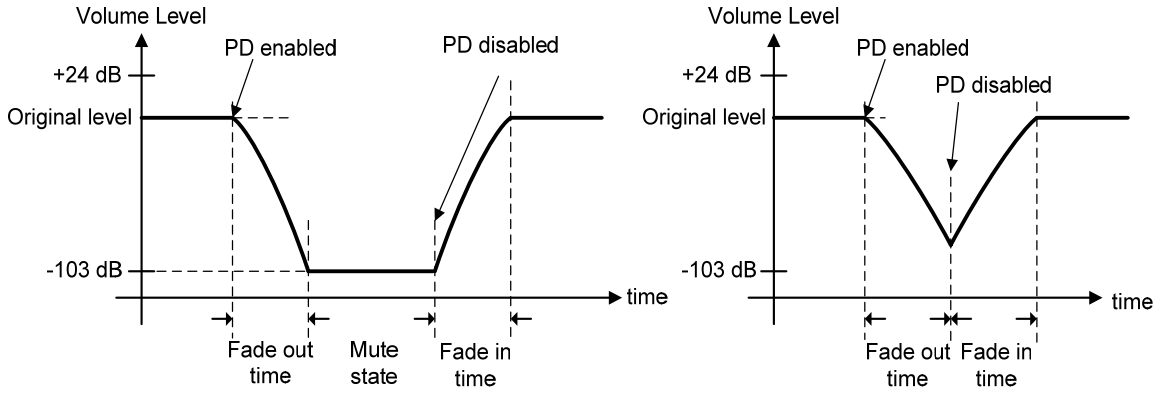
Operation Description

- Reset

When the $\overline{\text{RESET}}$ pin is lowered, AD82587 will clear the stored data and reset the register table to default values. AD82587 will exit reset state at the 256th MCLK cycle after the $\overline{\text{RESET}}$ pin is raised to high.

- Power down control

AD82587 has a built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD82587 will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After PD pin is pulled low, AD82587 requires 128[maximum (Gain-1)/(1dB/step)] LRCIN clocks to finish the forementioned work before entering power down state. Users can not program AD82587 during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal is removed during the fade-out procedure (above, right figure), AD82587 will still execute the fade-in procedure. In addition, AD82587 will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD82587 will return to its normal status.

- Internal PLL ($\overline{\text{PLL}}$)

AD82587 has a built-in PLL with multiple MCLK/FS ratio, which is selected by I^2C control interface. If $\overline{\text{PLL}}$ pin is pulled low, the built-in PLL is enabled; if $\overline{\text{PLL}}$ pin is pulled high, an external clock source for MCLK less than 50MHz should be provided. The MCLK/FS ratio will be fixed at 1024x, 512x, or 256x with a sample frequency of 48kHz, 96kHz, or 192kHz respectively.

- Anti-pop design

AD82587 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- Default volume (DEF)

The volume of AD82587 is +8dB when DEF pin is high, and the volume is muted when DEF pin low. When using AD82587 without I2C control interface, user should set the pin high. The user can change the values of the register table setting for volume control. For detailed information, refer to the register table section.

- Self-protection circuits

AD82587 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

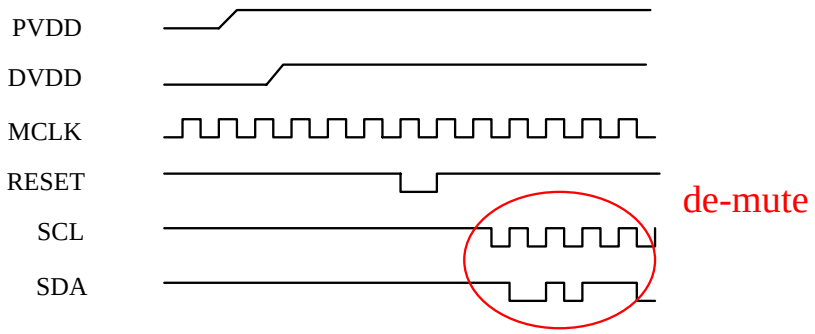
(i) When the internal junction temperature is higher than 160℃, power stages will be turned off and AD82587 will return to normal operation once the temperature drops to 120℃. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 24V operations, the current flowing through the power stage will be less than 5A for stereo configuration or less than 10A for mono configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state. Once the over-temperature or short-circuit condition is removed, AD82587 will exit ERROR state when one of the following conditions is met: (1) $\overline{\text{RESET}}$ pin is pulled low, (2) $\overline{\text{PD}}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 2.7V, AD82587 will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes larger than 2.8V, AD82587 will return to normal operation.

- Power on sequence

Hereunder is AD82587's power on sequence. Please note that we suggested users set DEF pin at low state initially, and than give a de-mute command via I^2C when the whole system is stable.



Note. Set DEF pin at low state initially

I²C-Bus Transfer Protocol

- Introduction

  AD82587 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD82587 is always an I²C slave device.

- Protocol

  - START and STOP condition

    START is identified by a high to low transition of the SDA signal.. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD82587 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

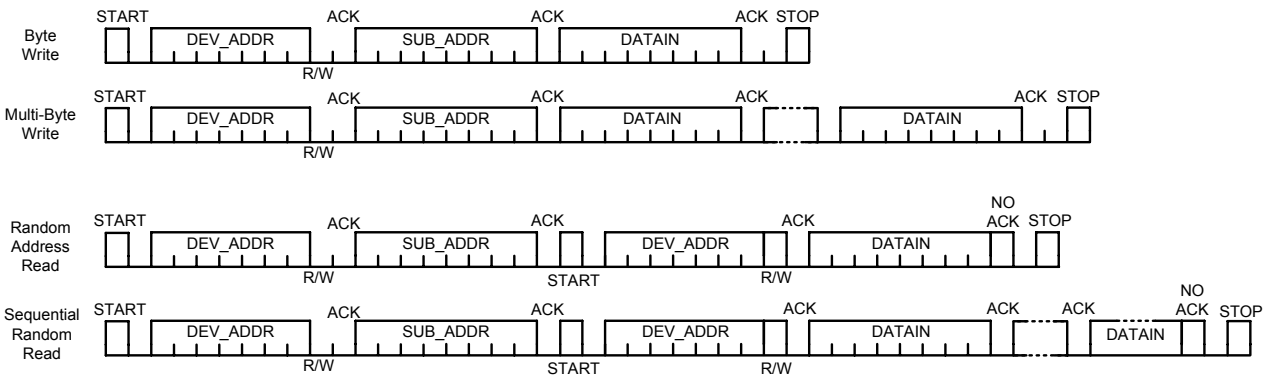
    The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD82587 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

    The master generates 7-bit address to recognize slave devices. When AD82587 receives 7-bit address matched with 0110x0y (where x and y can be selected by external SA0 and SA1 pins, respectively), AD82587 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD82587 internal sub-addresses.

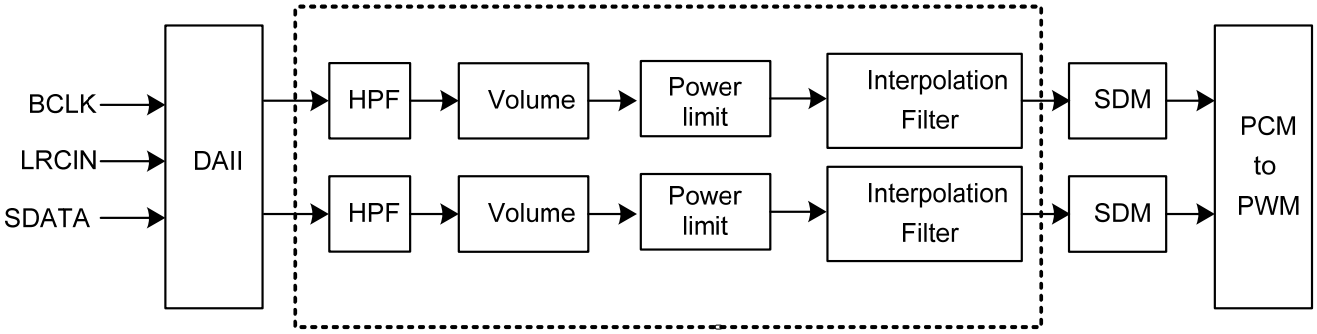
  - Data transferring

    Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD82587 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



Register Table

The AD82587's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.



Audio Signal Processing

Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0	State Control 1	IF[2]	IF[1]	IF[0]	LR_SEL	PWML_X	PWMR_X	PwmMode	Zero-detect
1	State Control 2	X	X	FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]
2	State Control 3	EN_CLKO	HF	X	X	MUTE	CM1	CM2	CompSDMEn
3	Master Volume	X	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
4	Channel1 Volume	X	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
5	Channel2 Volume	X	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
6	HV UV selection	X	X	X	X	HVUVSEL[3]	HVUVSEL[2]	HVUVSEL[1]	HVUVSEL[0]
7	Power limit level	X	X	X	PL_EN	PLL[3]	PLL[2]	PLL[1]	PLL[0]
8	Attack – Release rate	X	X	X	X	A_R[1]	A_R[0]	R_R[1]	R_R[0]
9	PWM mode switch	X	X	X	QTS[4]	QTS[3]	QTS[2]	QTS[1]	QTS[0]

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

- Address 0 : State control 1

  AD82587 supports multiple serial data input formats, including I^2S, Left-alignment and Right-alignment. The format is selected by users via bit7~bit5 of address 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			other	Reversed
B[4]	LR_SEL	Select Left or Right channel in MONO mode	0	Left channel
			1	Right channel
B[3]	PWML_X	LA/LB exchange	0	No exchange
			1	Exchange
B[2]	PWMR_X	RA/RB exchange	0	No exchange
			1	Exchange
B[1]	PwmMode	PWM modulation	0	Quarternary+Ternary
			1	Quarternary
B[0]	ZD_EN	Zero detect	0	Disable
			1	Enable

- Address 1 : State control 2

AD82587 has a built-in PLL, which can be bypassed by pulling the $\overline{PLL}$ pin High. When PLL is enabled, multiple MCLK/FS ratios are supported. Detail setting is shown in the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	X	Reserved		
B[5:4]	FS	Sampling Frequency	00	32/44.1/48kHz
			01	32/44.1/48kHz
			10	64/88.2/96kHz
			11	96/176.4/192kHz

Multiple MCLK/FS ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[5:4]=00/01	B[5:4]=10	B[5:4]=11
B[3:0]	PMF[3:0]	Multiple MCLK/FS ratio setting	0001	Reset Default (256x)	Reset Default (128x)	Reset Default (64x)
			0010	512x	256x	128x
			0011	768x	384x	192x
			0100	1024x	512x	256x

- Address 2 : State control 3

To prevent the DC current from damaging the speaker, a high pass filter (3dB frequency = 5Hz) is built into the AD82587. It can be enabled or disabled by bit 6 of address 2.

AD82587 has a mute function which includes master mute and individual channel mute modes. When the master mute mode is enabled, both left and right processing channels are muted. On the other hand, either channel can be muted by using the channel mute mode. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

The default settings of B[3:1] are determined by DEF pin. When DEF pin is pulled low or high, the default setting is muted or unmated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	EN_CLK_ OUT	PLL Clock Output	0	Disabled
			1	Enabled
B[6]	HF	High-Pass Filter	0	5Hz
			1	Disabled
B[5]	X	Reserved		
B[4]	X	Reserved		
B[3]	MUTE	Master Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[2]	CM1	Channel 1 Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[1]	CM2	Channel 2 Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[0]	CompSDMEn	Compensate SDM frequency response	0	Disable
			1	Enable

- Address 3 : Master Volume Control

AD82587 supports both master-volume (Address 3) and channel-volume control (Address 4 and 5) modes. Both volume control settings range from +12dB ~ -102dB. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

-102dB ≦ Total Volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	MV[6:0]	Master Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0000100	+8dB
			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110010	-102dB
			1110011	-∞dB
			:	:
			1111111	-∞dB

- Address 4 : Channel1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	C1V[6:0]	Channel 1 Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0000100	+8dB
			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110010	-102dB
			1110011	-∞dB
			:	:
			1111111	-∞dB

- Address 5 : Channel2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6:0]	C2V[6:0]	Channel 2 Volume	0000000	+12dB
			0000001	+11dB
			:	:
			0000100	+8dB
			:	:
			0001100	0dB
			0001101	-1dB
			:	:
			1110010	-102dB
			1110011	-∞dB
			:	:
			1111111	-∞dB

- Address 6 : Under Voltage selection for high voltage supply

The under-voltage detection level is programmable via bit3~ bit0. Once the output stage voltage drops below the preset value (see table), AD82587 will fade out audio signals to turn off the speaker.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	X	Reserved		
B[3:0]	HVUVSEL[3:0]	HV Under Voltage selection (Active)	Other	9.7V
			1100	19.5V
			0100	15.5V
			0011	13.2V
			0001	9.7V
			0000	8.2V

- Address 7 : Power Limit Level

Users can enable or disable the power limit function via bit4. If this function is enabled, users can select power limit level via bit3~ bit0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4]	PL_EN	Power limit enable	0	Disable
			1	Enable
B[3:0]	CHX[3:0]	Power limit level	0000	0dB
			0001	-2dB
			0010	-3dB
			0011	-5dB
			0100	-6dB
			0101	-8dB
			0110	-10dB
			0111	-15dB
			1000	-18dB
			1001	-25dB
			1010	-28dB
			1011	-35dB

- Address 8 : Attack rate and Release rate

When the power limit function is enabled, the volume of the amplifier will be adjusted to the pre-defined maximum value. When the audio signal after volume control processing exceeds the pre-defined maximum value, the volume gain will be set to a smaller value according to the attack rate (volume reducing rate). When the audio signal after volume control processing is below the release threshold (2dB less than power limit level), AD82587 will increase the volume level according to the release rate (volume increasing rate).

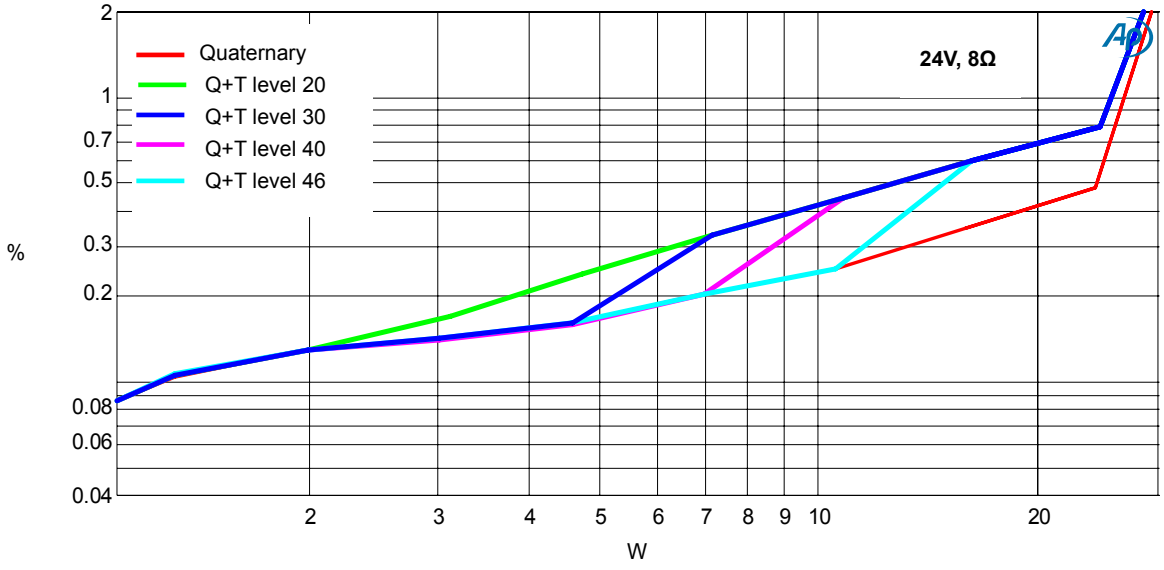
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	X	Reserved		
B[3:2]	A_Rate	Attack rate	00	0.4dB/ms
			01	0.2dB/ms
		X	X	Reserved
		X	X	Reserved
B[1:0]	R_Rate	Release rate	00	0.4dB/ms
			01	0.2dB/ms
			10	0.1dB/ms
			11	0.05dB/ms

- Address 9 : Quaternary and Ternary switching level

If the PWM exceeds the programmed switching power level (default 30*40ns), the modulation algorithm will change from quaternary to ternary modulation. Ternary modulation has less switching loss, resulting in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level, the modulation algorithm will change back to quaternary modulation.

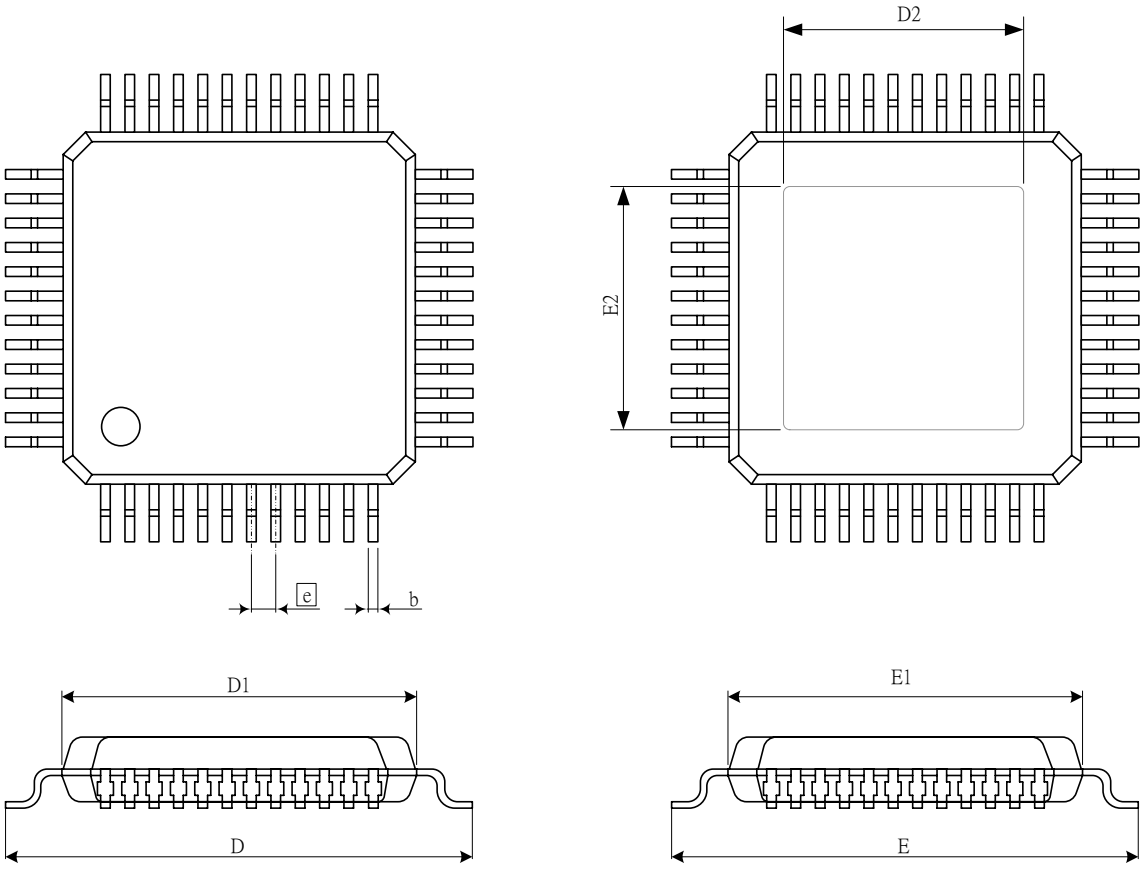
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	X	Reserved		
B[4:0]	QTS[3:0]	Quaternary and Ternary Switching level	11111	62
			11110	60
			:	:
			:	:
			10000	32
			01111	30
			01110	28
			:	:
			00010	4
			00001	4
			00000	4

Total Harmonic Distortion + Noise v.s. Output Power

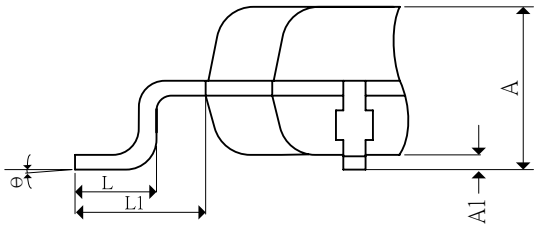


Package Dimensions

7mm x 7mm 48-pin E-LQFP



Symbols	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A1	0.05		0.15
b	0.17	0.22	0.27
D		9.00 BSC	
D1		7.00 BSC	
D2	4.5	5.0	5.5
E		9.00 BSC	
E1		7.00 BSC	
E2	4.5	5.0	5.5
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 BSC	
θ	0°	3.5°	7°



Revision History

Revision	Date	Description
0.1	2010.07.28	Original
0.2	2010.10.20	Add Q+T test fig.
1.0	2011.03.17	1. Modify system clock timing (page 14) 2. Delete Preliminary
1.1	2011.09.08	1) Changed PVDD range from 12V~24V to 10V~26V. 2) Changed PVDD absolute maximum rating from 26.4V to 30V. 3) Changed output power from 10Wx2CH to 15Wx2CH for stereo and 20Wx1CH to 30Wx1CH for mono. 4) Remove the unsuitable output power description for output power > 15Wx2CH @ stereo and 30Wx1CH @ mono. 5) Updated the application circuit that the snubber circuit can be removed while the PVDD <=18V for stereo. 6) Added the application circuit for economic type, moderate EMI suppression. 7) Added power on sequence flow. 8) Updated MPQ description. 9) Removed the product ID of AD82587-EF48NAR with QFN 48L package.
1.2	2012.08.10	Added product id for TR packing

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