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## **2X20W Stereo (BTL) / 1X40W Mono (PBTL) / 4x10W (SE) DIGITAL AMPLIFIER POWER STAGE**

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**Features**

- P2P with AD92580
- Single supply voltage(LDO built-in)
- PVDD range from 5V to 26V
- Support single-ended input audio PWM (AD) modulated signal
- Support differential input audio PWM (AD & BD) modulated signal
- Loudspeaker output power for stereo (BTL)
  - 20W x 2CH @ THD+N=0.1% into 8Ω at 24V
  - 15W x 2CH @ THD+N=0.1% into 8Ω at 18V
  - 10W x 2CH @ THD+N=0.15% into 8Ω at 15V
  - 6W x 2CH @ THD+N=0.18% into 8Ω at 12V
- Loudspeaker output power for mono (PBTL)
  - 40W x 1CH @ THD+N=0.1% into 4Ω at 24V
  - 30W x 1CH @ THD+N=0.13% into 4Ω at 18V
  - 20W x 1CH @ THD+N=0.15% into 8Ω at 15V
- Loudspeaker output power for 4CH (SE)
  - 10W x 4CH @ THD+N=0.22% into 4Ω at 24V
  - 8W x 4CH @ THD+N=0.29% into 4Ω at 18V
  - 5W x 4CH @ THD+N=0.3% into 4Ω at 15V
  - 3W x 4CH @ THD+N=0.3% into 4Ω at 12V
- Over-temperature protection
- Over-current protection
- Under-voltage detection
- Error report
- Built-in anti-pop function
- Add mute function
- 24-pin E-TSSOP thermally-enhanced package

**Applications**

- TV audio
- DVD Receiver
- Home Theaters

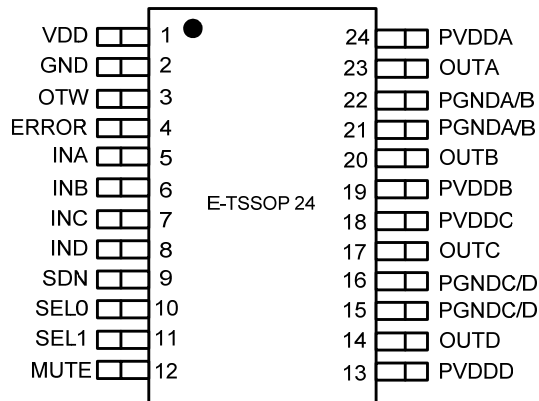
**Description**

AD92580C is a high performance stereo digital amplifier power stage. It can deliver 20Wx2CH output power (BTL) into 8Ω loudspeaker for stereo; or 40Wx1CH output power into 4Ω loudspeaker for mono in PBTL configuration within <1% THD+N at 24V supply. AD92580C also supports 10Wx4CH output power into 4Ω loudspeaker for 4CH in SE configuration within <1% THD+N at 24V supply.

A patented, built-in anti-pop function can reduce the speaker's pop noise without requiring complex anti-pop sequence in PWM input.

AD92580C's chip is integrated with over-temperature, over-current, and under-voltage protection circuits. These additions safeguard the AD92580C against fault conditions that could damage the chip and system catastrophically.

## Pin Assignments



## Pin Description

PIN	NAME	TYP	DESCRIPTION
1	VDD	P	Regulated output
2	GND	P	Ground for digital circuit
3	OTW	O	Over temperature warning.
4	ERROR	O	Error pointer
5	INA	I	PWM input A
6	INB	I	PWM input B
7	INC	I	PWM input C
8	IND	I	PWM input D
9	SDN	I	Shutdown (active-low) with soft pulled resistor 100kohm to ground
10	SEL0	I	Mode select pin 0
11	SEL1	I	Mode select pin 1
12	MUTE	I	Mute Selection (with soft pulled resistor 100kohm to ground ) 1:Mute 0:Normal
13	PVDDD	P	Power supply for half bridge D
14	OUTD	O	Half-bridge output D
15	PGNDC/D	P	Ground for half bridge C/D
16	PGNDC/D	P	Ground for half bridge C/D
17	OUTC	O	Half-bridge output C
18	PVDDC	P	Power supply for half bridge C
19	PVDDB	P	Power supply for half bridge B
20	OUTB	O	Half-bridge output B
21	PGNDA/B	P	Ground for half bridge A/B
22	PGNDA/B	P	Ground for half bridge A/B
23	OUTA	O	Half-bridge output A
24	PVDDA	P	Power supply for half bridge A

## Ordering Information

Product ID	Package	Packing	Comments
AD92580C-QG24NAT	E-TSSOP 24L	62 units / tube 100 tubes / small box (6.2k)	Green

## Available Package

Package Type	Device No.	$\theta_{ja}$ (°C/W)	$\Psi_{jt}$ (°C/W)	$\theta_{jc}$ (°C/W)	Exposed Thermal Pad
E-TSSOP 24L	AD92580C	31.5	2.16	7.5	Yes ( <b>Note 1</b> )

**Note 1.1:** The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

**Note 1.2:**  $\theta_{ja}$  is measured on a room temperature ( $T_A=25^\circ\text{C}$ ), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

**Note 1.3:**  $\theta_{jc}$  represents the heat resistance for the heat flow between the chip and the package's top surface.

**Note 1.4:**  $\Psi_{jt}$  represents the heat resistance for the heat flow between the chip and the exposed pad's center.

## Marking Information

### AD92580C

- Marking Information

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

