# 5.0A, Synchronous Step-Down DC-DC Converter

#### **General Description**

EML3273 is a high efficiency, DC-DC synchronous buck converter witch provides 5.0A output loading after output voltage reach preset voltage. EML3273 uses different modulation algorithms for various loading conditions. Under heavy load, EML3273 regulates the output voltage using Pulse Width Modulation (PWM). The PWM mode provides low output voltage ripple and fixed frequency noise. While in light load, it enters Power Skip Modulation (PSM) automatically to ensure a highly efficient operation at light load condition. Under very heavy load condition, or when the input voltage approaches the output voltage, EML3273 enters low dropout voltage operation under 100% duty cycle.

The internal generated 0.8V precision feedback reference voltage is designed for low output voltage request. Low Power-FET Ron synchronous switch dramatically reduces conduction loss.

The EML3273 is available in an 8-pin, space-saving E-SOP-8L package.

#### **Features**

- Wide Operating Voltage Ranges: 3.0V to 5.5V
- 5.0A Output Current
- High efficiency Buck Power Converter
- Auto-select PSM/PWM (Mode=VCC)
- Force PWM (Mode=GND)
- Power Good Indicator
- LDO mode: duty cycle: 100%
- Synchronous Power Switches Rectification, no Schottky Diode Required
- 1 MHz Switching Frequency
- Internal Soft-Start
- Current Limit Protection
- Over Temperature Protection
- Output Shorting Protect
- Output Over Voltage Protection

#### **Applications**

- Cellular telephone
- Wireless and DSL Modems
- Digital Still Cameras
- Portable Products
- MP3 Players

## **Typical Application**

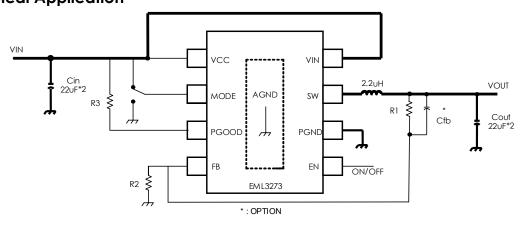
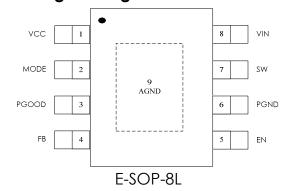


Fig. 1 EML3273 application circuit



## **Package Configuration**



#### EML3273-00SG08NRR

00 Adjustable

SE08 E-SOP-8L Package

NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85°C

Package in Tape & Reel

## Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
E-SOP-8L	adjustable	EML3273-00SG08NRR	ESMT EML 3273 Tracking code	Tape & Reel 3K units

## **Functional Block Diagram**

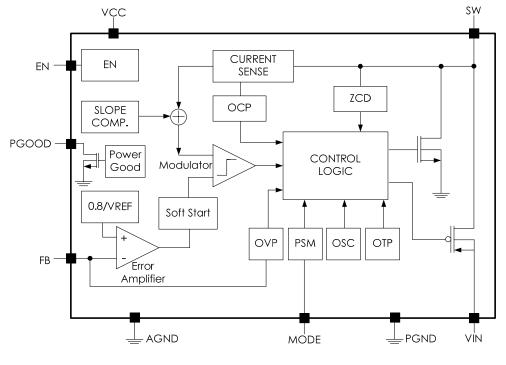


Fig. 2



#### **Pin Functions**

Pin Name	E-SOP-8L	Function
VCC	1	Analog Input Pin.
VCC	ı	Supply power to internal circuit.
		Mode Select Pin.
		Mode=VCC: The device is operating in regulated frequency pulse
MODE	2	width modulation (PWM) or pulse skip modulation (PSM)
MODE	2	at heavy load and light load respectively.
		Mode=GND: The device is forced in regulated frequency PWM
		operation
		Power Good Pin
PGOOD	3	Open-Drain Output. Connect this pin to VCC by a $100 \mathrm{K}\Omega$ pull-up
		resistor.
	4	Feedback Pin.
FB		Receives the feedback voltage from an external resistive divider
		across the output.
EN	5	Enable Pin.
LIN	3	Chip enable pin (1:Enable ; 0:Disable).
PGND	6	Ground Pin.
	7	Switch Pin.
SW		Must be connected to Inductor. This pin connects to the drains of the
		internal main and synchronous power MOSFET switches.
	8	Power Supply Pin.
VIN		Must be closely decoupled to PGND pin with a 22µF*2 or greater
		ceramic capacitor.
	9	Ground Pin/Thermal Pad
AGND		This Pin must be connected to ground. The thermal pad with large
		thermal land area on the PCB will helpful chip power dissipation.



#### **Absolute Maximum Ratings**

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage (VIN, VCC)	0.3V to 6.0V
EN, FB Voltages	0.3V to V <sub>IN</sub>
SW Voltage	$-0.3V$ to $(V_{IN} + 0.3V)$
Lead Temperature (Solder	ing, 10 sec) 260°C

Operating Temperature Range ----- -40°C to 85°C Junction Temperature (Note 1) ----- 150°C Storage Temperature Range ----- - 65°C to 150°C

#### Thermal data

Package	Thermal resistance	Parameter	Value
F 00D 01	heta JA (Note 2)	Junction-ambient	50°C/W
E-SOP-8L	$\theta$ JC (Note 3)	Junction-case	10°C/W

#### **Electrical Characteristics**

 $V_{IN} = V_{VCC} = V_{EN} = 3.6 V$ ,  $V_{OUT} = 1.2 V$ ,  $V_{FB} = 0.8 V$ , L = 2.2 uH,  $C_{IN} = 22 uF^*2$ ,  $C_{OUT} = 22 uF^*2$ ,  $T_A = 25 ^{\circ}C$ , MODE=VCC.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
$V_{IN}$	Input Voltage Range		3.0		5.5	٧
lo	Supply Current \/ =2 (\/	Switching (EN=VCC)		265		μΑ
lq	Supply Current V <sub>IN</sub> =3.6V	Shutdown (EN=0)			1	μΑ
UVLO	Under Voltage Lockout	When SW starts/stops switching	1.8		2.1	٧
Vref	Reference Voltage	$V_{IN} = 3.0V \text{ to } 5.0V$	0.784	0.8	0.816	٧
V <sub>EN</sub>	Enable Threshold	-40°C ~ +85°C	0.4		1.5	٧
Vo	Output Voltage Range	When using external feedback resistors to drive FB	0.8		VIN	>
Vout	Output Voltage Accuracy	$3.0V \le V_1 \le 5.5V$ , $0mA \le I_0 \le 5A$	0.97xV <sub>NOM</sub>	$V_{NOM}$	1.03xV <sub>NOM</sub>	٧
	Lie - De audelie -	$V_{IN} = 3.0V \text{ to } 5.0V, I_{OUT} = 10\text{mA}$		0.04		%/V
Δνουτ/Δνουτ	Line Regulation	V <sub>IN</sub> = 3.0V to 5.0V, I <sub>OUT</sub> =5.0A		0.08		%/V
ΔVουτ/ΔΙουτ	Load Regulation	l <sub>out</sub> = 1mA to 5.0A		0.01		%/A
R <sub>ON(P)</sub>	R <sub>DS(ON)</sub> of PMOS	I <sub>OUT</sub> =500mA		76		mΩ
Ron(n)	R DS(ON) of NMOS	Iout=500mA		71		mΩ
Fosc	Oscillator Frequency	VFB=0.8V, -40°C ~+85°C	0.8	1	1.2	MHz
Max. Duty	Maximum Duty	V 0.0V/1 5.0V/	100			%
Min. Duty	Minimum Duty.	$V_{IN} = 3.0V \text{ to } 5.0V$		15		%
ОТР	Thermal Shutdown	Hysteresis=30°C		159		$^{\circ}\mathbb{C}$

**Note 1:**  $T_J$  is a function of the ambient temperature  $T_A$  and power dissipation  $P_D$  ( $T_J = T_A + (P_D) * \theta J_A$ )).

Note 2: θ JA is measured in the natural convection at TA=25°C on a highly effective thermal conductivity test board(2 layers, 2S0P) according to the JEDEC 51-7 thermal measurement standard.

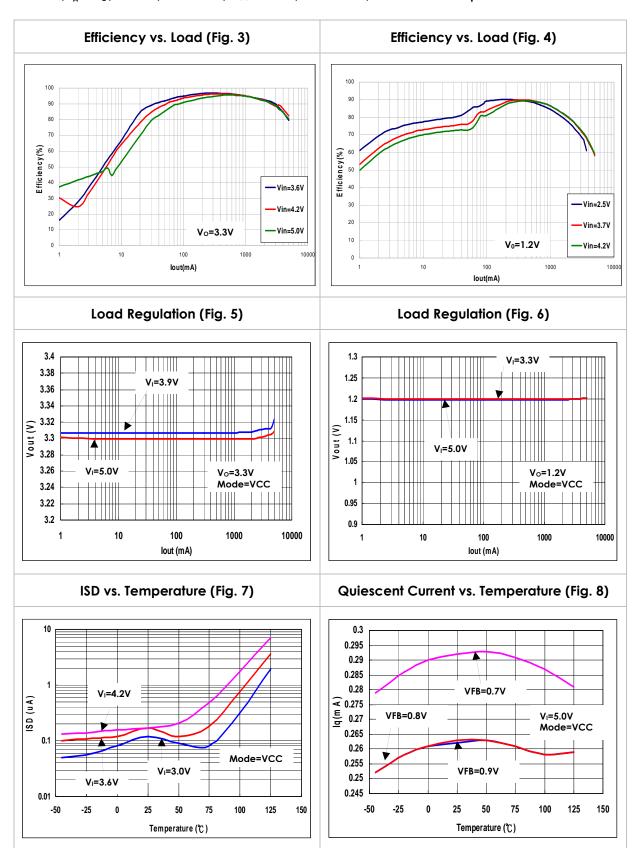
**Note 3:**  $\theta$  JT represents the heat resistance between the chip and the center of package top.

Publication Date: Jun. 2014 Revision: 0.1 4/17



### **Typical Performance Characteristics**

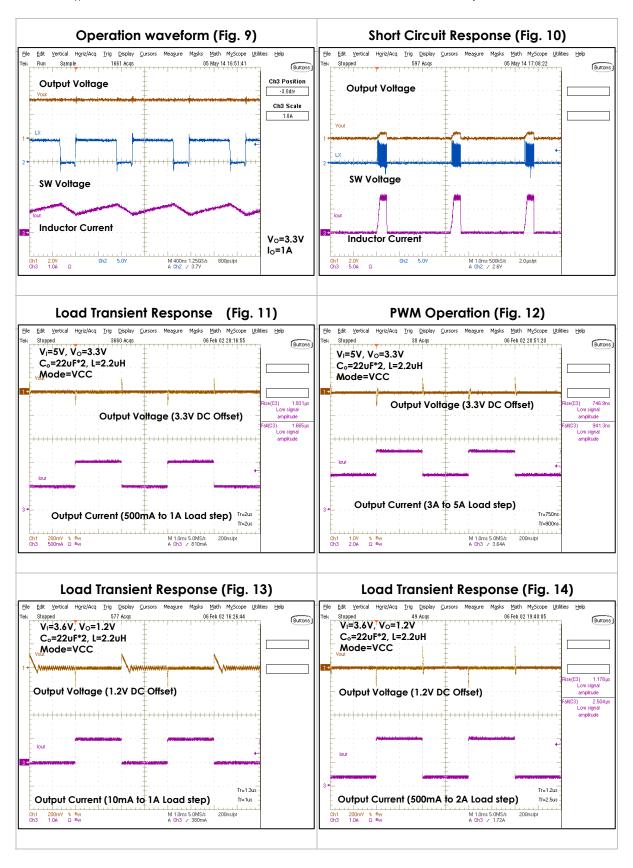
V<sub>IN</sub>=5.0V, T<sub>A</sub>=25°C, L=2.2uH, C<sub>IN</sub>=22uF\*2, C<sub>OUT</sub>=22uF\*2, Mode=VCC, unless otherwise specified





#### **Typical Performance Characteristics**

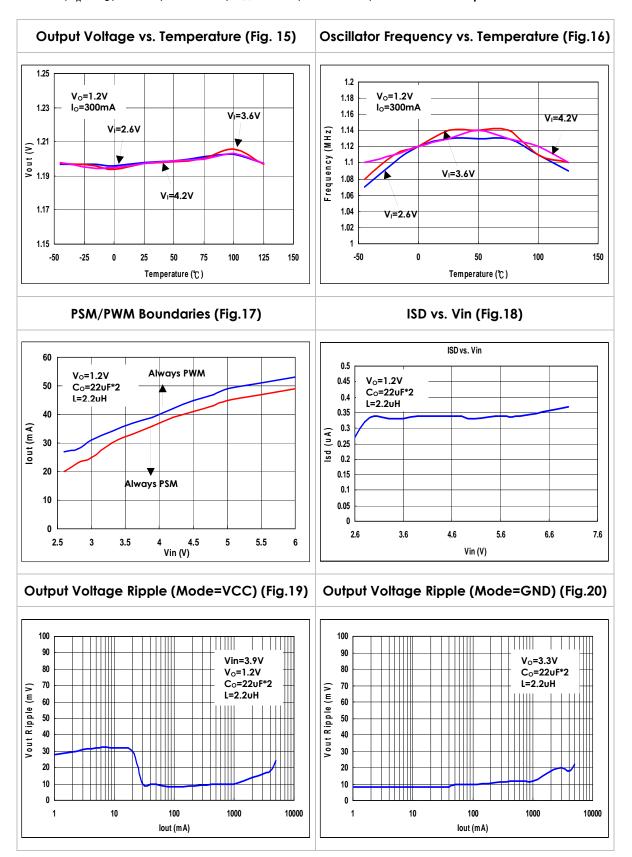
V<sub>IN</sub>=5.0V, T<sub>A</sub>=25℃, L=2.2uH, C<sub>IN</sub>=22uF\*2, C<sub>OUT</sub>=22uF\*2, Mode=VCC, unless otherwise specified





## **Typical Performance Characteristics**

V<sub>IN</sub>=5.0V, T<sub>A</sub>=25℃, L=2.2uH, C<sub>IN</sub>=22uF\*2, C<sub>OUT</sub>=22uF\*2, Mode=VCC, unless otherwise specified



**ESMT** 

**Application Information** 

**Detailed Description** 

The EML3273 is a synchronous, step-down DC/DC converter. It allows up to 5.0A current output with adjustable output voltage. Throughout the entire operating range, EML3273 can maintain high efficiency using both PWM (heavy load) and PSM (light load) modes with very small output voltage ripple performance.

During normal operation, the internal oscillator sends a pulse signal to set latch to turn on/off internal high-side MOSFET and low-side MOSFET during each clock cycle. When the current-mode ramp signal which is the sum of internal high-side MOSFET current and slope compensation ramp exceeds output voltage of error amplifier, the PWM comparator will send a signal to reset latch and turn off/on internal high-side MOSFET/low-side MOSFET. The error amplifier adjusts its output voltage by comparing the reference voltage and the feedback voltage.

The basic EML3273 application circuits are shown as in Figure 1, External components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

**PSM** 

In order to increase light load efficiency, save switching loss is used in EML3273. During in light load, the device only switching when output voltage is below the pre-set threshold. This function can skip some switching cycle that save unnecessary loss. The fig.19 and fig.20 illustrate the difference between PSM and PWM output voltage ripple. The switching frequency and output ripple is dependant on factors such as loading, inductor and output capacitance. Besides, the input and output voltage ratio is a factor which affects device going PSM mode or not. Reference fig.17, as input voltage decreases, PSM/PWM boundary decreases to close 0mA. Keep light load in PSM,  $V_{IN} > V_{OUT}+1V$  is necessary.

**Mode Selection** 

The mode pin allows to select the operating mode of the device. Connecting this pin to high make PWM and PSM change automatically. The converter operates in regulated frequency PWM mode at heavy loads and in the PSM mode during light loads, which maintains high efficiency over a wide load current range. Pulling the mode pin low forces the converter to operate in the PWM mode. There is smaller ripple in this mode at the light load current.

**Power Good** 

Power good flag is pulled down when EML3273 start-up and the FB pin voltage is still outside pre-set voltage window. During normal operation phase, when FB pin voltage drop under 87.5% or increase over 112.5%, power good flag is also pulled down.

Publication Date: Jun. 2014 Revision: 0.1 **8/17** 



#### **Inductor Selection**

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance result in high ripple current. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. In experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN} - V_{OUT})}{F_{OSC} * \Delta I_L} * \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{F_{OSC} * (2 * (10\% \sim 20\%) * I_{LOAD})} * \frac{V_{OUT}}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_{L} = \frac{V_{OUT}}{F_{OSC} * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Choose an inductor that does not saturate under the worst-case load conditions, which is the load current plus half the peak-to-peak inductor ripple current, even at the highest operating temperature. The peak inductor current is:

$$I_{L\_PEAK} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The inductors in different shape and style are available from manufacturers. Shielded inductors are small and radiate less EMI issue. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

#### Recommend Table

Inductor	Dimensions	Component	Model	ISAT	DCR
Value (µH)	(mm)	Supplier		(A)	(mΩ)
2.2	5.2 x 4.9 x 3.0 max.	CYNTEC	PCMB053T-2R2MS	9	29 typ.

Elite Semiconductor Memory Technology Inc.

Publication Date: Jun. 2014 Revision: 0.1



#### **Input Capacitor Selection**

The input capacitor must be connected to the VIN pin and GND pin of EML3273 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage. In normal operation, the input current is discontinuous in a buck converter. The source current waveform of the high-side MOSFET is a square wave. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{\mathit{RMS}} = I_{\mathit{LOAD\_MAX}} * \sqrt{\frac{V_{\mathit{OUT}}}{V_{\mathit{IN}}}} * \left(1 - \frac{V_{\mathit{OUT}}}{V_{\mathit{IN}}}\right)$$

It can be seen that when  $V_O$  is half of  $V_{IN}$ ,  $C_{IN}$  is under the worst current stress. The worst current stress on  $C_{IN}$  is  $I_{O\_MAX}/5.0$  A 47µF ceramic capacitor is recommended value in typical application.

#### **Output Capacitor Selection**

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_{OUT} = \Delta I_L * \left( ESR_{COUT} + \frac{1}{8 * F_{OSC} * C_{OUT}} \right)$$

Where  $F_{OSC}$  = operating frequency,  $C_{OUT}$ = output capacitance and  $\Delta I_L$  = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage. A 22µF ceramic capacitor is recommended value in typical application.

#### Recommend Table

Capacitor Value (µF)	Case Size	Component Supplier	Model
22	0805 1206	TDK	C2012JB0J226M

Elite Semiconductor Memory Technology Inc.

Publication

Publication Date: Jun. 2014 Revision: 0.1 10/17



#### **Using Ceramic Input and Output Capacitors**

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush current through the long wires can potentially cause a voltage spike at V<sub>IN</sub>, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R specification. Their dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

#### **Load Transient**

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, VOUT immediately shifts by an amount equal to

$$\Delta I_{IOAD} * ESR_{COUT}$$

ESR is the effective series resistance of output capacitor.  $\triangle$ ILOAD also begins to charge or discharge Cour generating a feedback error signal used by the regulator to return Vour to its steady-state value. During the recovery time, Vour can be monitored for overshoot or ringing that would indicate a stability problem.

#### **Short-Circuit Protection**

When EML3273 output node is shorted to GND, chip will enter soft-start to protect itself, when short circuit is removed, EML3273 enter normal operation again. If EML3273 reach OCP threshold while short circuit, EML3273 will enter soft-start cycle until the current under OCP threshold.

#### **Over Temperature Protection**

The internal high-side MOSFET is turned off when the internal thermal sensor detects that the junction temperature exceeds  $160^{\circ}$ C, entering the Over Temperature Protection mode (OTP). The OTP mode is unlocked at  $130^{\circ}$ C, i.e. a  $30^{\circ}$ C hysteresis.

#### **Output Voltage Setting**

The output voltage of EML3273 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R_1}{R_2}\right) = 0.8 * \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider senses the fraction of the output voltage as shown in Fig.21 Using large feedback resistor can increase efficiency, but too large value affects the device's output accuracy because of leakage current going into device's FB pin. The recommended value for R2 is therefore in the range of  $50K\Omega$ .

Elite Semiconductor Memory Technology Inc.

Publication Date: Jun. 2014 Revision: 0.1 11/17



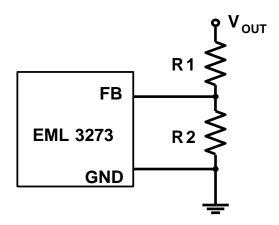


Fig. 21 Setting the Output Voltage

## **Under Voltage Lock Out**

The under-voltage lockout (UVLO) circuitry ensures that the EML3273 starts up with adequate voltage. The regulator output is disabled whenever VIN is below UVLO. The hysteresis of UVLO is designed to be 100 mV.



## **Applications**

## Typical Schematic for PCB Layout

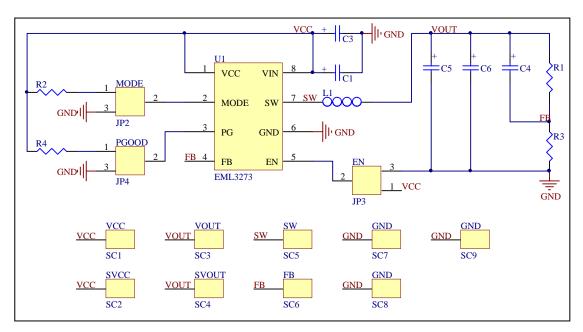


Fig. 25

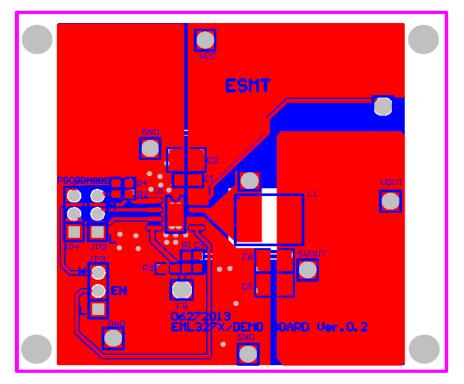
## **PCB Layout Guidelines**

When laying out the printed circuit board, the following checklist should be used to optimize the performance of EML3273.

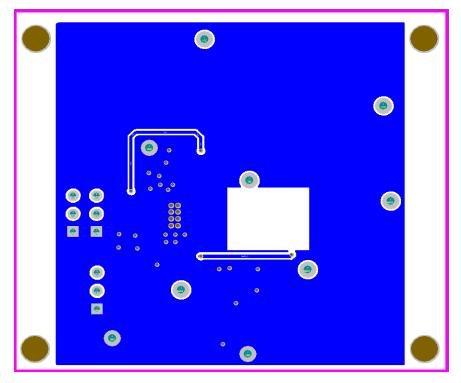
- 1. The power traces, including the GND trace, the SW trace and the  $V_{IN}$  trace should be kept direct, short and wide.
- 2. Put input capacitor as close as possible to the  $V_{\mbox{\scriptsize IN}}$  and GND pins.
- 3. The FB pin should be connected directly to the feedback resistor divider.
- 4. Keep the switching node, SW, away from the sensitive FB pin and the node should be kept small area.



## Typical Schematic for PCB layout (cont.)



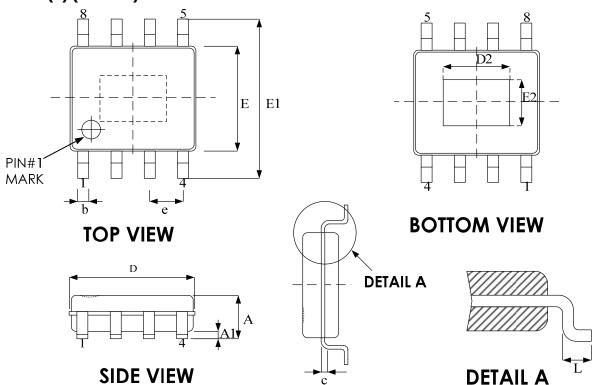
Top Layer



Bottom Layer



# Package Outline Drawing SOP-8 (E) (150 mil)



C1 1	Dimension in mm		
Symbol	Min	Max	
А	1.35	1.75	
A1	0.00	0.25	
Ъ	0.33	0.51	
С	0.17	0.25	
D	4.80	5.00	
Е	3.81	4.00	
E1	5.79	6.20	
е	1.27 BSC		
L	0.41	1.27	

Exposed pad

	Dimension	on in mm
	Min	Max
D2	1.93	2.39
E2	1.93	2.39



## **Revision History**

Revision	Date	Description
0.1	2014.06.27	initial version.

Publication Date: Jun. 2014 Revision: 0.1 16/17

## Important Notice

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of ESMT.

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.