2.5A, 18V Synchronous Step-Down Converter

General Description

The EML3300 is a synchronous buck regulator with integrated two 0.13Ω power MOSFETs. It achieves 2.5A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. The device includes cycle-by-cycle current limiting and thermal shutdown protection. The EML3300 requires a minimum number of readily available external components to complete a 2.5A buck regulator solution.

EML3300 is available in an 8-pin, space-saving E-SOP-8L package.

Features

- Wide 4.5V to 18V operating input range
- 2.5A output current
- 0.13ohm internal power MOSFET switches
- Stable with low ESR output ceramic capacitors up to 93% efficiency
- Programmable Soft-Start
- Fixed 340KHz frequency
- Thermal shutdown
- Cycle-by-cycle over current protection
- Output adjustable from 0.923V to 16V
- Input under voltage lockout

Applications

- Distributed power systems
- Battery charger network cards
- Pre-regulator for linear regulators
- DSL modems

Typical Application

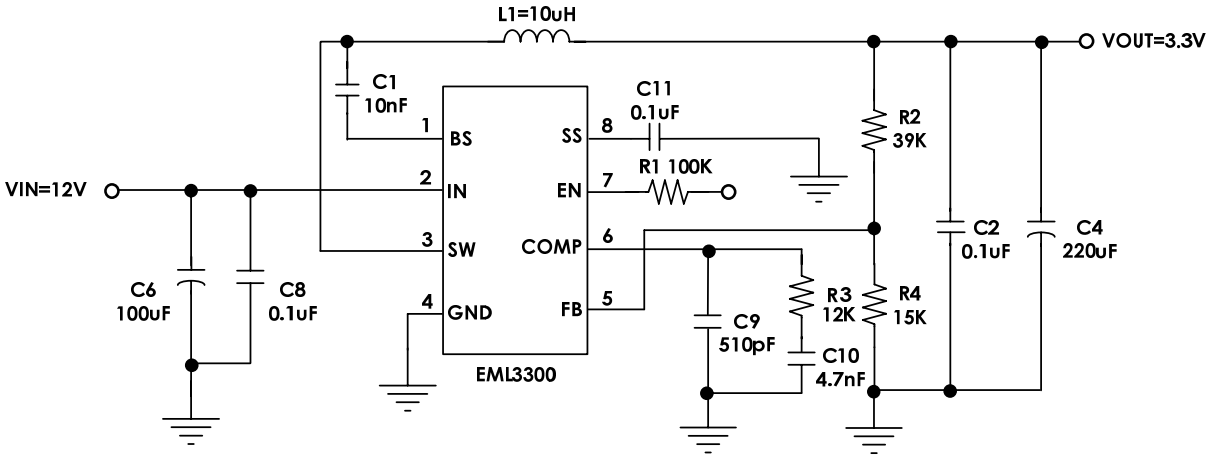
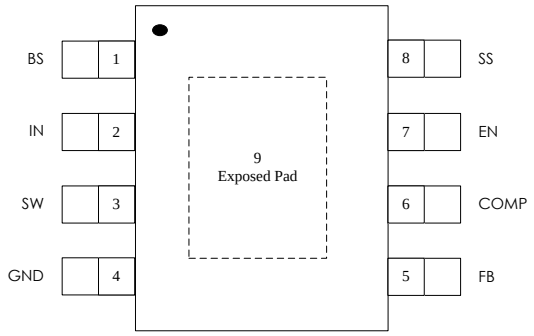


Fig. 1 EML3300 application circuit

Package Configuration

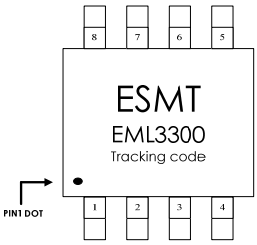


E-SOP-8L

EML3300-00SG08NRR

00	Adjustable
SG08	E-SOP-8L Package
NRR	RoHS & Halogen free package
	Commercial Grade Temperature
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
E-SOP-8L	adjustable	EML3300-00SG08NRR		Tape & Reel 3K units

Functional Block Diagram

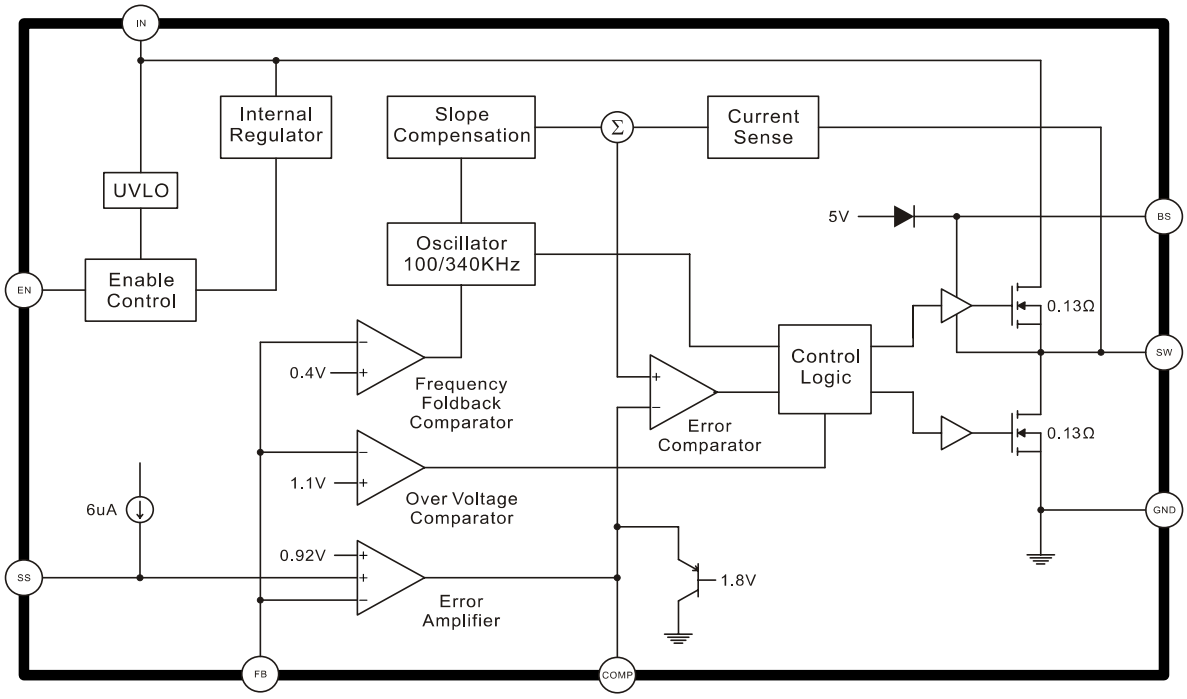


Fig. 2

Pin Functions

Pin Name	E-SOP-8L	Function
BS	1	**Bootstrap Pin.**
IN	2	**Power Supply Pin.** Must be closely decoupled to PGND pin with a 100μF or greater capacitor.
SW	3	**Switch Pin.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
GND	4	**Ground Pin.**
FB	5	**Feedback Pin.** Receives the feedback voltage from an external resistive divider across the output.
COMP	6	**Compensation Pin.**
EN	7	**Enable/UVLO Pin.** Chip enable pin (1:Enable ; 0:Disable).
SS	8	**Soft Start Pin.**
Exposed Pad	9	**Thermal Land Pad.** This Pin must be connected to ground. The thermal pad with large thermal land area on the PCB will be helpful chip power dissipation.

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage ---------- – 0.3V to 18V
EN, FB Voltages ---------- – 0.3V to 6V
SW Voltage ---------- – 1V to (V_{IN} + 0.3V)
Bootstrap Voltage ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)

Lead Temperature (Soldering, 10 sec)---------- 260°C
Operating Temperature Range ----- –40°C to 85°C
Junction Temperature (Note 1) ---------- 150°C
Storage Temperature Range -------- – 65°C to 150°C

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 2)	Junction-ambient	50°C/W
	θ_{JC} (Note 3)	Junction-case	10°C/W

Electrical Characteristics

V_{IN}=12V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Supply Voltage		4.5		18	V
I_{SB}	Standby Current	V_{EN}≧3V,V_{FB}≧1.0V		0.7		mA
I_{ST}	Shutdown Supply Current	V_{EN}=0		1		μA
V_{FB}	Feedback Voltage	V_{IN}=12V,V_{COMP}<2V	0.900	0.923	0.946	V
V_{FB-OV}	Feedback Over Voltage Threshold			1.1		V
G_{EA}	Error Amplifier Voltage Gain			400		V / V
T_{EA}	Error Amplifier Transconductance	△IC=±10μA		830		μA / V
R_{ON-HS}	High Side Switch ON Resistance			0.13		Ω
R_{ON-LS}	Low Side Switch ON Resistance			0.13		Ω
I_{IL}	High Side Switch Leakage Current	V_{EN}=0,V_{SW}=0V		0.1	10	μA
I_{HCL}	High Side Current Limit		2.4	3.4		A
I_{LCL}	Low Side Current Limit	From Drain to Source		1.1		A
T_{CS}	COMP to Current Sense Transconductance			2.3		A / V
F_{OSC}	Oscillation Frequency		300	340	380	KHz
F_{SC}	Short Circuit Oscillation Frequency	V_{FB}=0V		100		KHz
D_{MAX}	Maximum Duty Cycle	V_{FB}=0.8V		90		%
T_{ON}	Minimum On Time			220		ns
V_{UVLO}	Input Under Voltage Lockout Threshold	V_{IN} Rising	3.8	4.0	4.4	V
$V_{UVLO-Hys}$	Input Under Voltage Lockout Threshold Hysteresis			200		mV
V_{ENLO}	EN Lockout Threshold	V_{EN} Rising	2.2	2.4	2.7	V
$V_{ENLO-Hys}$	EN Lockout Threshold Hysteresis			100		mV
V_{EN}	EN Threshold Voltage			1.0		V

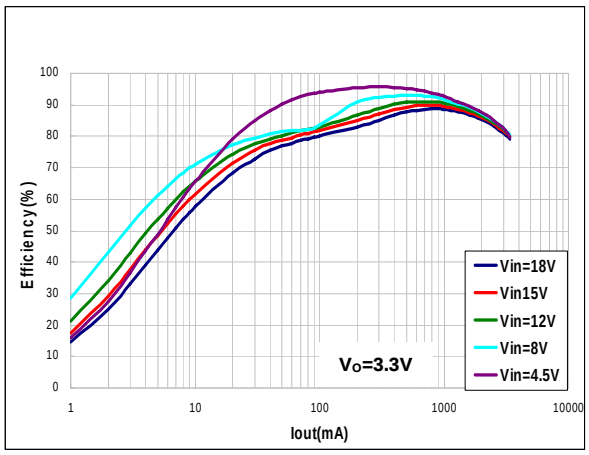
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{EN-Hys}	EN Threshold Voltage Hysteresis			250		mV
SS	Soft-Start Current	V_{SS}=0V		6		μA
T_{TS}	Thermal Shutdown			+150		°C

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * \theta_{JA}$)).
Note 2: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board(2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.
Note 3: θ_{JT} represents the heat resistance between the chip and the center of package top.

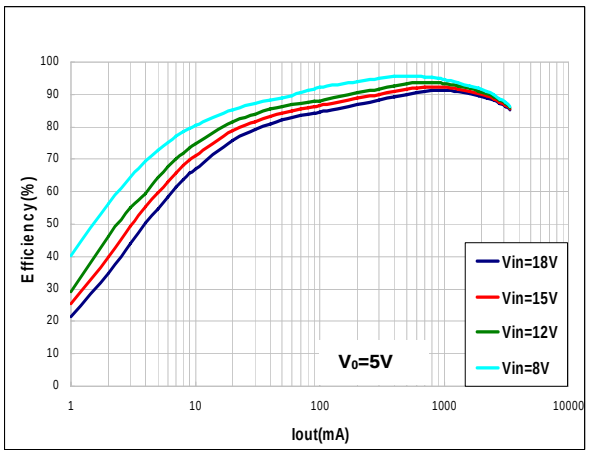
Typical Performance Characteristics

V_{IN}=12V, T_A=25℃, L=10uH, C_{IN}=100uF, C_{OUT}=220uF, unless otherwise specified

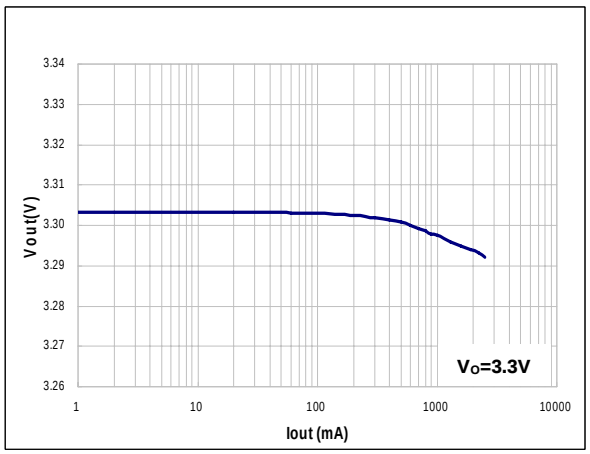
Efficiency vs. Load (Fig. 3)



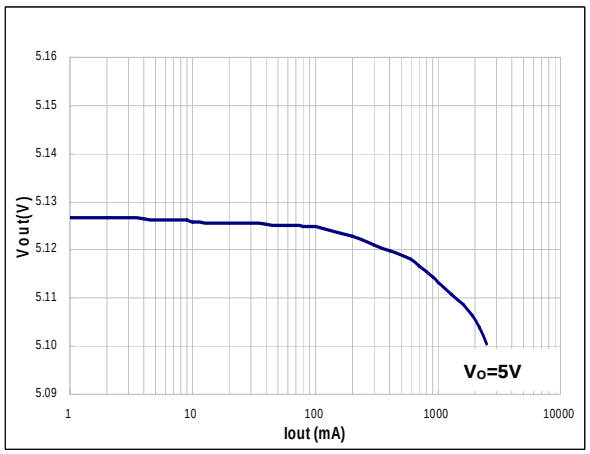
Efficiency vs. Load (Fig. 4)



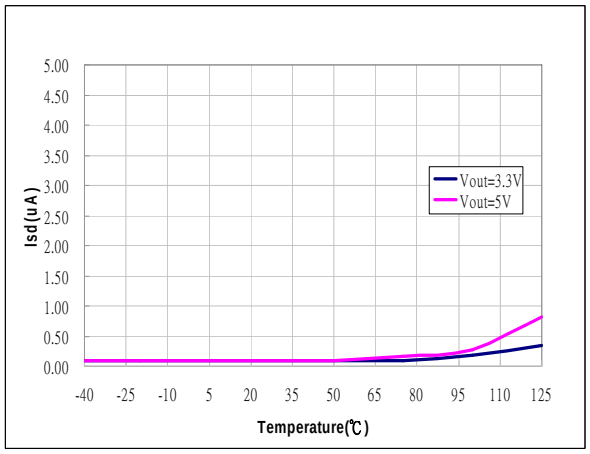
Load Regulation (Fig. 5)



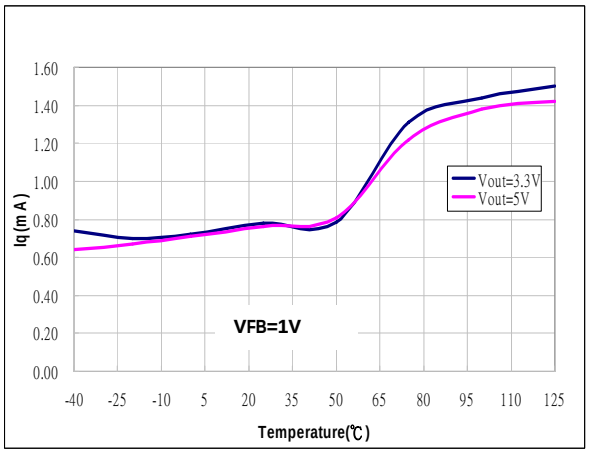
Load Regulation (Fig. 6)



ISD vs. Temperature (Fig. 7)



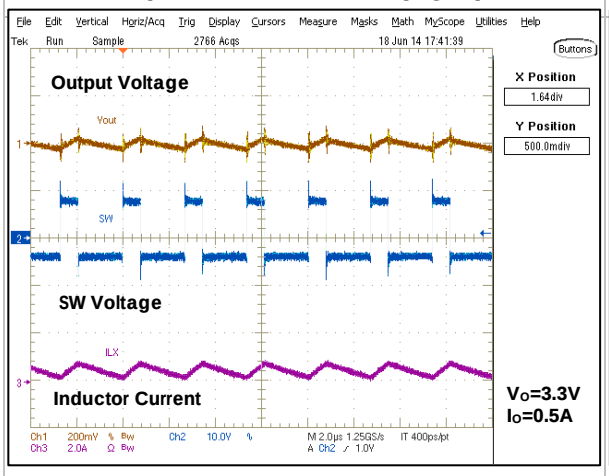
Quiescent Current vs. Temperature (Fig. 8)



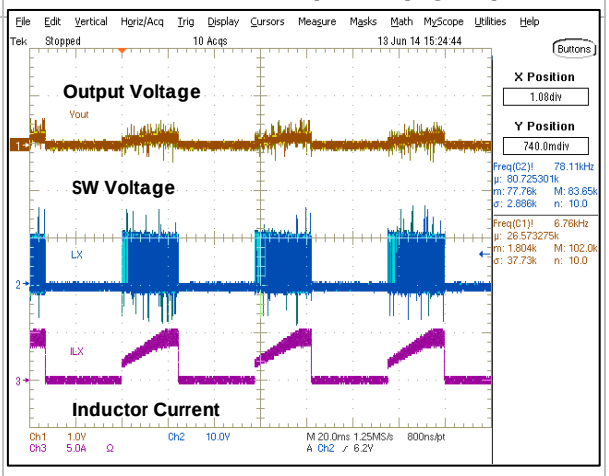
Typical Performance Characteristics

V_{IN}=12V, T_A=25℃, L=10uH, C_{IN}=100uF, C_{OUT}=220uF, unless otherwise specified

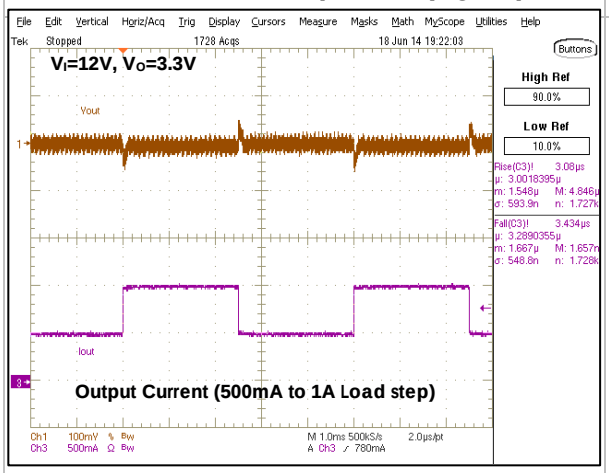
Operation waveform (Fig. 9)



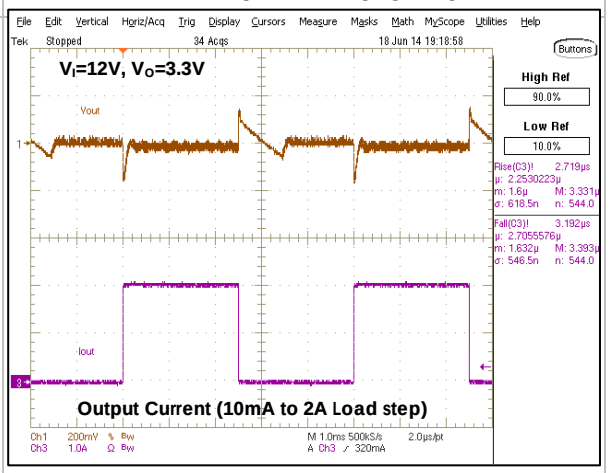
Short Circuit Response (Fig. 10)



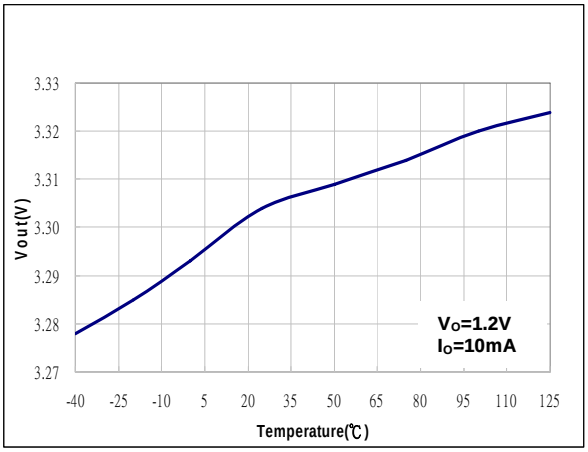
Load Transient Response (Fig. 11)



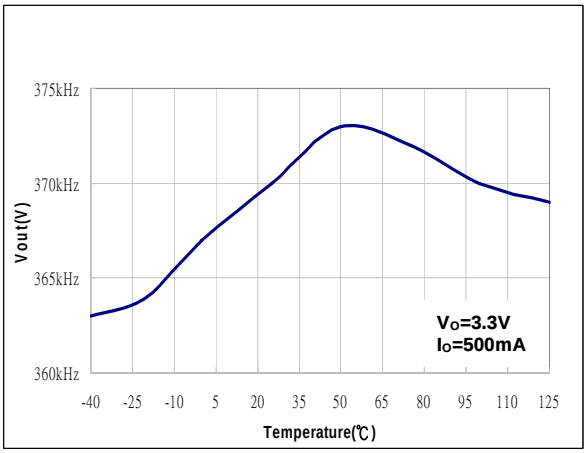
PWM Operation (Fig. 12)



Output Voltage vs. Temperature (Fig. 13)

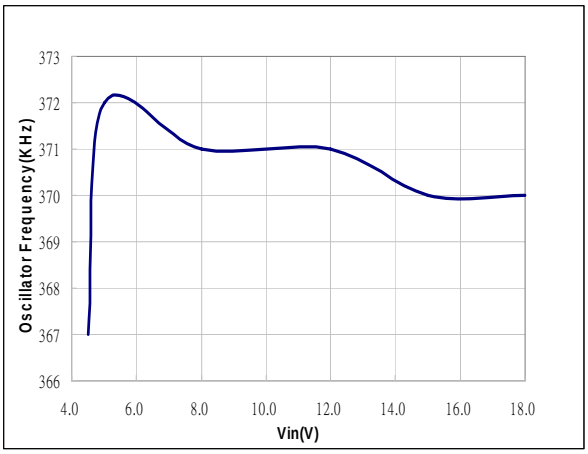
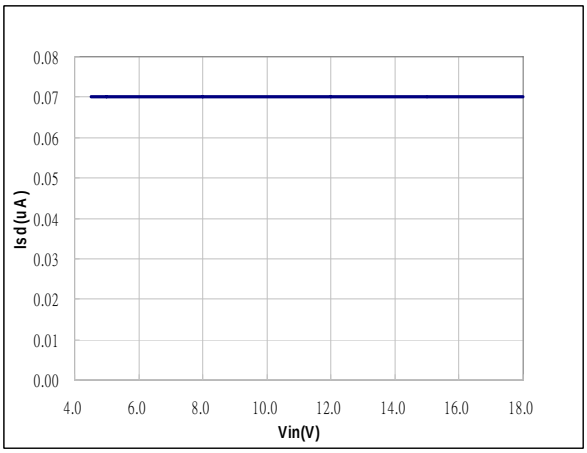


Oscillator Frequency vs. Temperature (Fig.14)



Typical Performance Characteristics

V_{IN}=12V, T_A=25℃, L=10uH, C_{IN}=100uF, C_{OUT}=220uF, unless otherwise specified

Oscillator Frequency vs. Vin (Fig.15)	ISD vs. Vin (Fig.16)
	

Function Information

Detailed Description

The EML3300 is a synchronous current-mode buck regulator. It regulates input voltages from 4.5V to 18V down to an output voltage as low as 0.923V, and is able to supply up to 2.5A of load current. The EML3300 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified by the internal error amplifier. The output current of the transconductance error amplifier is presented at COMP where a network compensates the regulation control system. The voltage at COMP is compared to the switch current measured internally to control the output voltage. The converter uses internal n-channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS drives the gate. The capacitor is charged from the internal regulator when the SW pin is low.

Output Voltage (V_{OUT})

The output voltage is set using a resistive voltage divider from the output voltage to FB. The voltage divider divides the output voltage down by the ratio:

$$V_{OUT} = V_{FB} \times \left(\frac{R2 + R4}{R4} \right)$$

A typical value for R4 can be as high as 100KΩ, but a typical value is 10KΩ.

Enable Mode / Shutdown Mode

Drive the EN Pin to ground to shutdown the EML3300. Shutdown forces the internal power MOSFETs off, turns off all internal circuitry. The EN Pin rising threshold is 1V (typ), and hysteresis is 250mV. For automatic startup application, pull up the EN pin with 100KΩ resister.

Boost High-Side Gate Drive (BST)

Since the MOSFET requires a gate voltage greater than the input voltage, connect a flying bootstrap capacitor between SW and BS to provide the gate-drive voltage to the high-side n-channel MOSFET switch. The capacitor is alternately charged from the internal regulator. On startup, an internal low-side switch connects SW to ground and charges the BST capacitor to internal regulated voltage. Once the BST capacitor is charged, and the internal low-side switch is turned off, the BST capacitor voltage provides the necessary enhancement voltage to turn on the high-side switch.

Thermal Shutdown Protection

The EML3300 features integrated thermal shutdown protection. When the IC junction temperature exceeds +150°C, thermal shutdown protection will be triggered. The internal power MOSFET is then turned off to limit the device power dissipation (P_D). Once thermal shutdown occurs, this device can go back to normal operation until the junction temperature drops below +100°C approximately.

Application Information

Input Capacitor Selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

The input capacitor can be electrolytic, tantalum or ceramic. When electrolytic or tantalum capacitors using, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors adopted, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by the formal below:

$$C_{IN} = \frac{I_O}{f \times \Delta V_{IN}} \times D(1-D)$$

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f \times L \times V_{IN}} \times \left(ESR + \frac{1}{8 \times f \times C_{OUT}} \right)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency.

a) In the case of ceramic capacitors

$$C_{OUT} = \frac{V_{OUT}}{8 \times f^2 \times L \times \Delta V_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

b) In the case of tantalum or electrolytic capacitors

$$ESR = \frac{\Delta V_{OUT} \times f \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})}$$

Inductor Selection

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and / or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by the formal below:

$$L = \frac{V_O + V_D}{I_O \gamma f}(1-D)$$

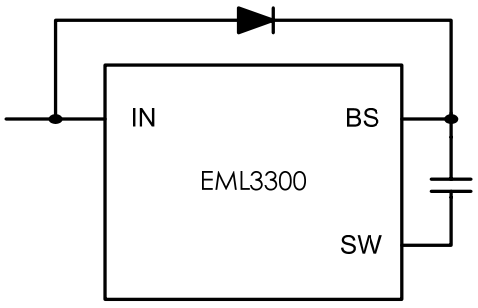
Where

r is the ratio of ripple current.

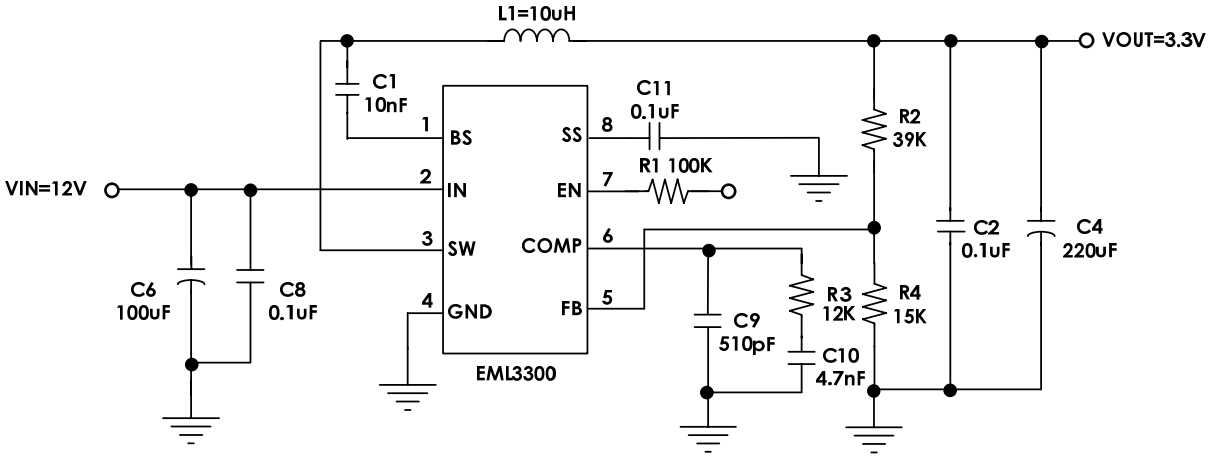
$I_{Lrms} = I_O \sqrt{1+\frac{\gamma^2}{12}}$, RMS current in inductor

External Boost Diode

For 5V input application, an external bootstrap diode is added to enhance the efficiency of the regulator. In these cases, the insufficient V_{GS} on the high side MOS will decrease the efficiency of the regulator, an external boost diode is recommended from V_{IN} to BT PIN.

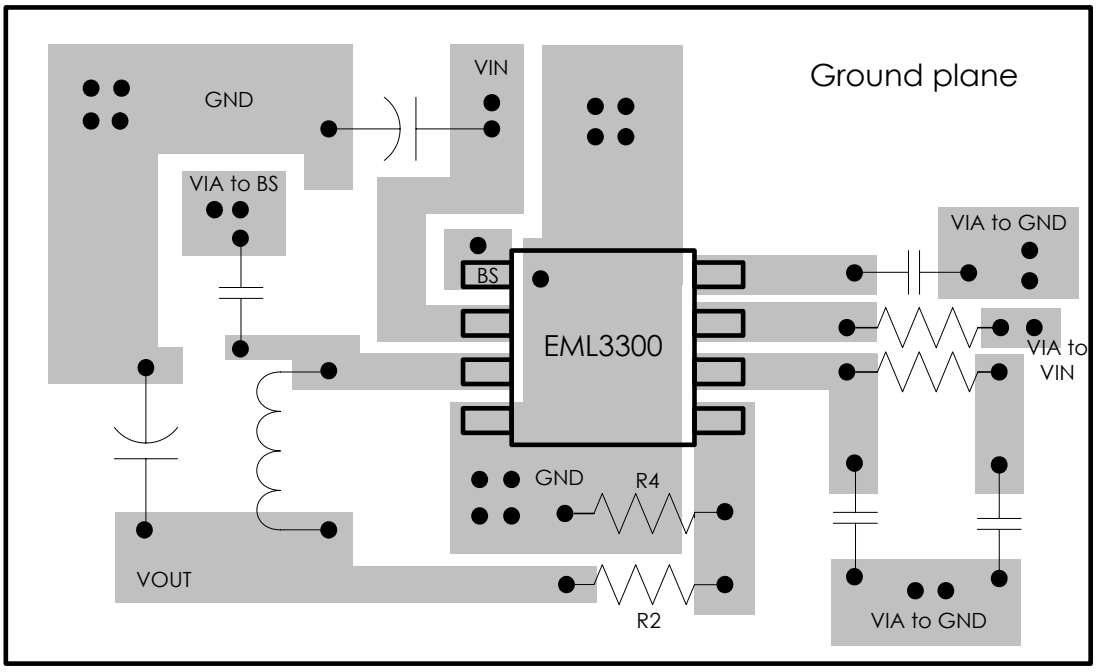


Typical Schematic for PCB Layout



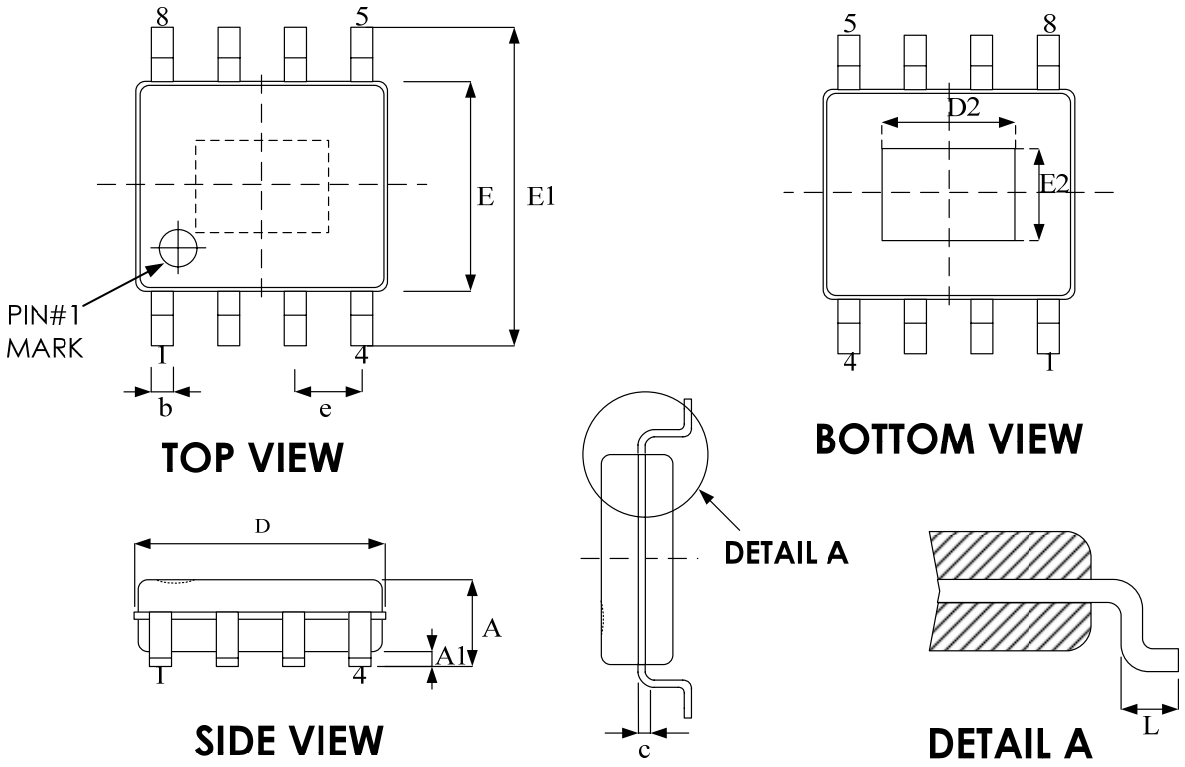
PC Board Layout Checklist

1) The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2) Place C_{IN} near IN Pin as closely as possible. To maintain input voltage steady and filter out the pulsing input current.
3) The resistive divider $R_2$and R_4 must be connected to FB pin directly as closely as possible.
4) FB is a sensitive node. Please keep it away from switching node, SW. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and the layer on which the feedback trace is routed. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.



Package Outline Drawing

SOP-8 (E) (150 mil)



Symbol	Dimension in mm	
	Min	Max
A	1.35	1.75
A1	0.00	0.25
b	0.33	0.51
c	0.17	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.41	1.27

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.84	3.10
E2	2.06	2.31

Revision History

Revision	Date	Description
0.1	2014.06.24	Initial version.
0.2	2014.11.21	Update Typical Performance Characteristics For efficiency
1.0	2015.03.11	Revise version to 1.0 & remove preliminary word

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