600mA CMOS Linear Regulator

General Description

The EMP8021 low-dropout (LDO) CMOS linear regulators feature low output voltage noise (63μV), low quiescent current (50μA), and fast transient response. It guarantees delivery of 600mA output current, and supports preset output voltages ranging from 0.8V to 4.75V with 0.05V increment.

The EMP8021 is ideal for battery-powered applications by virtue of its low quiescent current consumption and its 1nA shutdown mode of logical operation. The regulator provides fast turn-on and start-up time by using dedicated circuitry to pre-charge an optional external bypass capacitor. This bypass capacitor is used to reduce the output voltage noise without adversely affecting the load transient response. The regulator is stable with small ceramic capacitive loads (2.2μF typical).

Additional features include bandgap voltage reference, constant current limiting and thermal overload protection. The EMP8021 is available in miniature 5-pin SOT-23-5 package.

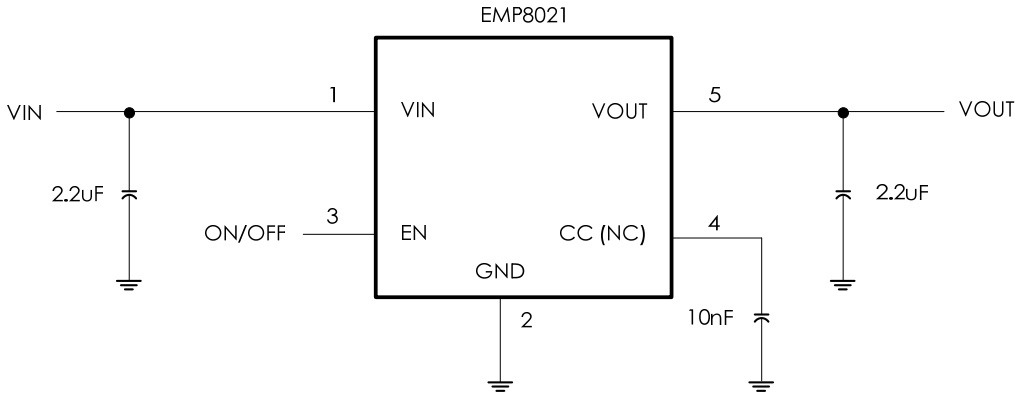
Applications

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

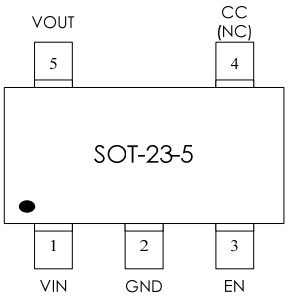
Features

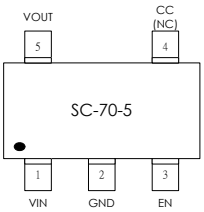
- Miniature SOT-23-5 packages
- 600mA guaranteed output current
- 63μV RMS output voltage noise (10Hz to 100kHz) (Vout=3.3V, Cbypass=10nF)
- 580mV typical dropout at 600mA(Vout=3.3V)
- 270mV typical dropout at 300mA(Vout=3.3V)
- 50μA typical quiescent current
- 1nA typical shutdown mode
- Fast line and load transient response
- 140μs typical fast turn-on time (Vout=3.3V, Cbypass=10nF)
- 2.2V to 5.5V input range
- Stable with small ceramic output capacitors
- Over temperature and over current protection
- ±2% output voltage tolerance

Typical Application



Connection Diagrams



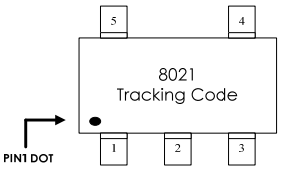


Order information

EMP8021-XXVF05NRR
XX Output voltage
VF05 SOT-23-5 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

EMP8021-XXVI05NRR
XX Output voltage
VI05 SC-70-5 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

Order, Marking & Packing Information

Package	Vout	Product ID.	No. of Pin	EN	CC (NC)	Marking	Packing
SOT-23-5	2.8	EMP8021-28VF05NRR	5	Y	Y		Tape & Reel 3Kpcs
	3.3	EMP8021-33VF05NRR					
SC-70-5	3.3	EMP8021-33VI05NRR	5	Y	Y		Tape & Reel 3Kpcs

Pin Functions

Name	SOT-23-5	Function
VIN	1	**Supply Voltage Input** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	**Ground Pin**
CC (NC)	4	**Compensation Capacitor** Connect an optimum 10nF noise bypass capacitor between the CC and the ground pins to reduce noise in VOUT. **(Note. It can be floated, but don't connect the CC pin to any DC voltage.)**
EN	3	**Shutdown Input** Set the regulator into the disable mode by pulling the EN pin low. To keep the regulator on during normal operation, connect the EN pin to VIN. The EN pin must not exceed VIN under all operating conditions.
VOUT	5	**Output Voltage Feedback**

Functional Block Diagram

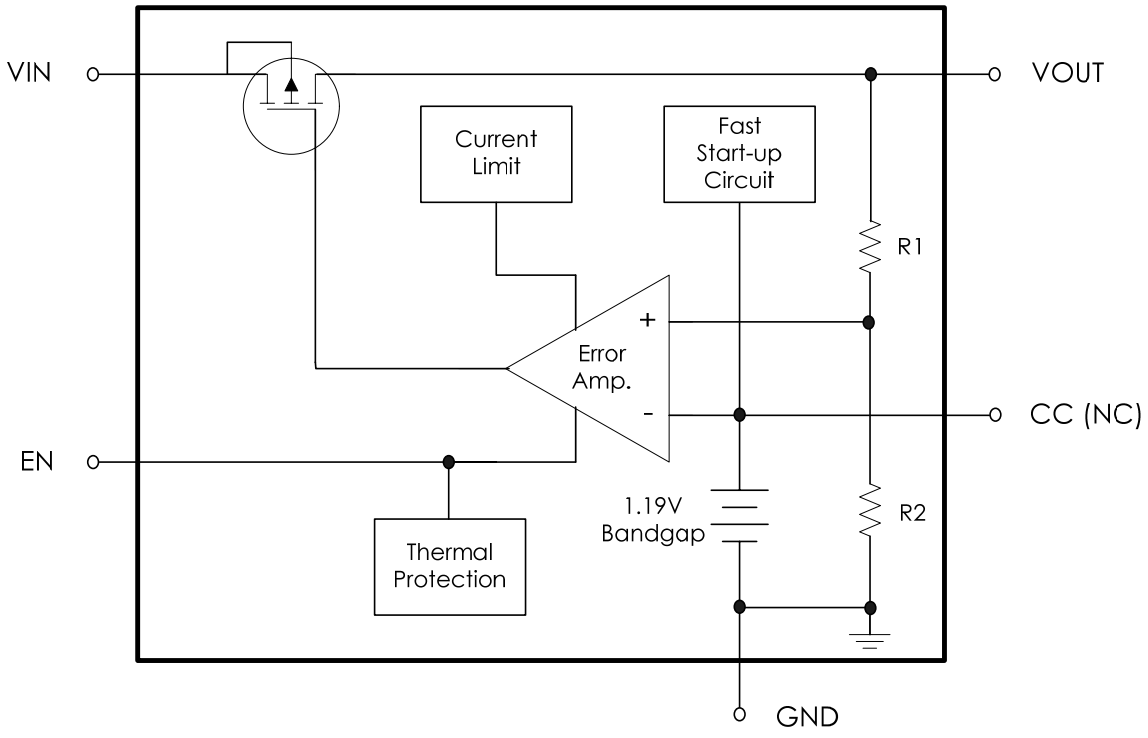


FIG.1. Functional Block Diagram of EMP8021

Absolute Maximum Ratings (Notes 1, 2)

VIN, VOUT, VEN	-0.3V to 6.0V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 5)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Model (Note 5)	2KV
Junction Temperature (T_J)	150°C	MM	200V

Operating Ratings (Note 1, 2)

Supply Voltage	2.2V to 5.5V	Thermal Resistance (θ_{JA}) (Note 3)	135°C /W(SOT-23-5)
Storage Temperature Range	-40°C to 85°C	Thermal Resistance (θ_{JC}) (Note 4)	81°C /W(SOT-23-5)

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_{OUT}$ +1V (Note 8), VEN = V_{IN}, $C_{IN} = C_{OUT}$ = 2.2µF, C_{CC} = 33nF, T_A = 25°C. **Boldface** limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V_{IN}	Input Voltage		**2.2**		**5.5**	V
ΔV_{OTL}	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 600mA $V_{OUT\ (NOM)}$ +1V ≤ VIN ≤ 5.5V (Note 8)	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
I_{OUT}	Maximum Output Current	Average DC Current Rating	**600**			mA
I_{LIMIT}	Output Current Limit		**620**	700		mA
I_Q	Supply Current	I_{OUT} = 0mA		50		µA
		I_{OUT} = 600mA		225		
	Shutdown Supply Current	V_{OUT} = 0V, EN = GND		0.001	1	
V_{DO}	Dropout Voltage I_{OUT} = 600mA	V_{OUT} = 2.8V		644		mV
		V_{OUT} = 3.3V		580		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V (Note 9)	-0.1	0.02	0.1	%/V
	Load Regulation	100µA ≤ I_{OUT} ≤ 600mA		0.001		%/mA
e_n	Output Voltage Noise	I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz V_{OUT} = 3.3V,Cbypass = 33nF		63		μV_{RMS}

		I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz V_{OUT} = 3.3V,Cbypass = float		205		
VEN	EN Input Threshold	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V (Note 8)	**1.2**			V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V (Note 8)			**0.4**	
IEN	EN Input Bias Current	EN = GND or VIN		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			167		℃
	Thermal Shutdown Hysteresis			30		
T_{ON}	Start-Up Time	C_{OUT} = 10μF, V_{OUT} at 90% of Final Value		140		μs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: θ_{JA} is measured in the natural convection at TA=25℃ on a high effective thermal conductivity test board (2 layers , 2S0P) of JEDEC 51-7 thermal measurement standard.

Note 4: θ_{JC} represents the resistance to the heat flows the chip to package top case.

Note 5: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-23-5 package θ_{JA} = 135°C/W, T_J (MAX) = 150°C and using TA = 25°C, the maximum power dissipation is found to be 925mW. The derating factor (-1/θ_{JA}) = -7.4mW/°C, thus below 25°C the power dissipation figure can be increased by 7.4mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 6: Typical Values represent the most likely parametric norm.

Note 7: Human body model: 1.5kΩ in series with 100pF.

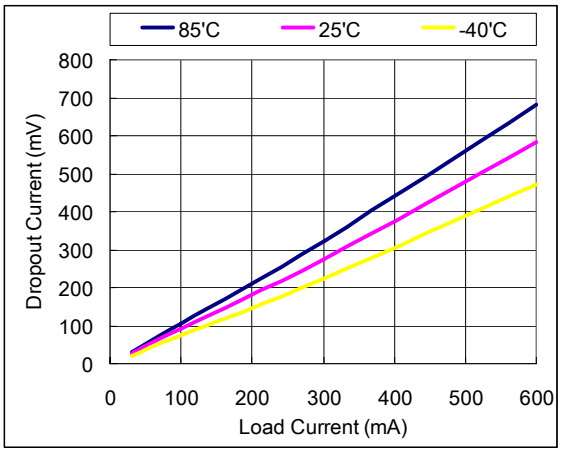
Note 8: Condition does not apply to input voltages below 2.2V since this is the minimum input operating voltage.

Note 9: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 1.8V.

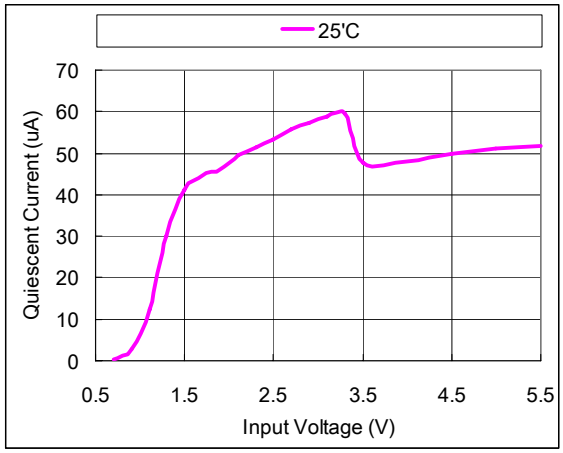
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2μF, C_{CC} = 33nF, T_A = 25°C, VEN = VIN.

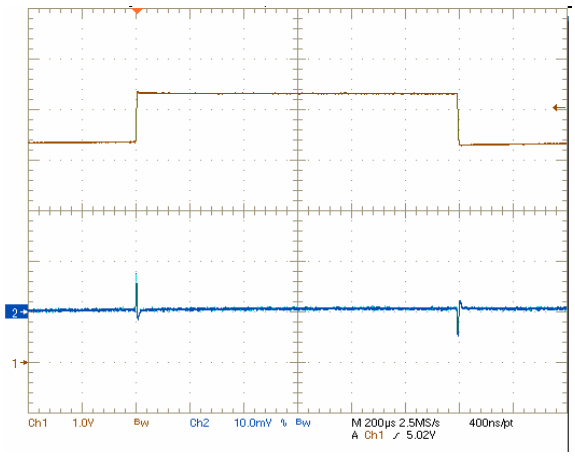
Dropout Voltage vs. Load Current (VOUT=3.3V)



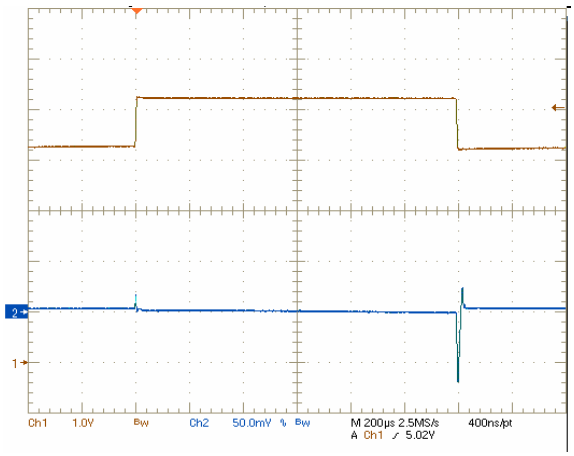
Quiescent Current vs. VIN (VOUT=3.3V)



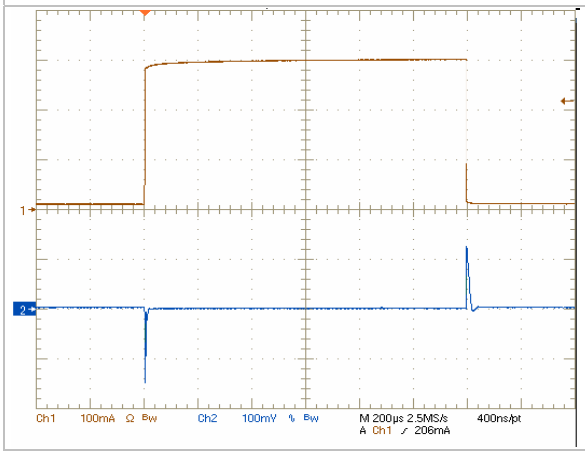
Line Transient (VOUT=3.3V, IOUT=10mA)



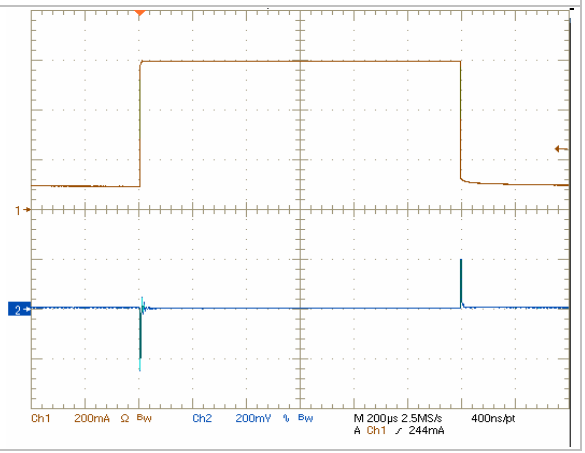
Line Transient (VOUT=3.3V, IOUT=600mA)



Load Transient (VOUT=3.3V, IOUT=10mA to 300mA)



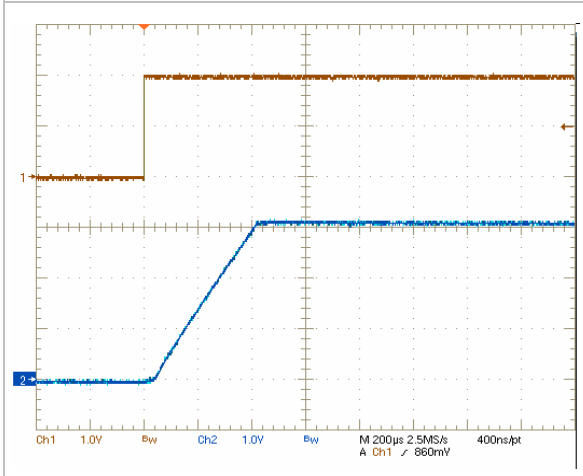
Load Transient (VOUT=3.3V, IOUT=100mA to 600mA)



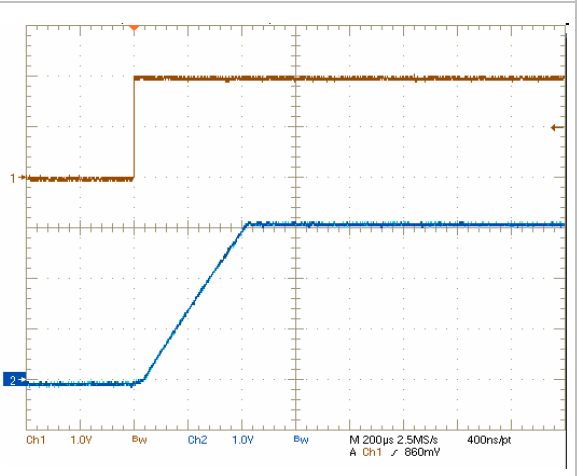
Typical Performance Characteristics (cont.)

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, VEN = VIN.

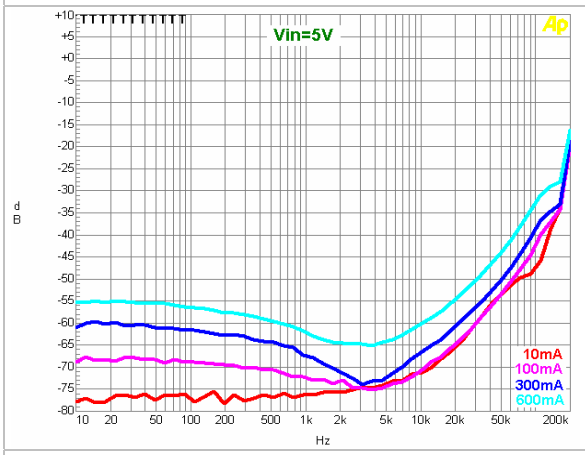
Enable Response (VOUT=3.3V, IOUT=0mA)



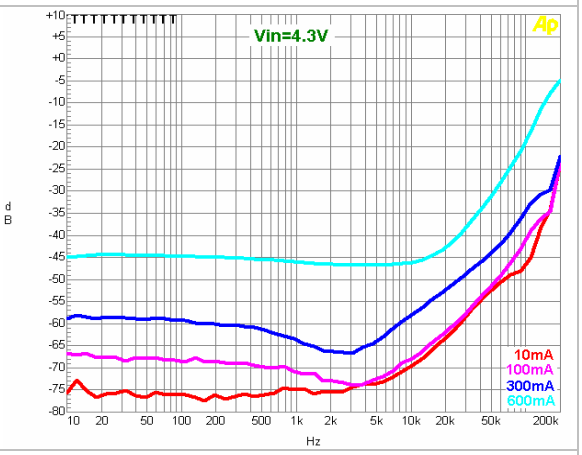
Enable Response (VOUT=3.3V, IOUT=100mA)



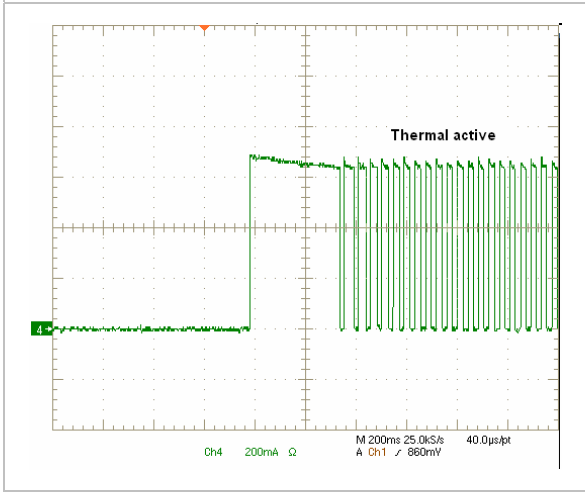
PSRR vs. Frequency (VIN=5.0V, VOUT=3.3V)



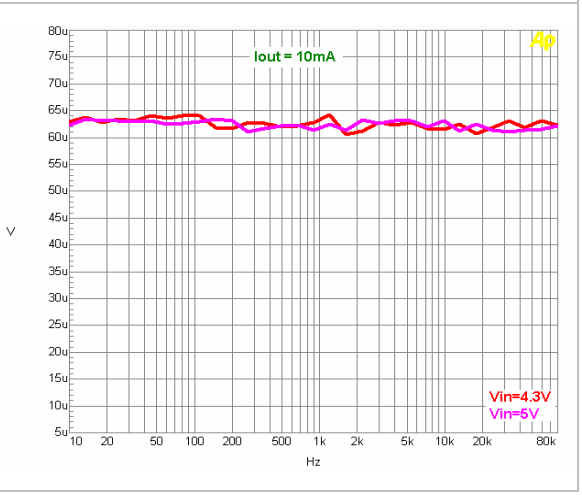
PSRR vs. Frequency (VIN=4.3V, VOUT=3.3V)



Current Limit (VOUT=3.3V)



Noise Level (VOUT=3.3V, IOUT=10mA)



Application Information

General Description

Referring to Fig.1as shown in the Functional Block Diagram section, the EMP8021 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

The EMP8021 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8021 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8021 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8021. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Compensation (Noise Bypass) Capacitor

Substantial reduction in the output voltage noise of the EMP8021 is accomplished through the connection of the noise bypass capacitor CC (10nF optimum) between pin 4 and the ground. Because pin 4 connects directly to the high

impedance output of the bandgap reference circuit, the level of the DC leakage currents in the CC capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the CC capacitor types for use with the EMP8021. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the CC capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Trade off exists between output noise level and turn-on time when selecting the CC capacitor value.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8021 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 167°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and TJ is as follows:

$T_J = \theta_{JA}$ (PD) + T_A

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$P_D = I_{OUT} (V_{IN} - V_{OUT})$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8021, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

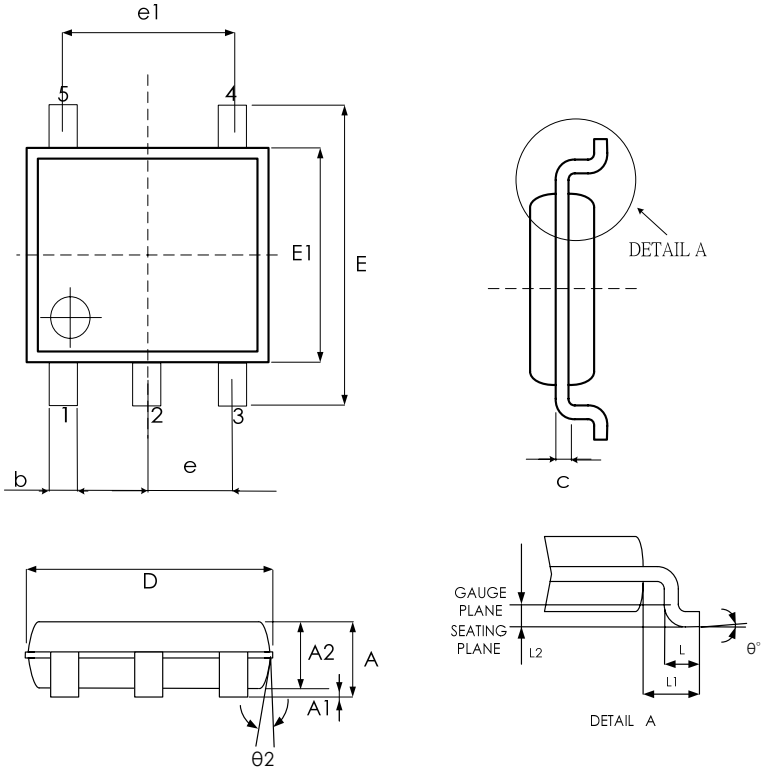
Shutdown

The EMP8021 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the EMP8021 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.4V. A minimum guaranteed voltage of 1.2V at the EN pin will activate the EMP8021. Direct connection of the EN pin to the VIN to keep the regulator on is allowed for the EMP8021. In this case, the EN pin must not exceed the supply voltage VIN.

Fast Start-Up

Fast start-up time is important for overall system efficiency improvement. The EMP8021 assures fast start-up speed when using the optional noise bypass capacitor (CC). To shorten start-up time, the EMP8021 internally supplies a current to charge up the capacitor until it reaches about 90% of its final value.

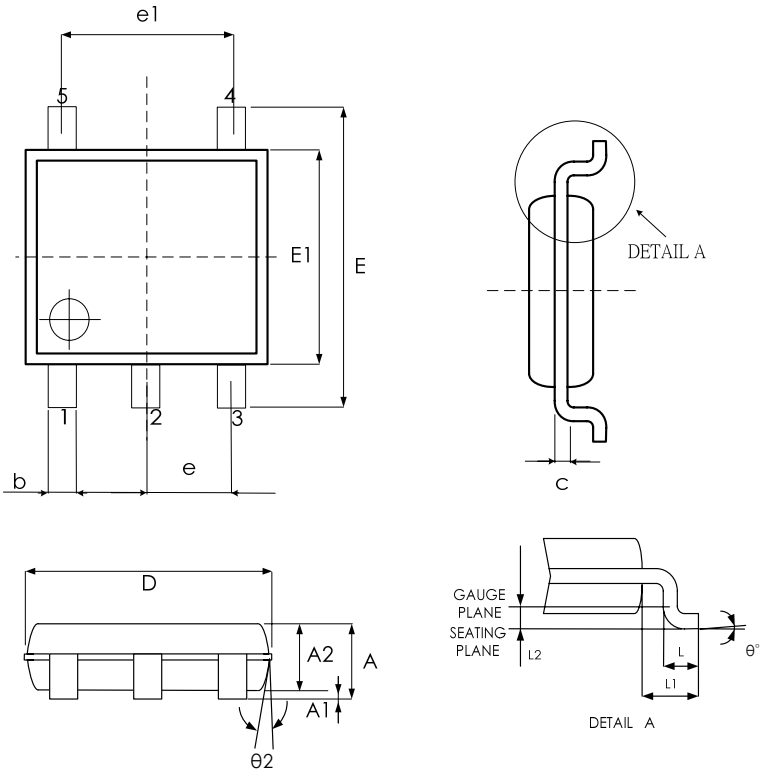
Package Outline Drawing
SOT-23-5



SYMBPLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0.05	0.10	0.15
A2	1.00	1.10	1.20
B	0.30	—	0.50
C	0.08	—	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
E	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
θ°	0	5	10
θ2°	6	8	10

UNIT: MM

Package Outline Drawing
SC-70-5



SYMBPLS	MIN.	NOM.	MAX.
A	0.8	—	1.10
A1	0	—	0.10
A2	0.8	0.90	1.00
B	0.15	—	0.30
C	0.08	—	0.22
D	1.85	2.00	2.15
E	1.8	2.10	2.40
E1	1.10	1.25	1.40
E	0.65 BSC		
e1	1.30 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
θ°	0	4	8
θ2°	4	—	12

UNIT: MM

Revision History

Revision	Date	Description
0.1	2010.1.13	Original
0.2	2010.08.27	1) Added 2.8V Vout version. 2) Added Dropout voltage for Vout=2.8V 3) Node. 9 item revised. 4) Modified I_{OUT} = 1mA, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V →I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V for Electrical Characteristics.
0.3	2011.04.20	Add 3.3V option for SC-70 package

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