High Input Voltage, Low Quiescent Current, Low-Dropout Linear Regulator

General Description

The EMP8040 is a high voltage, low quiescent current, low dropout regulator with 150mA output driving capacity. The EMP8040, which operates over an input range **up** to 40V, is stable with any capacitors, whose capacitance is larger than 1μF, and suitable for powering battery-management ICs because of the virtue of its low quiescent current consumption and low dropout voltage. EMP8040 also includes bandgap voltage reference, constant current limiting and thermal overload protection.

Ordering Information

Part Number	Remark
EMP8040	±2.5% output voltage tolerance
EMP8040B	±1.0% output voltage tolerance

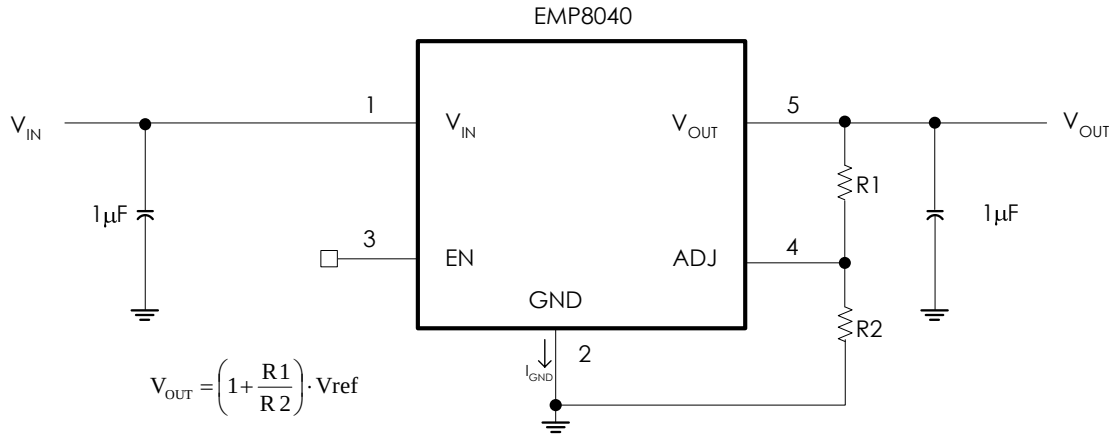
Applications

- Logic Supply for High Voltage Batteries
- Keep-Alive Supply
- 3-4 Cell Li-ion Batteries Powered systems

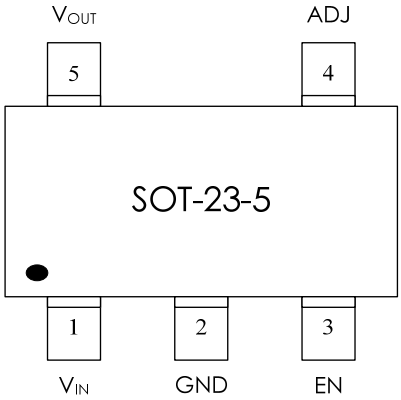
Features

- 150mA output current driving capacity
- 780mV typical dropout at Io=150mA
- 10μA typical quiescent current
- 1μA typical shutdown mode
- **Up** to 40V input range
- Stable with small ceramic output capacitors (1μF)
- Over temperature and over current protection

Typical Application



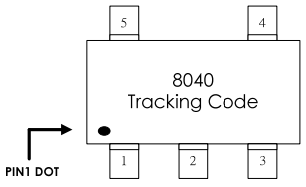
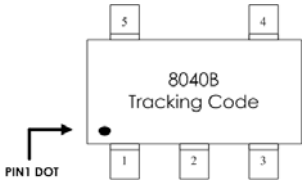
Connection Diagrams



Order information

EMP8040-XXVF05NRR**/ EMP8040B-XXVF05NRR**
XX Output voltage
VF05 SOT-23-5 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

Order, Marking & Packing Information

Package	Vout	Product ID.	Marking	Packing
SOT-23-5	ADJ	EMP8040-00VF05NRR		Tape & Reel 3Kpcs
		EMP8040B-00VF05NRR		

Pin Functions

Name	SOT-23-5	Function
VIN	**1**	**Supply Voltage Input** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	**2**	**Ground Pin**
EN	**3**	**Shutdown Input** Set the regulator into the disable mode by pulling the EN pin low. To keep the regulator on during normal operation, force this pin > 1V. Once the forcing voltage > 6V, there will be several micro-ampere leaking current.
ADJ	**4**	**Adjust:** Feedback input. Connect to resistive voltage-divider network.
VOUT	**5**	**Output Voltage**

Functional Block Diagram

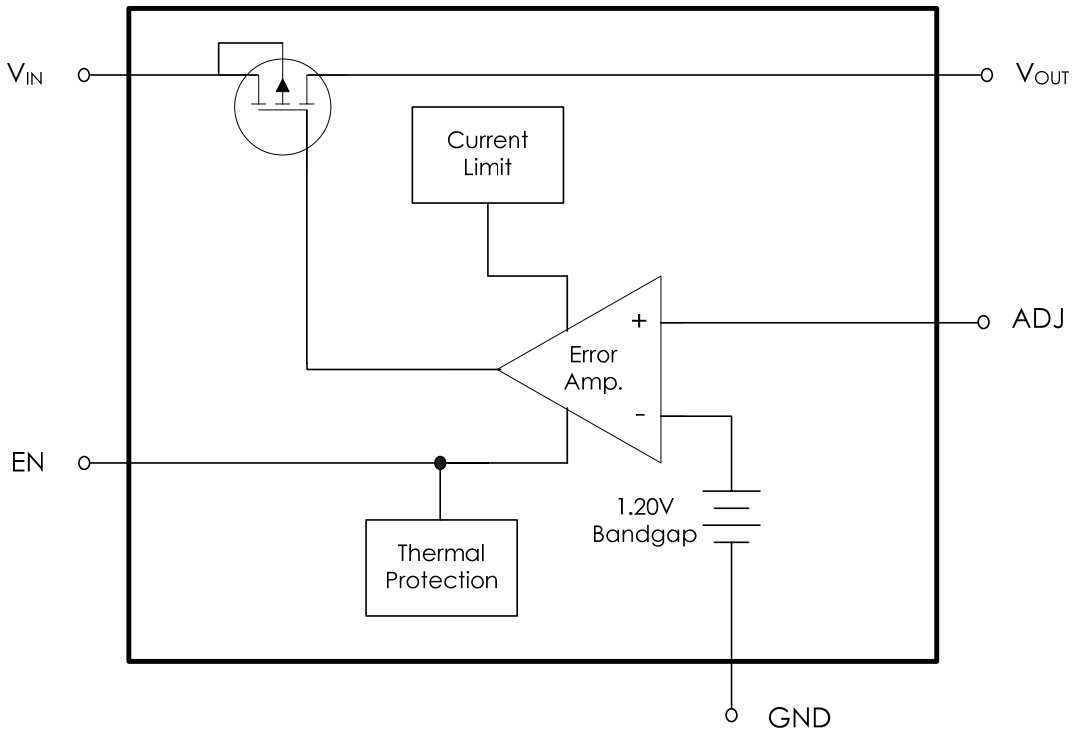


FIG.1. Functional Block Diagram of EMP8040

Absolute Maximum Ratings (Notes 1, 2)

V_{IN}, EN	-0.3V to 42V	Junction Temperature (T_J)	150°C
V_{OUT}	-0.3V to 13.2V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 3)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Model	2KV

Operating Ratings (Note 1, 2)

Supply Voltage (EMP8040)	3.0V to 40V	Thermal Resistance (θ_{JA})	
Supply Voltage (EMP8040B)	**2.7V to 40V**	SOT-23-5	152°C/W
Operating Temperature Range	-40°C to 85°C	Thermal Resistance (θ_{JC} , Note 3))	
		SOT-23-5	81°C/W

Electrical Characteristics

T_A = 25°C, V_{OUT}(NOM)=5V; unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V, EN = 2V, C_{IN} = C_{OUT} =1µF.

Symbol	Parameter	Conditions		Min	Typ (Note4)	Max	Units
ΔV_{OTL}	Output Voltage Tolerance	I_{OUT} = 10mA	EMP8040	-2.5		+2.5	% of
		$V_{OUT\ (NOM)}$ +1V ≤ V_{IN} ≤ 40V	**EMP8040B**	**-1**		**+1**	$V_{OUT\ (NOM)}$
Vref	Reference voltage		EMP8040	1.176	1.2	1.224	V
			EMP8040B	**1.188**	**1.200**	**1.212**	
I_{OUT}	Maximum Output Current	Average DC Current Rating		150			mA
I_{LIMIT}	Output Current Limit			300			mA
I_Q	Supply Current	I_{OUT} = 0.1mA			10	30	µA
		I_{OUT} = 100mA			50	100	
		I_{OUT} = 150mA			80	130	
	Shutdown Supply Current	V_{OUT} = 0V, EN = GND			1	5	
V_{DO}	Dropout Voltage V_{OUT}=5.0V (Note. 5)	I_{OUT} = 30mA			135		mV
		I_{OUT} = 100mA			500		
		I_{OUT} = 150mA			780		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 40V			0.1		%
	Load Regulation	0.1mA ≤ I_{OUT} ≤ 100mA			0.5		%
e_n	Output Voltage Noise	I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz V_{OUT} = 5.0V			800		μV_{RMS}
V_{EN}	EN Input Threshold	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 40V		1.0			V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 40V				0.3	
I_{EN}	EN Input Bias Current	EN = GND or V_{IN} (V_{IN}<6V)			0.1		µA
		EN = V_{IN} (40V>V_{IN}>6V)				35	
T_{SD}	Thermal Shutdown Temperature				160		℃
	Thermal Shutdown Hysteresis				30		
t_{ON}	Start-Up Time	C_{OUT} = 1.0µF, V_{OUT} at 90% of Final Value			500		µs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-23-5 package θ_{JA} = 152°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 822mW. The derating factor (-1/θ_{JA}) = -6.57mW/°C, thus below 25°C the power dissipation figure can be increased by 6.57mW per degree, and similarity decreased by this factor for temperatures above 25°C.

- θ_{JC} represents the resistance between the chip and the top of the package case.

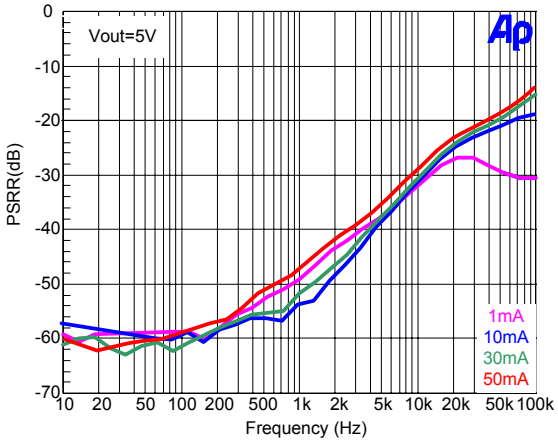
Note 4: Typical Values represent the most likely parametric norm

Note 5: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops to 98% its nominal value.

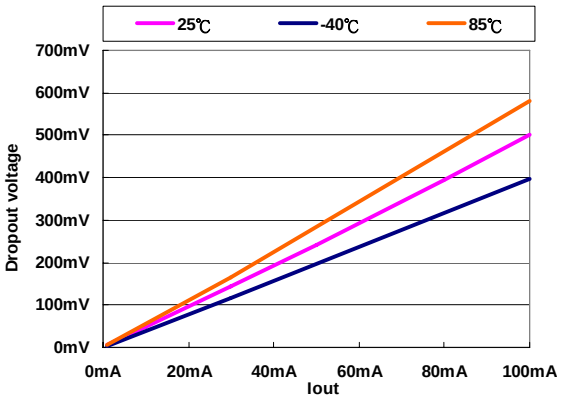
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

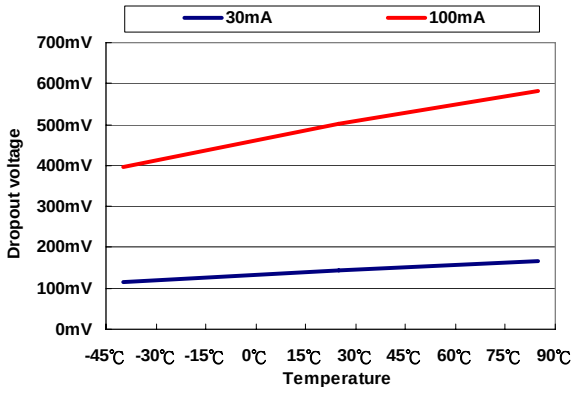
PSRR vs. Frequency (V_{IN}=6V, V_{OUT}=5V)



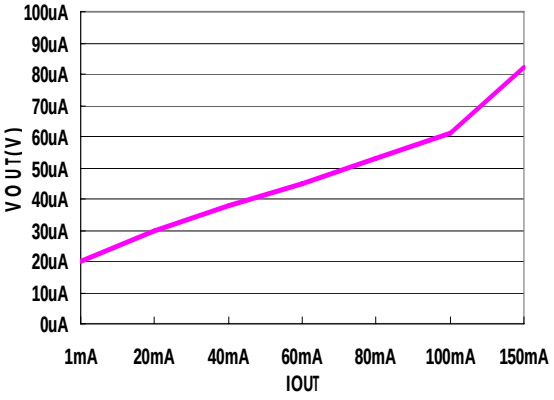
Dropout Voltage vs. Load Current (V_{OUT}=5.0V)



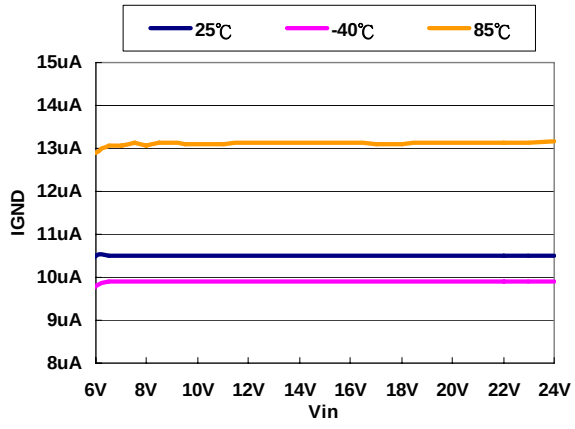
Dropout Voltage vs. Temp (V_{OUT}=5.0V)



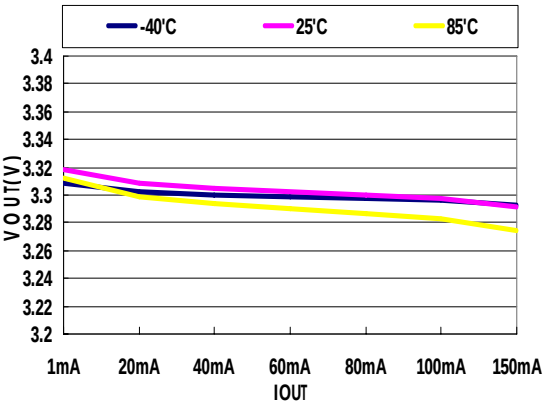
Ground Current vs. Iout (V_{OUT}=3.3V, T_A=25'C)



Ground Current vs. V_{IN} (V_{OUT}=5.0V)



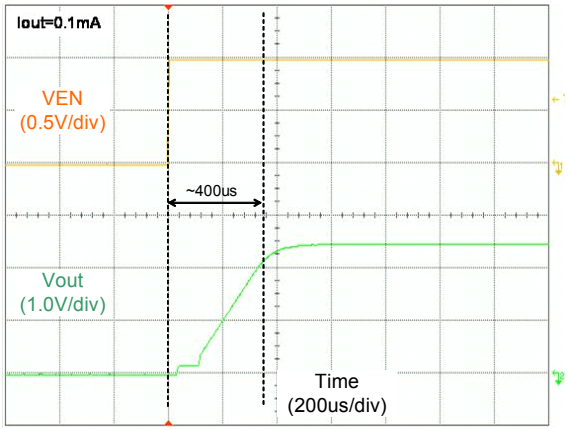
V_{OUT} vs. Iout (V_{OUT}=3.3V)



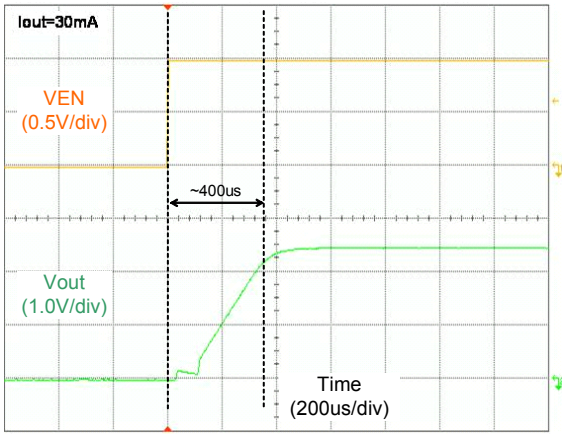
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

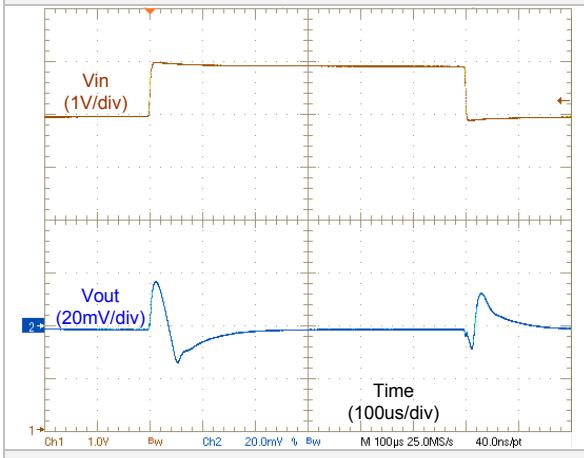
Enable Response (V_{OUT}=5.0V, IOUT=0.1mA)



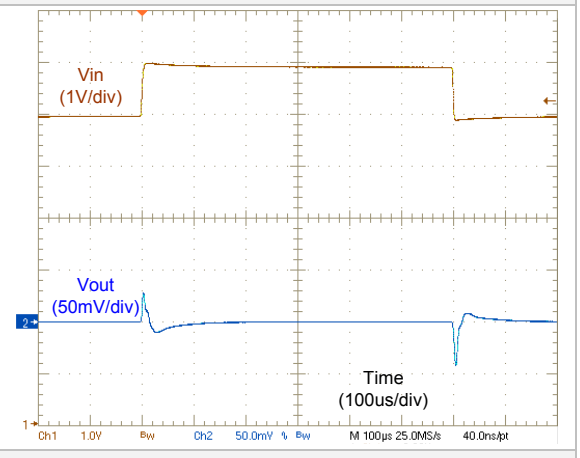
Enable Response (V_{OUT}=5.0V, IOUT=30mA)



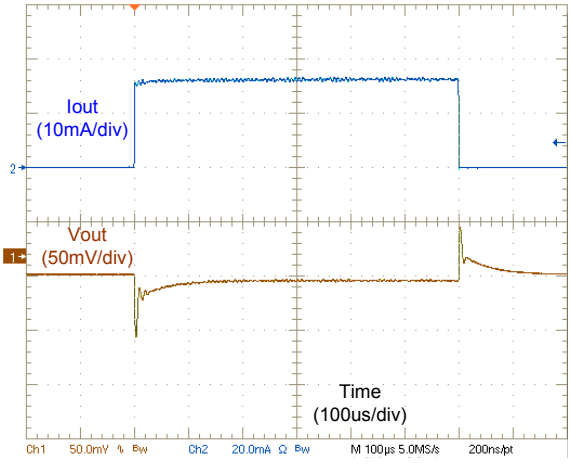
Line transient (Iout=1mA)



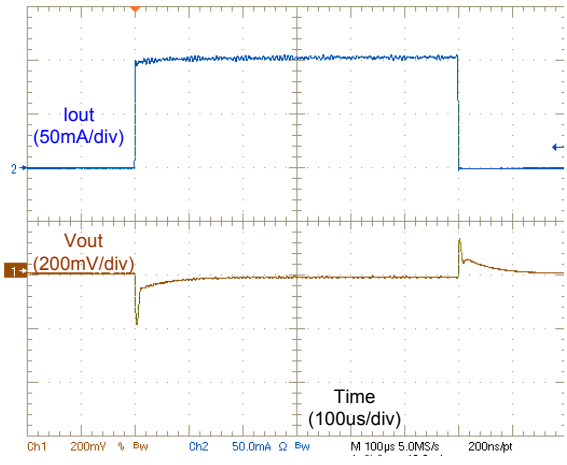
Line transient (Iout=30mA)



Load transient (V_{OUT}=5.0V)



Load transient (V_{OUT}=5.0V)



Application Information

General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the EMP8040 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By the virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

The EMP8040 is specially designed for use with ceramic output capacitors of as low as 1.0μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) is restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8040 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8040 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8040. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8040 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature T_J exceeding 150°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA} \times (P_D) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

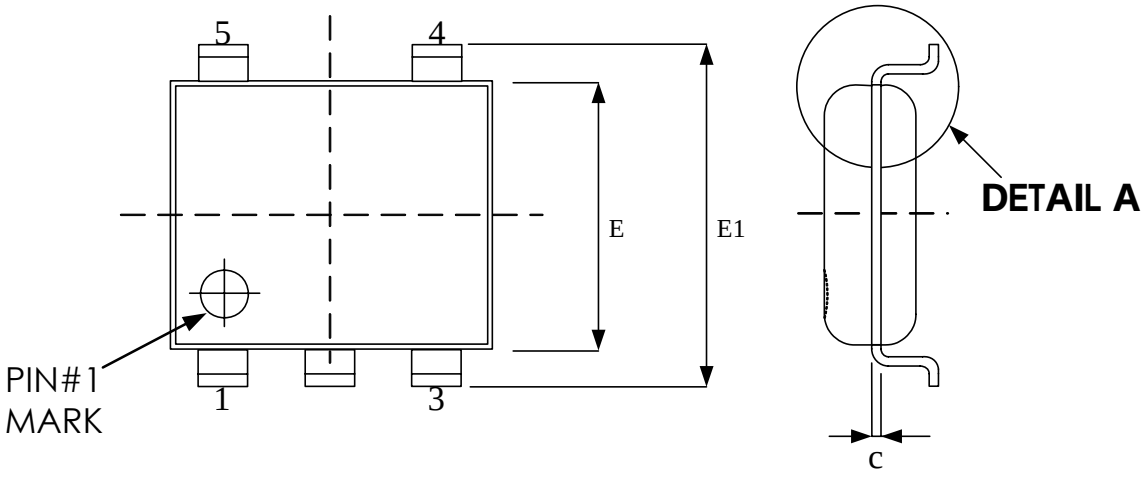
$$P_D = I_{OUT} (V_{IN} - V_{OUT})$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8040, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

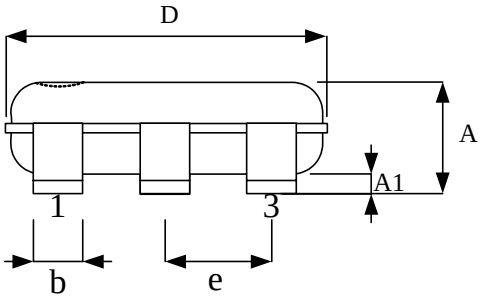
Shutdown

The EMP8040 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1μA. Such a low supply current makes the EMP8040 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.3V. A minimum guaranteed voltage of 1.0V at the EN pin will activate the EMP8040. Direct connection of the EN pin to the V_{IN} to keep the regulator on is allowed for the EMP8040, but there will be several micro-ampere leaking current for V_{IN} to GND when V_{IN} > 6V.

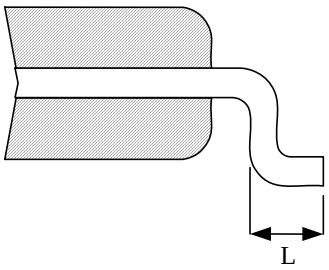
Package Outline Drawing
SOT-23-5



TOP VIEW



SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Revision History

Revision	Date	Description
0.1	2011.01.06	Original
1.0	2011.02.23	1. Skip “Preliminary” 2. Revise page3 “FIG.1” 3. Revise page4 “Electrical Characteristics”
1.1	2011.12.13	1) Modified 100mA output driving capacity to 150mA. 2) Modified the output voltage accuracy is based on Iout=10mA this condition. 3) Added Iout=150mA spec. into electrical characteristics table. 4) Updated the OT temperature from 150’C to 160’C.
1.2	2012.03.29	1) Modified the operating voltage from 36V to 40V. 2) Modified the absolute maximum ratings V_{IN}, EN from 40V to 42V. 3) Updated the package outline drawing.
1.3	2013.10.17	Modify package outline drawing
1.4	**2017.06.26**	**Added EMP8040B series product**

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