

## 2 Channel Power Management IC For Portable Devices

### GENERAL DESCRIPTION

The EMQ9920 is a high efficiency, 2-channel power management IC for battery-powered, portable devices application. It integrates two high efficiency step-down DC/DC converters.

The two Synchronous Buck converters (CH3, CH4) operate from 2.5V to 5.5V input voltage, up to 600mA loading capability and regulate adjustable output voltage from 0.6V to 5.5V. It features low quiescent current, 1.5MHz internal frequency operation.

The EMQ9920 is available in TQFN16 3x3 package. It is **Green compliant** (RoHS and Halogen-free).

### FEATURES

#### Two Synchronous Buck Converters

- Achieve 95% efficiency
- Input Voltage : 2.5V to 5.5V
- Output Current up to 600mA
- Reference voltage 0.6V
- Quiescent Current 200  $\mu$  A with No Load
- Internal switching frequency 1.5MHz
- No Schottky Diode needed
- Low Dropout Operation: 100% Duty Cycle
- Shutdown current < 1  $\mu$  A
- Excellent Line and Load Transient Response
- Over-temperature Protection

### APPLICATIONS

- Blue-Tooth devices
- Cellular and Smart Phones
- Personal multi-media Player (PMP)
- Wireless networking
- Digital Still Cameras
- Portable applications

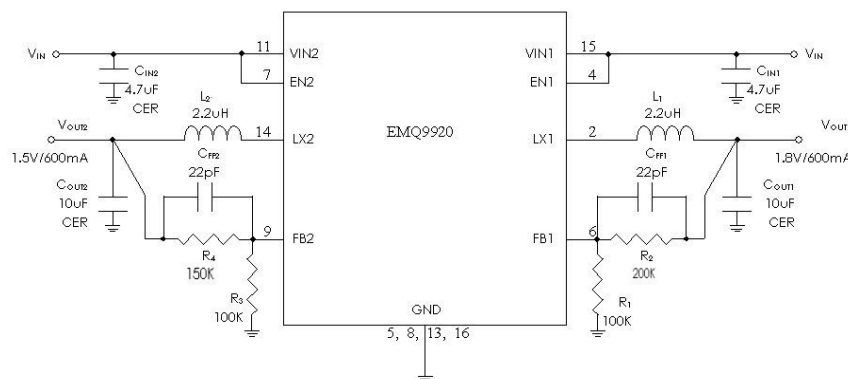
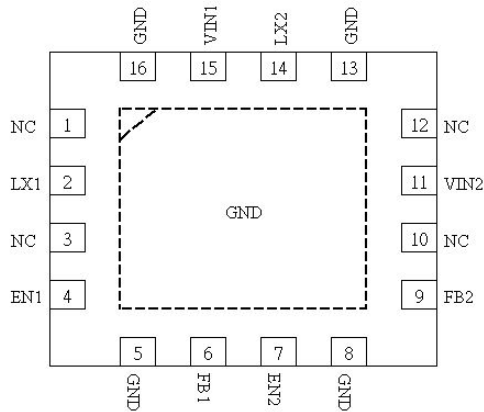


Figure 1. Typical Application

## CONNECTION DIAGRAM

TQFN16 3x3



## ORDER INFORMATION

EMQ9920-00HB16NRR

- 00 Adjustable output voltage
- HB16 TQFN16 Package
- N Green(RoHS and Halogen-free)
- R Commercial Grade Temperature  
Rating: -40 to 85°C
- R Package in Tape & Reel

## MARKING & PACKING INFORMATION

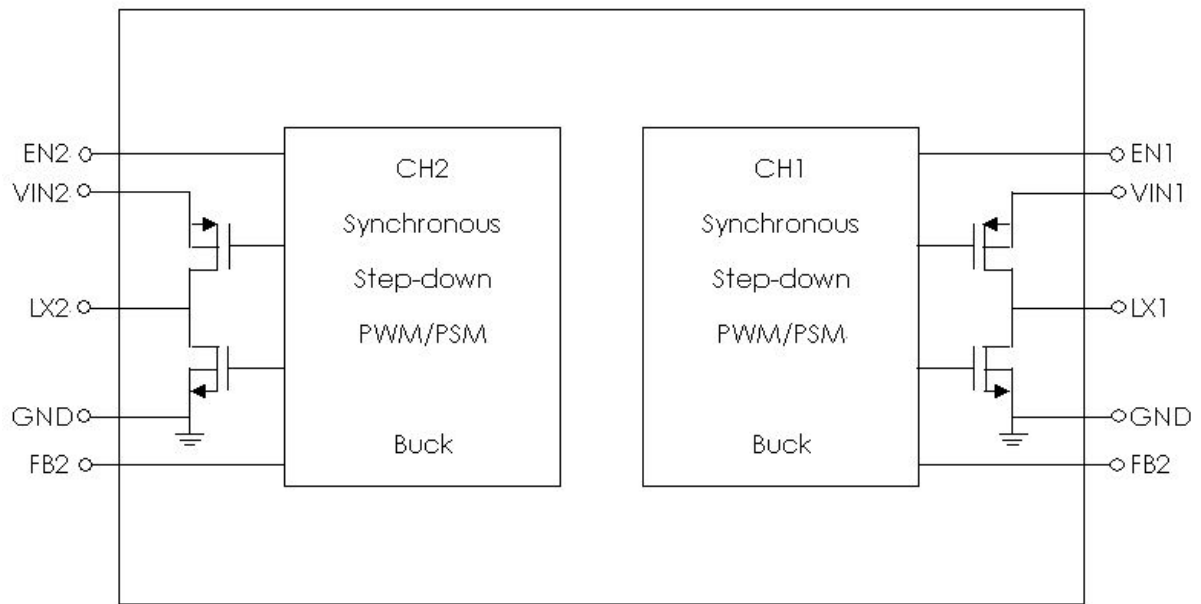
Package	Product ID	Marking	Packing
TQFN16	EMQ9920-00HB16NRR	<div style="border: 1px solid black; padding: 5px; display: inline-block;"> <p style="text-align: center;">EMP EMQ9920 Tracking Code</p> </div> <p>Pin#1 →</p>	5K units Tape & Reel

## TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
NC	1, 3, 10, 12	N/A	Non-connection.
LX1	2	O	CH1 Switch PIN. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
EN1	4	I	CH1 Enable Input. Minimum 1.3V to enable the device. Maximum 0.5V to shut down the device. Do not leave this pin floating and enable the chip after $V_{IN1}$ is in the input voltage range.
GND	5, 8, 13, 16	I	Ground PIN.
FB1	6	I	CH1 Voltage Feedback PIN.

			Receives the feedback voltage from an external resistive divider across the output $V_{OUT1}$ .
EN2	7	I	CH2 Enable Input. Minimum 1.3V to enable the device. Maximum 0.5V to shut down the device. Do not leave this pin floating and enable the chip after $V_{IN2}$ is in the input voltage range.
FB2	9	I	CH2 Voltage Feedback PIN. Receives the feedback voltage from an external resistive divider across the output $V_{OUT1}$ .
VIN2	11	I	CH2 Input Voltage. Must be closely decoupled to GND pin with a 4.7 $\mu$ F or greater ceramic capacitor.
LX2	14	O	CH2 Switch PIN. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VIN1	15	I	CH1 Input Voltage. Must be closely decoupled to GND pin with a 4.7 $\mu$ F or greater ceramic capacitor.

## FUNCTION BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (VIN1, VIN2)	-0.3V to 6.0V	ESD Susceptibility	TBD
LX1 Switch PIN Voltage	-0.3V to (VIN1+0.3V)	Junction Temperature	150°C
LX2 Switch PIN Voltage	-0.3V to (VIN2+0.3V)	Thermal Resistance	
Other I/O PIN Voltage	-0.3V to VIN (VIN1, VIN2)	$\theta_{JA}$ (TQFN16 3x3)	55°C/W
Storage Temperature	-65°C to +150°C	Operating Ratings	
Switch Source Current (DC)	800mA	Temperature Range	-40°C $\leq$ TA $\leq$ 85°C
Switch Sink Current (DC)	800mA	Supply Voltage (VIN1, VIN2)	2.5V $\leq$ VDD $\leq$ 5.5V

## ELECTRICAL CHARACTERISTICS

Apply for  $V_{IN1} = 3.6V$ ,  $V_{IN2} = 3.6V$  and  $T_A = 25^\circ C$  (unless otherwise noted), Boldface limits apply for the operating temperature extremes:  $-40^\circ C$  and  $85^\circ C$ .

Symbol	Parameter	Conditions	EMQ9920			Units
			Min	Typ	Max	
<b>CH1 (Note 4)</b>						
$I_{FB1}$	Feedback Current				$\pm 30$	nA
$V_{FB1}$	Regulated Feedback Voltage	$T_A = 25^\circ C$	0.588	0.600	0.612	V
		$-40^\circ C \leq T_A \leq 85^\circ C$	<b>0.585</b>	<b>0.600</b>	<b>0.615</b>	
$\Delta V_{FB1}$	Reference Voltage Line Regulation	$V_{IN1} = 2.5V$ to $5.5V$			<b>0.4</b>	%/V
$\Delta V_{OVL1}$	Output Over-voltage Lockout	$\Delta V_{OVL1} = V_{OVL1} - V_{FB1}$	20	50	80	mV
$\Delta V_{OUT1}$	Output Voltage Line Regulation	$V_{IN1} = 2.5V$ to $5.5V$			<b>0.4</b>	%/V
	Output Voltage Load Regulation			0.5		%
$I_{PK1}$	Peak Inductor Current	$V_{IN1} = 3V$ , $V_{FB1} = 0.5V$ or $V_{OUT1} = 90\%$ , Duty Cycle < 35%		1.0		A
$I_{Q1}$	Quiescent Current (Note 5)	$V_{FB1} = 0.5V$ or $V_{OUT1} = 90\%$		200	340	$\mu A$
	Shutdown	$V_{EN1} = 0V$ , $V_{IN1} = 4.2V$		0.1	1	$\mu A$
$f_{OSC1}$	Oscillator Frequency	$V_{FB1} = 0.6V$ or $V_{OUT1} = 100\%$	<b>1.2</b>	<b>1.5</b>	<b>1.8</b>	MHz
		$V_{FB1} = 0V$ or $V_{OUT1} = 0V$		<b>290</b>		kHz
$R_{PFET1}$	$R_{DS(ON)}$ of PMOS	$I_{LX1} = 100mA$		0.45	0.55	$\Omega$
$R_{NFET1}$	$R_{DS(ON)}$ of NMOS	$I_{LX1} = -100mA$		0.40	0.5	$\Omega$
$I_{LX1}$	LX1 Leakage	$V_{EN1} = 0V$ , $V_{LX1} = 0V$ or $5V$ , $V_{IN1} = 5V$			$\pm 1$	$\mu A$
$V_{EN1}$	EN1 Threshold		0.5		1.3	V
$I_{EN1}$	EN1 Leakage Current				$\pm 1$	$\mu A$
<b>CH2 (Note4)</b>						

I <sub>FB2</sub>	Feedback Current				±30	nA
V <sub>FB2</sub>	Regulated Feedback Voltage	T <sub>A</sub> = 25°C	0.588	0.600	0.612	V
		-40°C ≤ T <sub>A</sub> ≤ 85°C	<b>0.585</b>	<b>0.600</b>	<b>0.615</b>	
Δ V <sub>FB2</sub>	Reference Voltage Line Regulation	V <sub>IN2</sub> = 2.5V to 5.5V			<b>0.4</b>	%/V
Δ V <sub>OVL2</sub>	Output Over-voltage Lockout	Δ V <sub>OVL2</sub> = V <sub>OVL2</sub> - V <sub>FB2</sub>	20	50	80	mV
Δ V <sub>OUT2</sub>	Output Voltage Line Regulation	V <sub>IN2</sub> = 2.5V to 5.5V			<b>0.4</b>	%/V
	Output Voltage Load Regulation			0.5		%
I <sub>PK2</sub>	Peak Inductor Current	V <sub>IN2</sub> = 3V, V <sub>FB2</sub> = 0.5V or V <sub>OUT2</sub> = 90%, Duty Cycle < 35%		1.0		A
I <sub>Q2</sub>	Quiescent Current (Note 5)	V <sub>FB2</sub> = 0.5V or V <sub>OUT2</sub> = 90%		200	340	μA
	Shutdown	V <sub>EN2</sub> = 0V, V <sub>IN2</sub> = 4.2V		0.1	1	μA
f <sub>OSC2</sub>	Oscillator Frequency	V <sub>FB2</sub> = 0.6V or V <sub>OUT2</sub> = 100%	<b>1.2</b>	<b>1.5</b>	<b>1.8</b>	MHz
		V <sub>FB2</sub> = 0V or V <sub>OUT2</sub> = 0V		<b>290</b>		kHz
R <sub>PFET2</sub>	R <sub>DS(ON)</sub> of PMOS	I <sub>LX2</sub> = 100mA		0.45	0.55	Ω
R <sub>NFET2</sub>	R <sub>DS(ON)</sub> of NMOS	I <sub>LX2</sub> = -100mA		0.40	0.5	Ω
I <sub>LX2</sub>	LX2 Leakage	V <sub>EN2</sub> = 0V, V <sub>LX2</sub> = 0V or 5V, V <sub>IN2</sub> = 5V			±1	μA
V <sub>EN2</sub>	EN2Threshold		0.5		1.3	V
I <sub>EN2</sub>	EN2 Leakage Current				±1	μA

**Note 1:** Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

**Note 2:** All voltages are with respect to the potential at the ground pin.

**Note 3:** Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

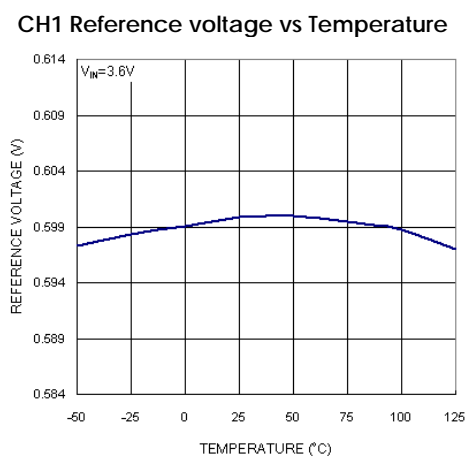
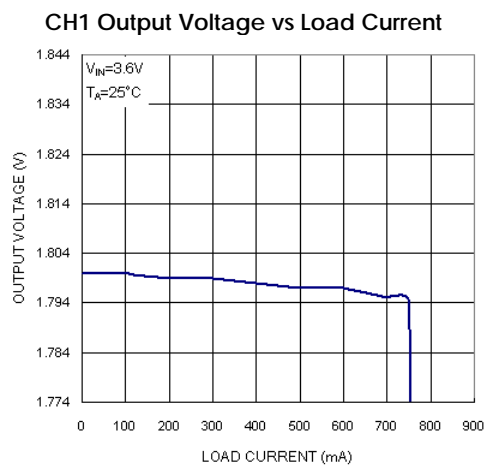
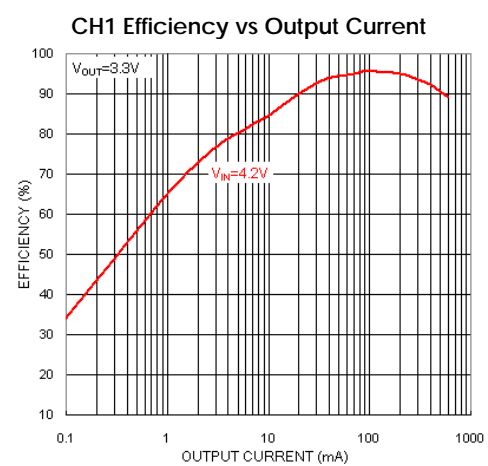
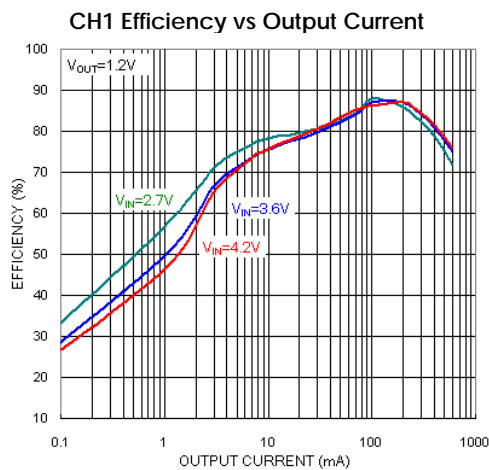
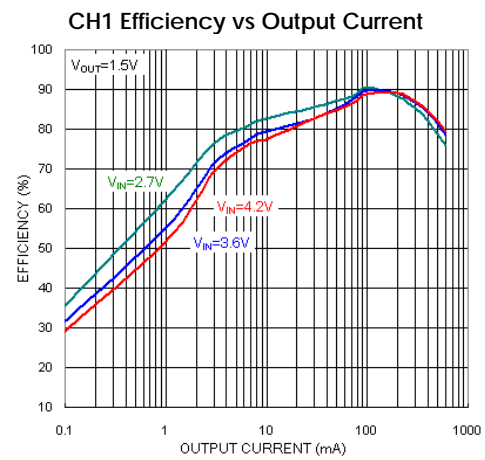
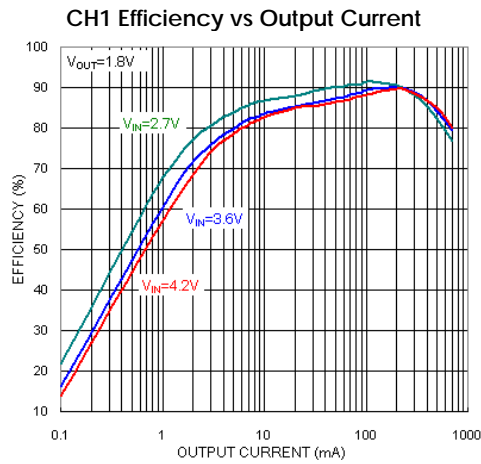
where T<sub>J(MAX)</sub> is the maximum junction temperature, T<sub>A</sub> is the ambient temperature, and θ<sub>JA</sub> is the junction-to-ambient thermal resistance.

**Note 4:** Build-in internal over-temperature protection to prevent over-load condition.

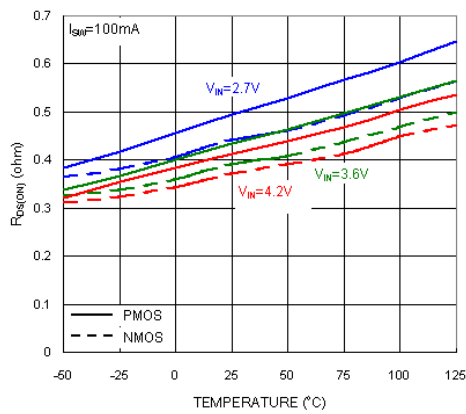
**Note 5:** Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.

## TYPICAL PERFORMANCE CHARACTERISTICS

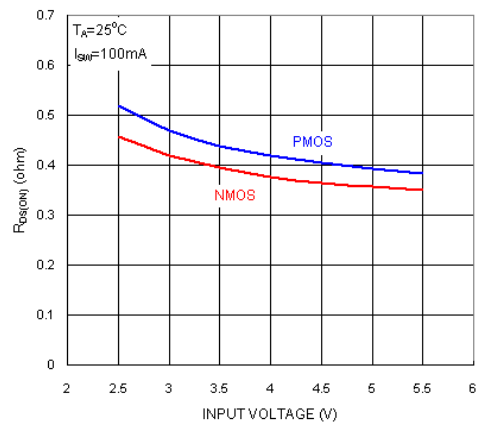
$V_{EN1} = V_{IN1}$ ,  $C_{IN1}=4.7\mu F$ ,  $L_1=2.2\mu H$ ,  $C_{OUT1}=4.7\mu F$ ,  $C_{IN2}=4.7\mu F$ ,  $L_2=2.2\mu H$ ,  $C_{OUT2}=4.7\mu F$ ,  $V_{EN2} = V_{IN2}$   $T_A = 25^\circ C$ , unless otherwise specified



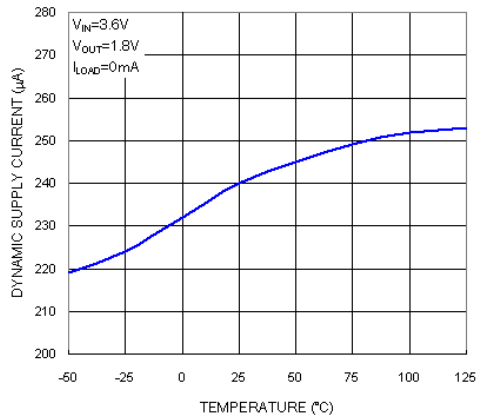
CH1 R<sub>DS(ON)</sub> vs Temperature



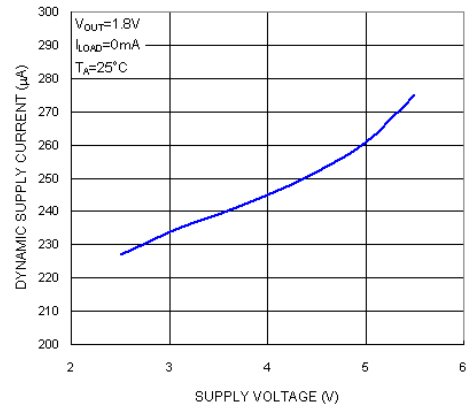
CH1 R<sub>DS(ON)</sub> vs Input Voltage



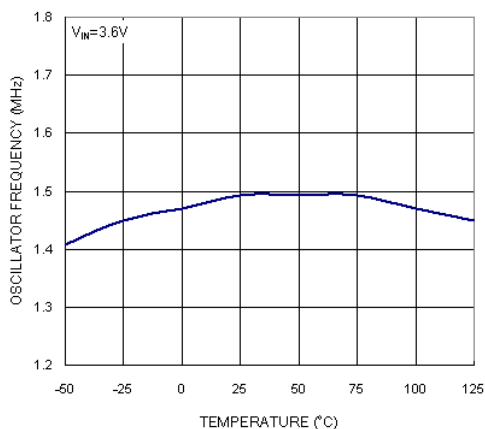
CH1 Dynamic Supply Current vs Temperature



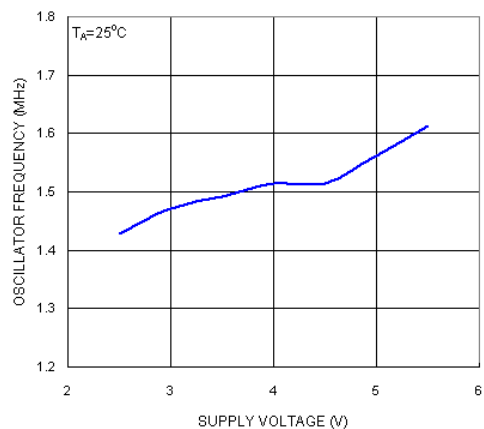
CH1 Dynamic Supply Current vs Supply Voltage



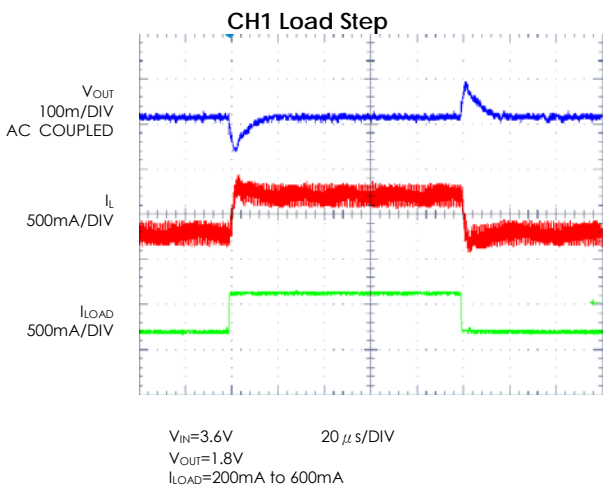
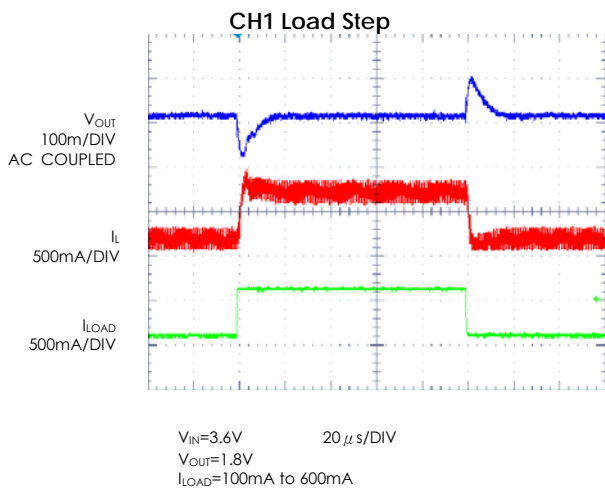
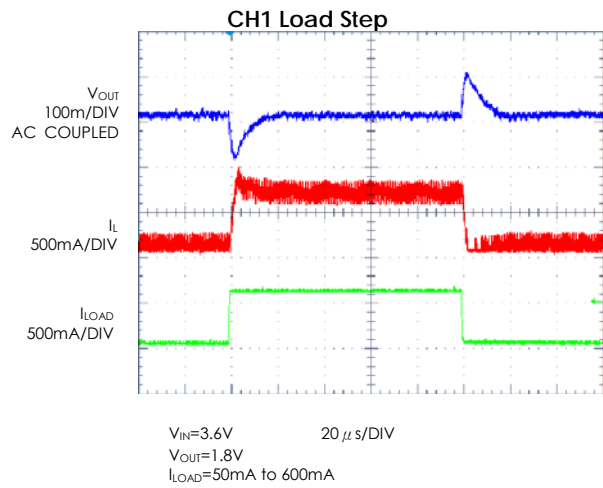
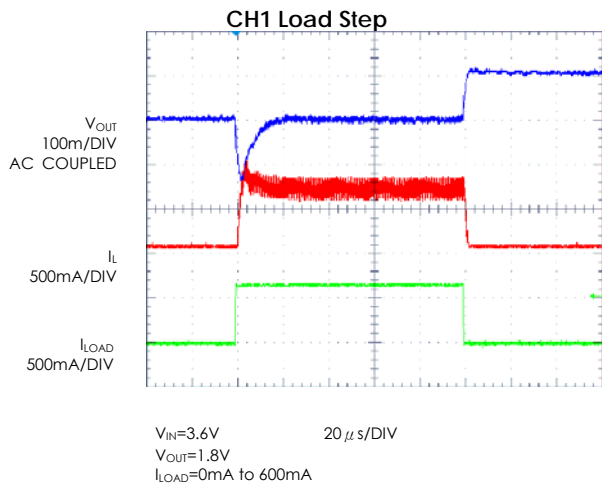
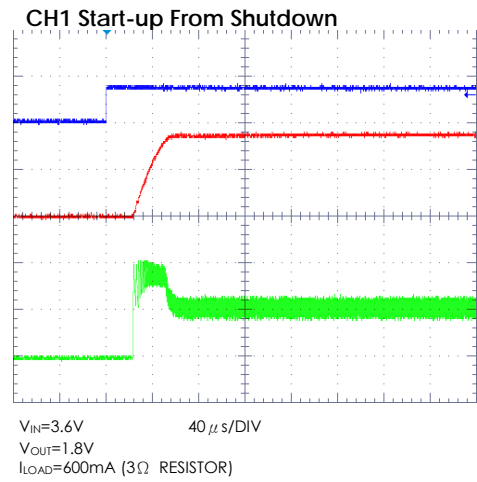
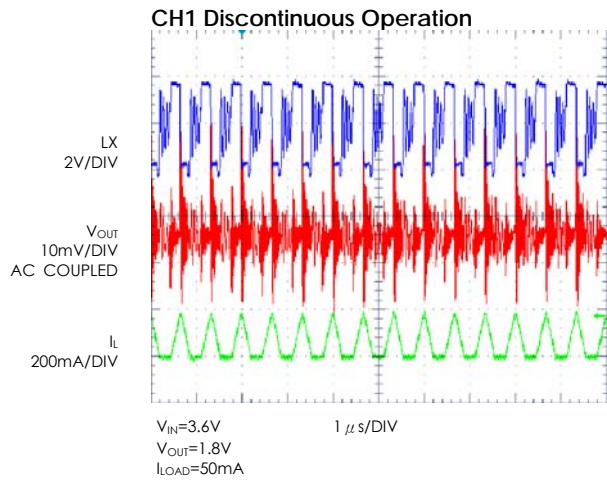
CH1 Oscillator Frequency vs Temperature

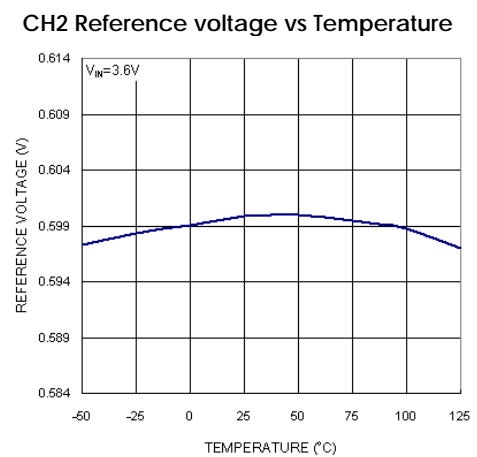
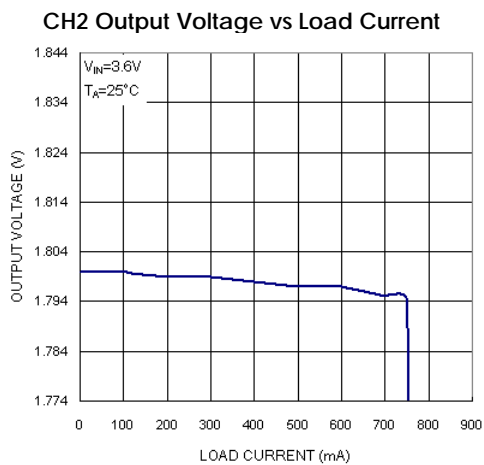
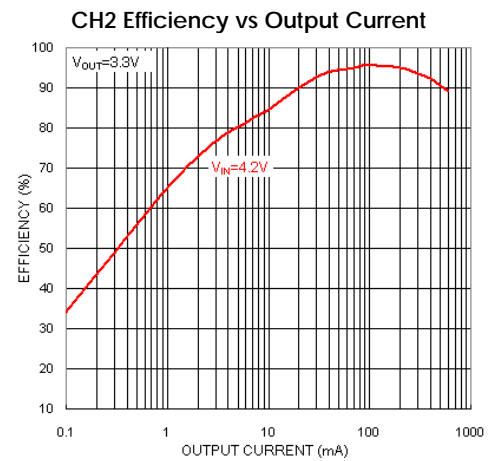
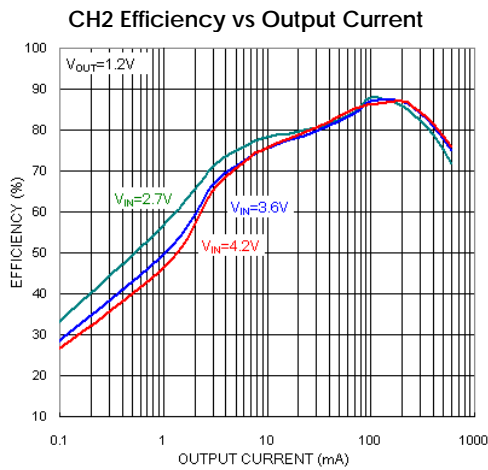
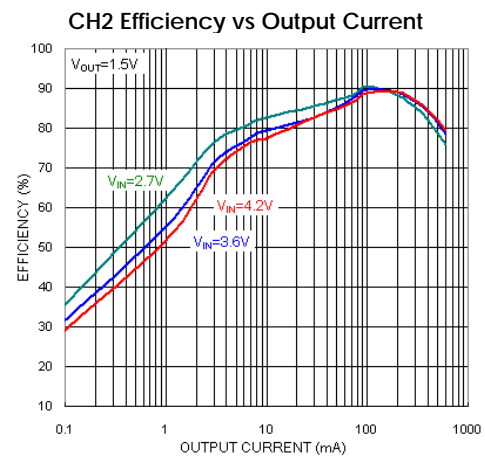
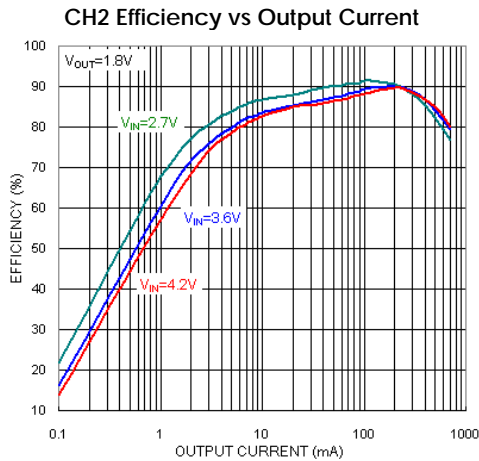


CH1 Oscillator Frequency vs Supply Voltage

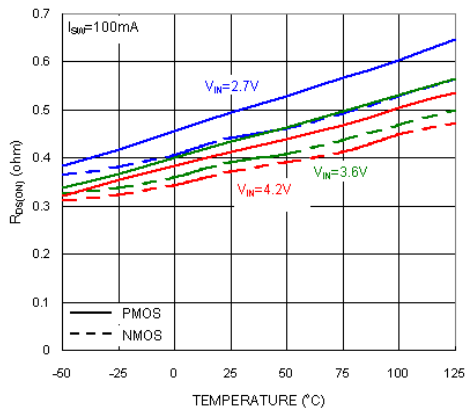




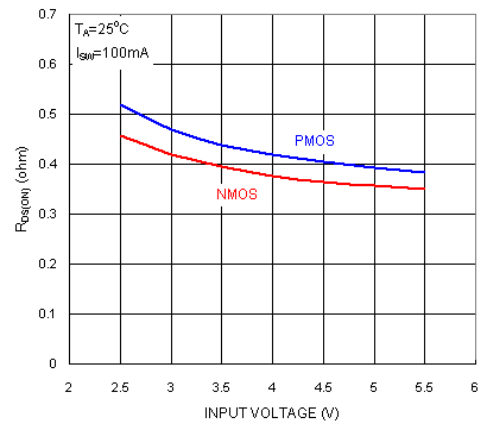




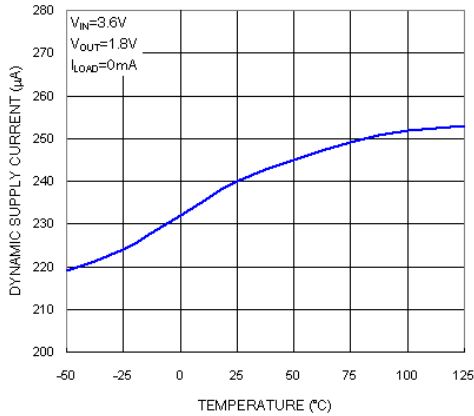
CH2 R<sub>DS(ON)</sub> vs Temperature



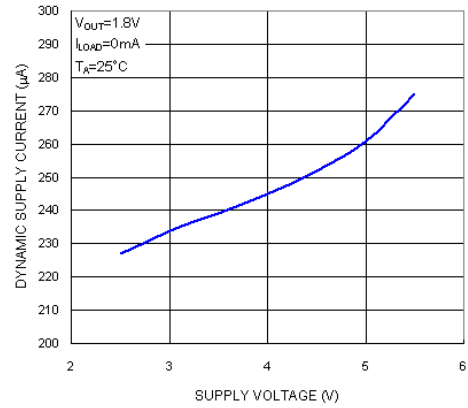
CH2 R<sub>DS(ON)</sub> vs Input Voltage



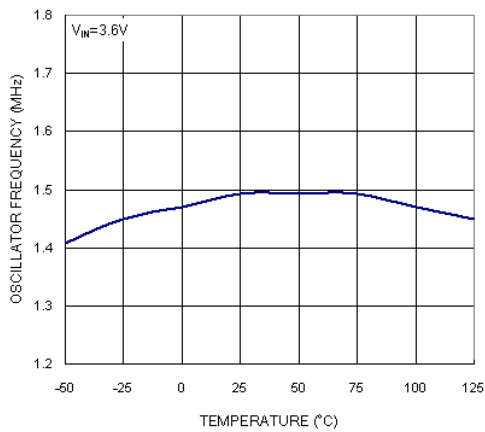
CH2 Dynamic Supply Current vs Temperature



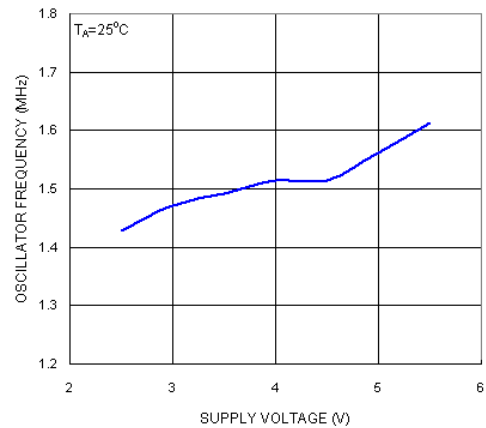
CH2 Dynamic Supply Current vs Supply Voltage

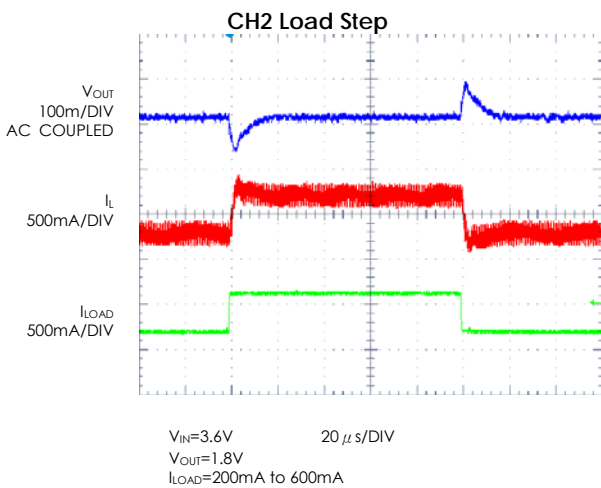
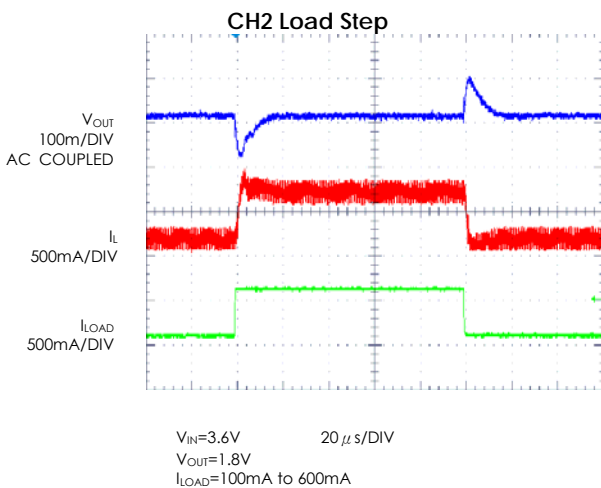
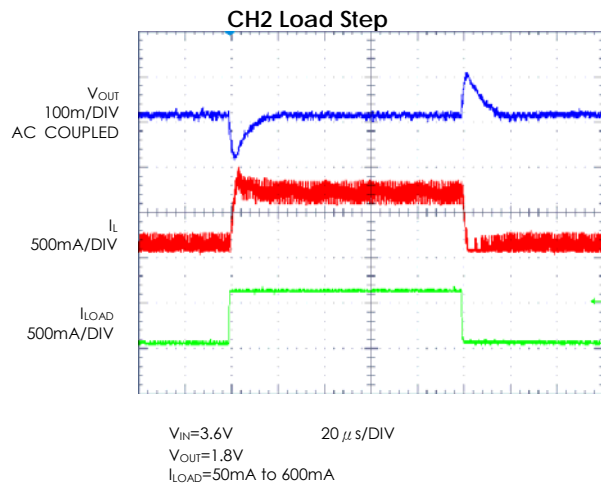
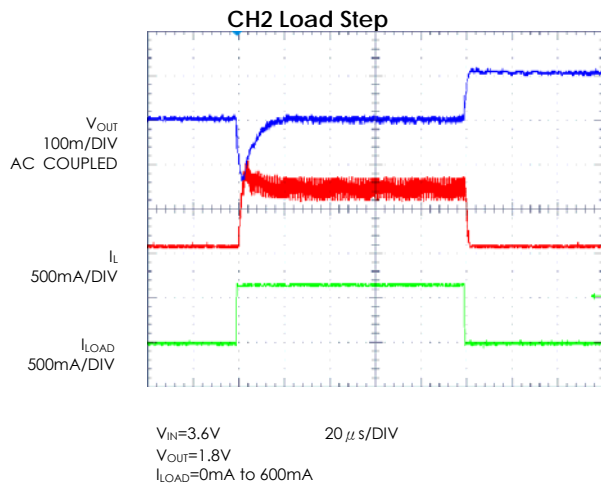
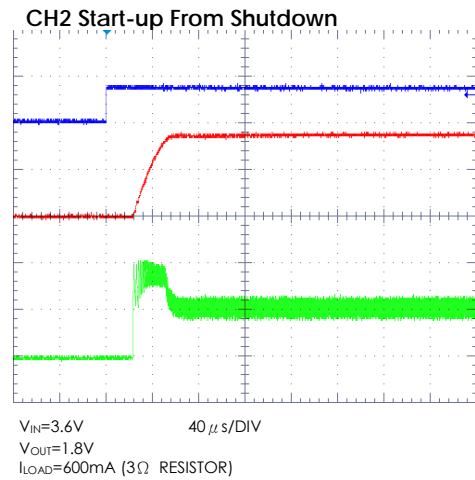
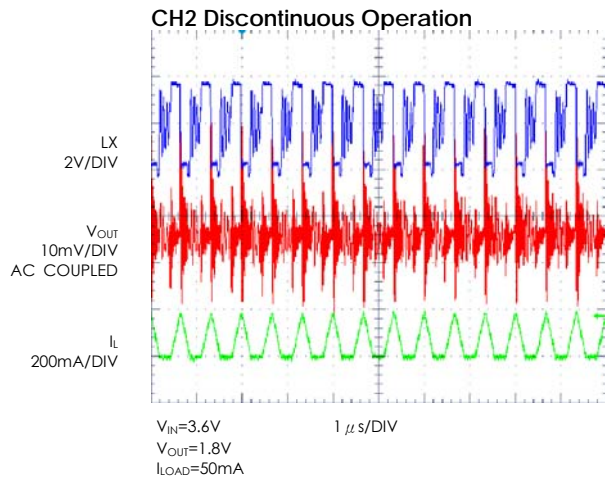


CH2 Oscillator Frequency vs Temperature



CH2 Oscillator Frequency vs Supply Voltage





## APPLICATION INFORMATION

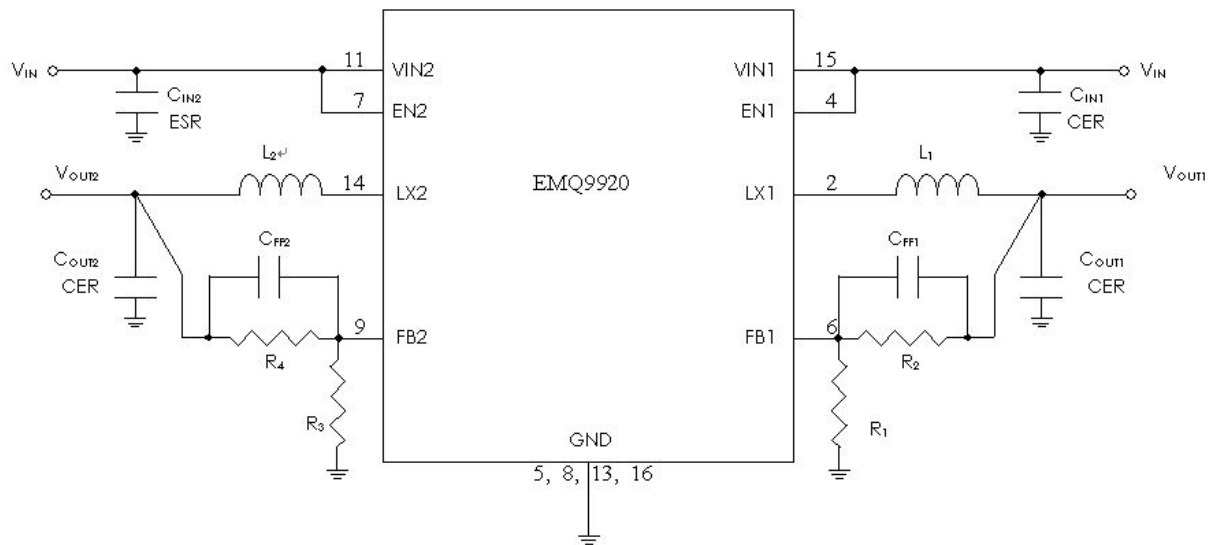


Figure 2. Typical EM9920 Application Circuit That Supports Two Adjustable Output Voltage

## Application Information

The EMQ9920 is a high efficiency, 2-channel power management IC for battery-powered, portable devices application.

The two channels are listed as following :

### CH1/2 : 600mA Synchronous Buck converters

All 2 channels are Vout adjustable

### CH1/2 : 600mA Synchronous Buck converters

The typical application circuit of the current mode DC/DC converters is shown in Fig.3.

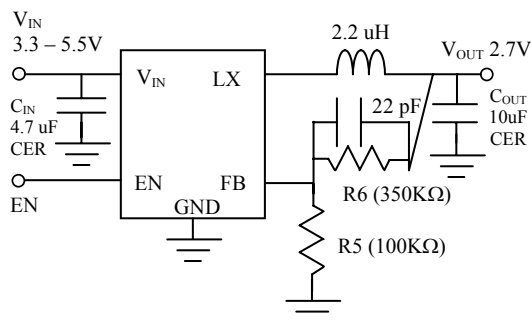


Fig. 3

### CH1, CH2 Inductor Selection

Basically, inductor ripple current and core saturation are two factors considered to decide the Inductor value.

$$\Delta I_L = \frac{1}{f \cdot L} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \dots\dots\dots (1)$$

The Eq. 1 shows the inductor ripple current is a function of frequency, inductance, VIN (VIN1, VIN2)

and VOUT (VOUT1, VOUT2). It is recommended to set ripple current to 40% of max. load current. A low ESR inductor is preferred.

### CH1, CH2 CIN and COUT Selection

A low ESR input capacitor can prevent large voltage transients at VIN (VIN1, VIN2). The RMS current of input capacitor is required larger than IRMS calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \dots\dots\dots (2)$$

ESR is an important parameter to select COUT (COUT1, COUT2). The output ripple ΔVOUT (ΔVOUT1, ΔVOUT2) is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \dots\dots\dots (3)$$

Higher values, lower cost ceramic capacitors are now available in smaller sizes. These ceramic capacitors have high ripple currents, high voltage ratings and low ESR that make them ideal for switching regulator applications. Optimize very low output ripple and small circuit size is doable from COUT selection since COUT does not affect the internal control loop stability. It is recommended to use the X5R or X7R which have the best temperature and voltage characteristics of all the ceramics for a given value and size.

### CH1, CH2 Output Voltage (VOUT1, VOUT2)

The output voltage can be determined by following equation:

$$V_{OUT} = 0.6 V \left( 1 + \frac{R_2}{R_1} \right) \dots\dots\dots (4)$$

CH1 Case, Replace R1 as R3, R2 as R4 in CH2 case.

### CH1, CH2 Thermal Considerations

Although thermal shutdown is build-in in the step-down DC/DC converter(s) that protects the device from thermal damage, the total power dissipation that the converter(s) can sustain should be base on the package thermal capability. The formula to ensure the safe operation is shown in Note 3.

To avoid the DC/DC converter(s) from exceeding the maximum junction temperature, the user will need to do some thermal analysis.

### CH1, CH2 Guidelines for PCB Layout

To ensure proper operation of the DC/DC converter(s), please note the following PCB layout

guidelines:

1. The GND trace, the LX (LX1, LX2) trace and the  $V_{IN}$  ( $V_{IN1}$ ,  $V_{IN2}$ ) trace should be kept short, direct and wide.
2.  $V_{FB}$  (FB1, FB2) pin must be connected directly to the feedback resistors. Resistive divider  $R_1/R_2$  (CH1);  $R_3/R_4$  (CH2) must be connected and parallel to the output capacitor  $C_{OUT}$  ( $C_{OUT1}$ ,  $C_{OUT2}$ ).
3. The Input capacitor  $C_{IN}$  ( $C_{IN1}$ ,  $C_{IN2}$ ) must be connected to pin  $V_{IN}$  ( $V_{IN1}$ ,  $V_{IN2}$ ) as closely as possible.
4. Keep LX (LX1, LX2) node away from the sensitive  $V_{FB}$  (FB1, FB2) node since this node is with high frequency and voltage swing.
5. Keep the (-) plates of  $C_{IN}$  ( $C_{IN1}$ ,  $C_{IN2}$ ) and  $C_{OUT}$  ( $C_{OUT1}$ ,  $C_{OUT2}$ ) as close as possible.

### CH1, CH2 Self-Enable Application

A self-enable function could be used when the step-down DC/DC converter(s) is (are) connected as fig. 4.

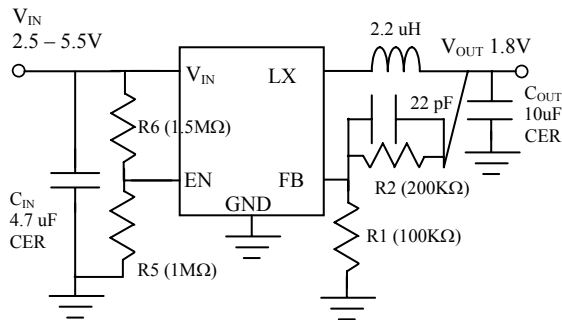


Fig. 4

The resistor ratio  $R_5:R_6=1:1.5$  is recommended.

### CH1, CH2 Design Example

Assume the Step-down DC/DC converter(s) is (are) used in a single lithium-ion battery-powered application. The  $V_{IN}$  ( $V_{IN1}$ ,  $V_{IN2}$ ) range will be about 2.7V to 4.2V. Output voltage ( $V_{OUT1}$ ,  $V_{OUT2}$ ) is 1.8V.

With this information we can calculate L using equation:

$$L = \frac{1}{f \cdot \Delta I_L} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

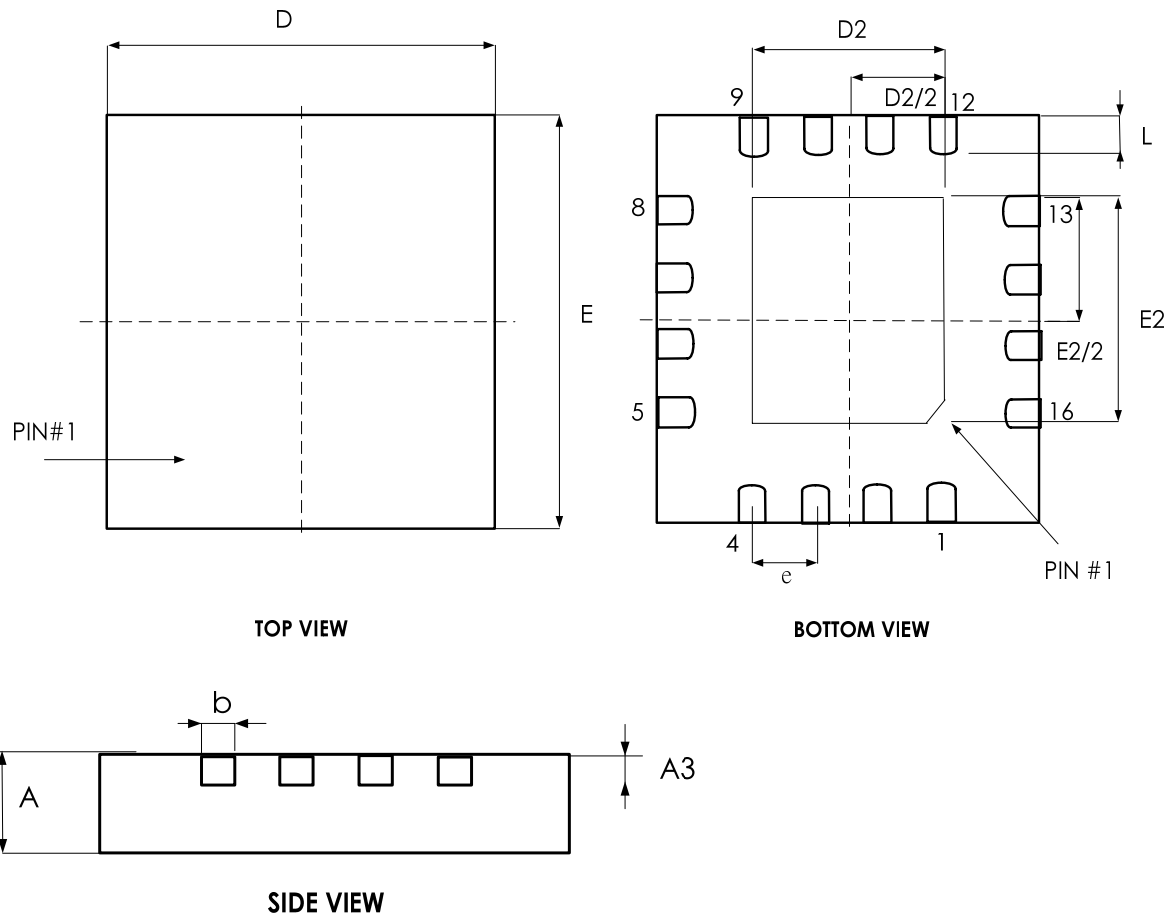
Substituting  $V_{OUT} = 1.8V$ ,  $V_{IN} = 4.2V$ ,  $I_L = 240mA$  and  $f = 1.5MHz$  in eq. 1 gives:

$$L = \frac{1.8V}{1.5MHz \cdot 240mA} \left( 1 - \frac{1.8V}{4.2V} \right) = 2.86\mu H$$

A 2.2 $\mu H$  inductor could be chose with this application.

A greater inductor with less equivalent series resistance makes best efficiency.  $C_{IN}$  ( $C_{IN1}$ ,  $C_{IN2}$ ) will require an RMS current rating of at least  $I_{LOAD(MAX)}/2$  and low ESR. In most cases, a ceramic capacitor will satisfy this requirement.

## TQFN-16 OUTLINE DIMENSION



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.027	0.029	0.031
A3	0.195	0.203	0.211	0.0077	0.0080	0.0083
b	0.180	0.230	0.300	0.007	0.009	0.012
D	2.950	3.000	3.050	0.116	0.118	0.120
E	2.950	3.000	3.050	0.116	0.118	0.120
e	0.50 BSC			0.020 BSC		
L	0.350	0.400	0.450	0.014	0.016	0.018
D2	1.500	1.625	1.750	0.059	0.064	0.069
E2	1.500	1.625	1.750	0.059	0.064	0.069

© Copyright 2007 All rights reserved.



## Revision History

Revision	Date	Description
2.0	2009.03.18	EMP transferred from version 1.0

## Important Notice

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of ESMT.

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.