2x15WStereo Class-D Audio Amplifier with Power Limit

Features

- Single supply voltage
  4.5V ~ 14.4V for loudspeaker driver
  Built-in LDO output 5V for others
- Loudspeaker power from 12V supply
  BTL Mode: 8W/CH into 8Ω @1% THD+N
  BTL Mode: 10W/CH into 6Ω @<1% THD+N
  BTL Mode: 12W/CH into 4Ω @<1% THD+N
  PBTL Mode: 16W/CH into 4Ω @1% THD+N
- Loudspeaker power from 12V supply
  BTL Mode: 10W/CH into 8Ω @10% THD+N
  BTL Mode: 14W/CH into 6Ω @10% THD+N
  BTL Mode: 15W/CH into 4Ω@<10% THD+N
  PBTL Mode: 20W/CH into 4Ω @10% THD+N
- 93% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

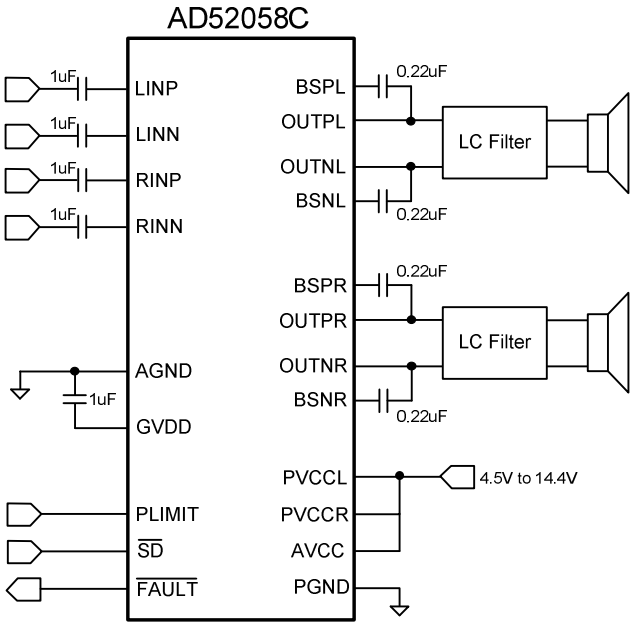
Description

The AD52058C is a high efficiency stereo class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~14.4V supply voltage. It can deliver 15W/CH output power into 4Ω loudspeaker within 10% THD+N at 12V supply voltage and without external heat sink when playing music.

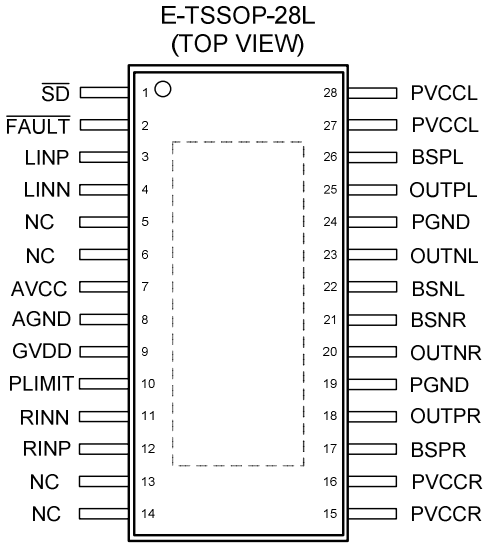
The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress.AD52058C provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

NAME	E-TSSOP -28L	TYP	DESCRIPTION
$\overline{SD}$	1	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	3	I	Positive audio input for left channel.
LINN	4	I	Negative audio input for left channel.
NC	5	NA	NC pin.
NC	6	NA	NC pin.
AVCC	7	P	Analog supply.
AGND	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	O	5V regulated output, also used as supply for PLIMIT function.
PLIMIT	10	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V_{PLIMIT}0.3~2.7V to set power limit level. Connect to GVDD (>3V) or GND (<0.26V) to disable power limit function.
RINN	11	I	Negative audio input for right channel.
RINP	12	I	Positive audio input for right channel.
NC	13	NA	NC pin.
NC	14	NA	NC pin.
PVCCR	15,16	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.

BSPR	17	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19	P	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24	P	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high side FET.
PVCCL	27,28	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
Thermal Pad		P	Must be soldered to PCB's ground plane.

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD52058C-26QG28NRR	E-TSSOP 28L	2500 Units / Reel 1reel/small box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L	AD52058C	28	27.1	1.33	Yes (Note 1)

Note 1.1: ***The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.***

Note 1.2: ***θ_{JA} is simulatedon a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.***

Note 1.3: ***θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.***

Note 1.4: ***Ψ_{JT}represents the thermal parameterfor the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-5.***