2x30W Stereo / 1x60W Mono Class-D Audio Amplifier With Low Idle Current and AGC

Features

- Single supply voltage
  4.5V ~ 26V for loudspeaker driver
  Built-in LDO output 5V for others
- Supports Multiple Output Configurations
  BTL Mode: 30W/CH into 8Ω at 24 V
  BTL Mode: 30W/CH into 4Ω at 18 V
  PBTL Mode: 60W/CH into 4Ω at 24 V
  PBTL Mode: 45W/CH into 4Ω at 18 V
  PBTL Mode: 60W/CH into 2Ω at 18 V
- Loudspeaker performance
  BTL Mode: 30W/CH into 8Ω <1% THD+N@24V
  BTL Mode: 30W/CH into 4Ω <1% THD+N@18V
- >90% efficient Class-D operation eliminates need for heat sink
- Energy Saving Class-D Operation
  Low Idle Current <23mA
- Multiple Switching Frequencies
  AM Avoidance
  Master/Slave Synchronization
  300KHz to 1.2MHz Switching Frequency
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable Automatic Gain Control or adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Thermal fold-back control
- Over temperature protection with auto recovery

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

Description

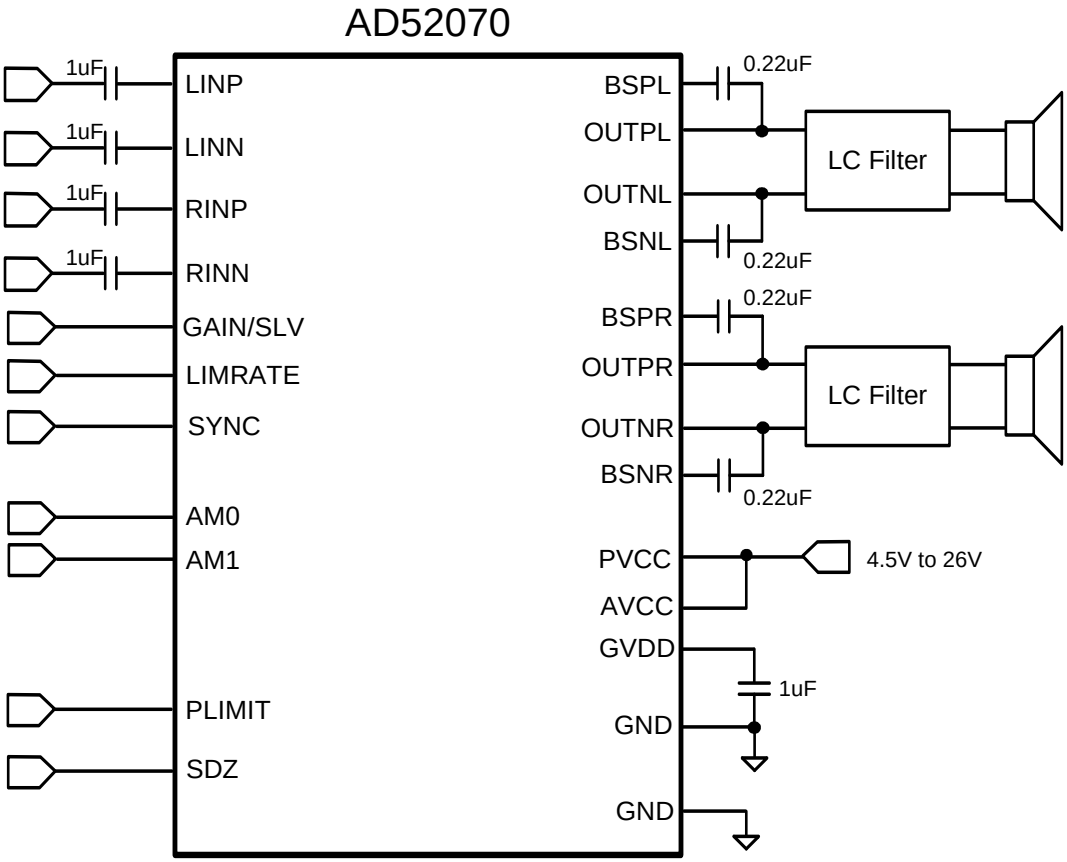
The AD52070 is a high efficiency stereo class-D audio amplifier with adjustable power limit function. It can deliver 30W/CH output power into 4Ω or 8Ω loudspeaker within 1% THD+N at 24V supply voltage. AD52070 also provides parallel BTL (Mono) application, and it can deliver 60W into 4Ω loudspeaker at 24V supply voltage.

The AD52070 has low idle current mode for battery-powered audio system and helps to extend the battery life. The advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences. In order to achieve multi-channels application, which the clock slave mode design with, making it possible to synchronize multiple devices.

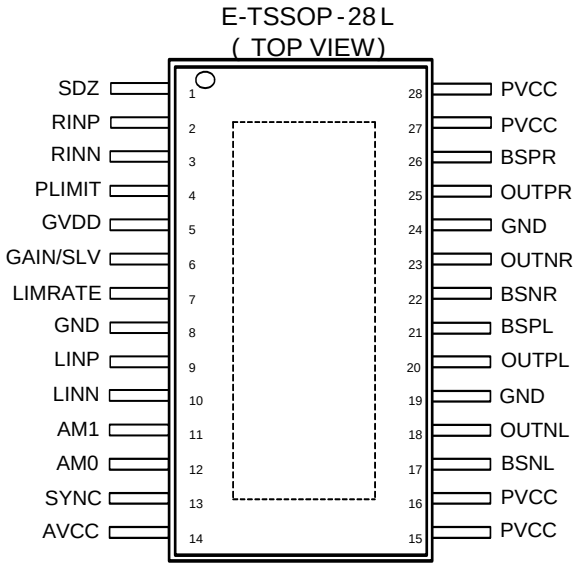
The Automatic Gain Control (AGC) is enabled to prevent output signal from distortion when the input signal exceeds a threshold level. The AGC allows adjustment of maximum output voltage without signal clipping for enhanced speaker protection and audio quality. The power-limit control can provide further limit output power level of amplifier. The adjustable power limit function allows user to set a voltage to limit the amount of current through the speaker. All these functions are performed automatically.

Output DC detection prevents speaker damage from long-time current stress. AD52070 output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

NAME	E-TSSOP -28L	TYP	DESCRIPTION
SDZ	1	DI	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC. Chip is with internal pull low, 250kohm@normal state, <250ohm@ fault state.
RINP	2	AI	Positive audio input for right channel. Connect to GND for MONO mode.
RINN	3	AI	Negative audio input for right channel. Connect to GND for MONO mode.
PLIMIT	4	AI	Voltage level for AGC or power limiter. Connect a resistor divider from GVDD to GND to set AGC or power limit level. Give $V_{PLIMIT} \leqq 2.1V$ to set AGC or power limit level. Connect to GND to disable AGC or power limit function, and chip will into mute function when connect to GVDD ($\geqq$ 2.4V).
GVDD	5	P	5V regulated output, with a 1uF X7R (or X5R) ceramic decoupling capacitor is necessary. Not to be used as a supply or connected to any components other than the PLIMIT and GAIN/SLV resistor dividers.
GAIN/SLV	6	AI	Selects gain depending on pin voltage divider.
LIMRATE	7	AI	Decay speed for clip free for AGC or power limiter. Connect a resistor divider from GVDD to GND to set decay speed. Connect directly to GND to enable power limit function.
GND	8	P	Power ground. Connect to the thermal pad.
LINP	9	AI	Positive audio input for left channel. Connect to GND for PBTL mode.
LINN	10	AI	Negative audio input for left channel. Connect to GND for PBTL mode.
AM1	11	DI	AM avoidance frequency selection 1. Chip is with internal pull low, 250kohm.

AM0	12	DI	AM avoidance frequency selection 0. Chip is with internal pull low, 250kohm.
SYNC	13	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal. Chip is at output mode @Master mode; Input mode (HiZ) @Slave mode.
AVCC	14	P	Analog supply.
PVCC	15,16	P	High-voltage power supply.
BSNL	17	BST	Bootstrap I/O for left channel, negative high side FET.
OUTNL	18	O	Class-D H-bridge negative output for left channel.
GND	19	P	Power ground. Connect to the thermal pad.
OUTPL	20	O	Class-D H-bridge positive output for left channel.
BSPL	21	BST	Bootstrap I/O for left channel, positive high side FET.
BSNR	22	BST	Bootstrap I/O for right channel, negative high side FET.
OUTNR	23	O	Class-D H-bridge negative output for right channel.
GND	24	P	Power ground. Connect to the thermal pad.
OUTPR	25	O	Class-D H-bridge positive output for right channel.
BSPR	26	BST	Bootstrap I/O for right channel, positive high side FET.
PVCC	27,28	P	High-voltage power supply.
Thermal Pad		P	Must be soldered to PCB's ground plane.

AI = Analog input; AO = Analog output; AI/O = Analog Bi-directional (input and output); DI = Digital Input; DO = Digital Output; DI/O = Digital Bi-directional (input and output); P = Power or Ground; BST = Boot Strap

Ordering Information

Product ID	Package	Packing	Comments
AD52070-QG28NRR	E-TSSOP 28L	2500 Units / Reel 1 Reels / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L	AD52070	28	27.1	1.33	Yes (Note 1)

Note 1.1: ***The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.***

Note 1.2: ***θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.***

Note 1.3: ***θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.***

Note 1.4: ***Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-5.***