2x40W Stereo / 1x80W Mono Class-D Audio Amplifier With Power Limit

Features

- Single supply voltage
  4.5V ~ 26V for loudspeaker driver
  Built-in LDO output 5V for others
- Supports Multiple Output Configurations
  BTL Mode: 30W/CH into 8Ω at 24 V
  BTL Mode: 40W/CH into 4Ω at 19 V
  PBTL Mode: 60W/CH into 4Ω at 24 V
  PBTL Mode: 80W/CH into 2Ω at 20 V
- Loudspeaker performance
  BTL Mode: 30W/CH into 8Ω <1% THD+N@24V
  BTL Mode: 40W/CH into 4Ω <1% THD+N@19V
- >90% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Over temperature protection with auto recovery
- E-TSSOP 28L Epad-Up thermally enhanced package

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

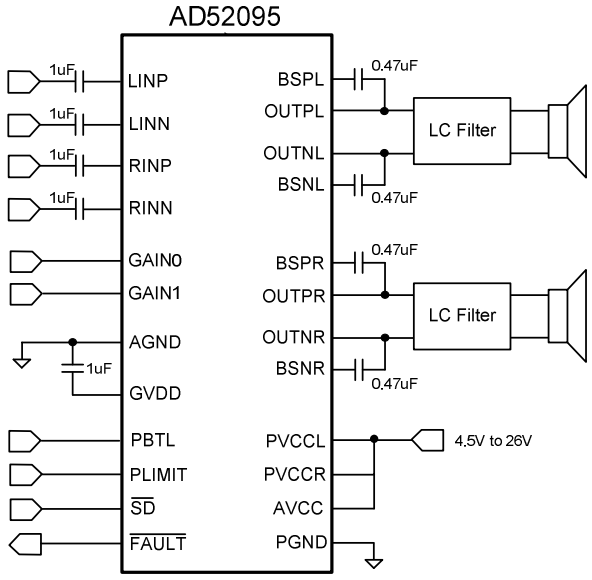
Description

The AD52095 is a high efficiency stereo class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~26V supply voltage and analog circuit operates at 5V supply voltage. It can deliver 40W/CH output power into 4Ω or 8Ω loudspeaker within 1% THD+N at 24V supply voltage.

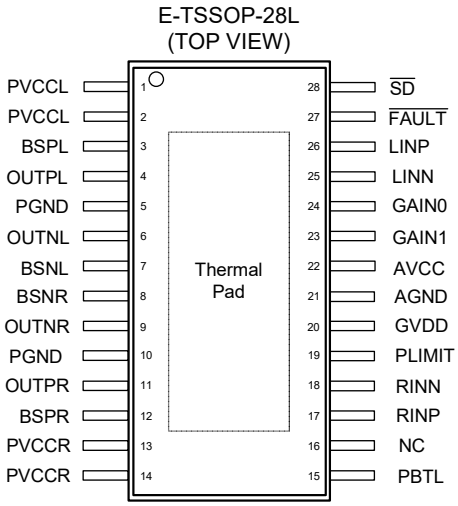
AD52095 provides parallel BTL (Mono) application, and it can deliver 80W into 2Ω loudspeaker at 24V supply voltage. The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. AD52095 output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

NAME	E-TSSOP -28L	TYP	DESCRIPTION
PVCCL	1,2	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPL	3	I	Bootstrap I/O for left channel, positive high side FET.
OUTPL	4	O	Class-D H-bridge positive output for left channel.
PGND	5	P	Power ground for the H-bridges.
OUTNL	6	O	Class-D H-bridge negative output for left channel.
BSNL	7	I	Bootstrap I/O for left channel, negative high side FET.
BSNR	8	I	Bootstrap I/O for right channel, negative high side FET.
OUTNR	9	O	Class-D H-bridge negative output for right channel.
PGND	10	P	Power ground for the H-bridges.
OUTPR	11	O	Class-D H-bridge positive output for right channel.
BSPR	12	I	Bootstrap I/O for right channel, positive high side FET.
PVCCR	13,14	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
PBTL	15	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
NC	16	NA	NC pin.
RINP	17	I	Positive audio input for right channel, biased at 1/10 of PVCC supply voltage.
RINN	18	I	Negative audio input for right channel, biased at 1/10 of PVCC supply voltage.
PLIMIT	19	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
GVDD	20	O	5V regulated output, also used as supply for PLIMIT function.

AGND	21	P	Analog signal ground.
AVCC	22	P	Analog supply.
GAIN1	23	I	Gain select most significant bit, voltage compliance to AVCC.
GAIN0	24	I	Gain select least significant bit, voltage compliance to AVCC.
LINN	25	I	Negative audio input for left channel, biased at 1/10 of PVCC supply voltage.
LINP	26	I	Positive audio input for left channel, biased at 1/10 of PVCC supply voltage.
$\overline{\text{FAULT}}$	27	O	Open drain output used to display short circuit or dc detect fault, voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{\text{FAULT}}$ pin to $\overline{\text{SD}}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
$\overline{\text{SD}}$	28	I	Shutdown signal for IC (low = disabled, high = operational), voltage compliance to AVCC.
Thermal Pad		P	Must be good connected to heat-sink for power dissipation requirement.

Ordering Information

Product ID	Package	Packing	Comments
AD52095-QG28NRR	E-TSSOP 28L (Epad-Up)	2500 Units / Reel 1 Reels / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L (Epad-Up)	AD52095	10	1.2	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-5.