2x31W Stereo / 1x62W Mono Digital Audio Amplifier With 40 bands EQ and DRC Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment and TDM data format
- PSNR & DR(A-weighting)
  Loudspeaker: 107dB (PSNR), 108dB (DR)@24V
- Multiple sampling frequencies (Fs)
  8kHz, 16kHz, 32kHz/44.1kHz/48kHz and 88.2kHz/96kHz
- System clock = 32x, 48x, 64x, 96x, 128x, 192x, 256x Fs
  BCLK system:
  32x~256x Fs for 8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2kHz / 96kHz
- Supply voltage
  3.3V/1.8V for digital circuit
  4.5V~26V for loudspeaker driver
- Supports 2.0CH/Mono configuration
- Loudspeaker output power@12V for stereo
  7W x 2CH into 8Ω <1% THD+N
  10W x 2CH into 4Ω <1% THD+N
- Loudspeaker output power@18V for stereo
  15W x 2CH into 8Ω <1% THD+N
- Loudspeaker output power@24V for stereo
  31W x 2CH into 8Ω <1% THD+N
- Sound processing including：
  40 bands parametric EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Three Band plus post Dynamic range control
  Auto Gain Limiter
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  DC-blocking high-pass filter
  Pre-scale/post-scale
  I^2S output with user programmed gain (+24dB~mute)
- I^2S/TDM output with selectable Audio DSP point
- Anti-pop design
- Level meter and power meter
- Short circuit and over-temperature protection
- Over voltage protection
- Supports Dynamic Temperature Control (DTC)
- Supports I^2C control without clock
- I^2C control interface with 4 selectable device address
- LV Under-voltage shutdown and HV Under-voltage detection
- Auto clock detection
- Power saving mode

Applications

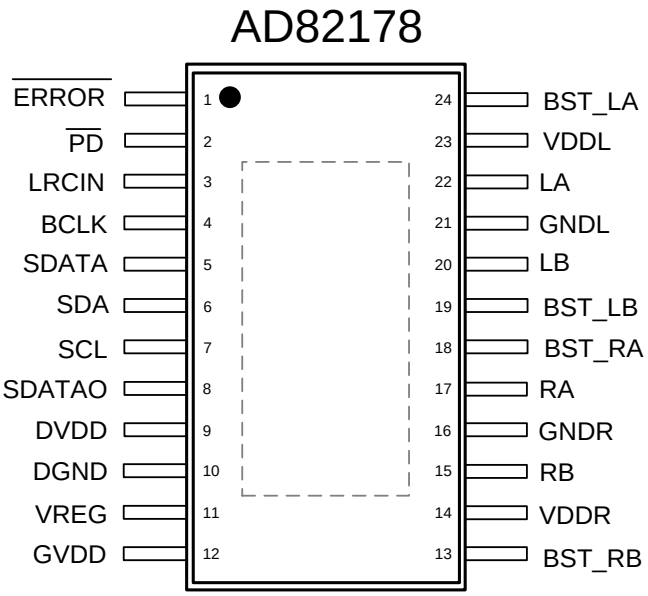
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD82178 is a digital audio amplifier capable of driving 25W (31W peak) each to a pair of 8Ω load speaker (BTL) and 50W (62W peak) to a 4Ω load speaker (PBTL) operating at 24V supply without external heat-sink or fan requirement with play music.

AD82178 provides advanced audio processing functions, such as volume control, 40 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC) and Auto Gain Limiter (AGL). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82178 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82178 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82178 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



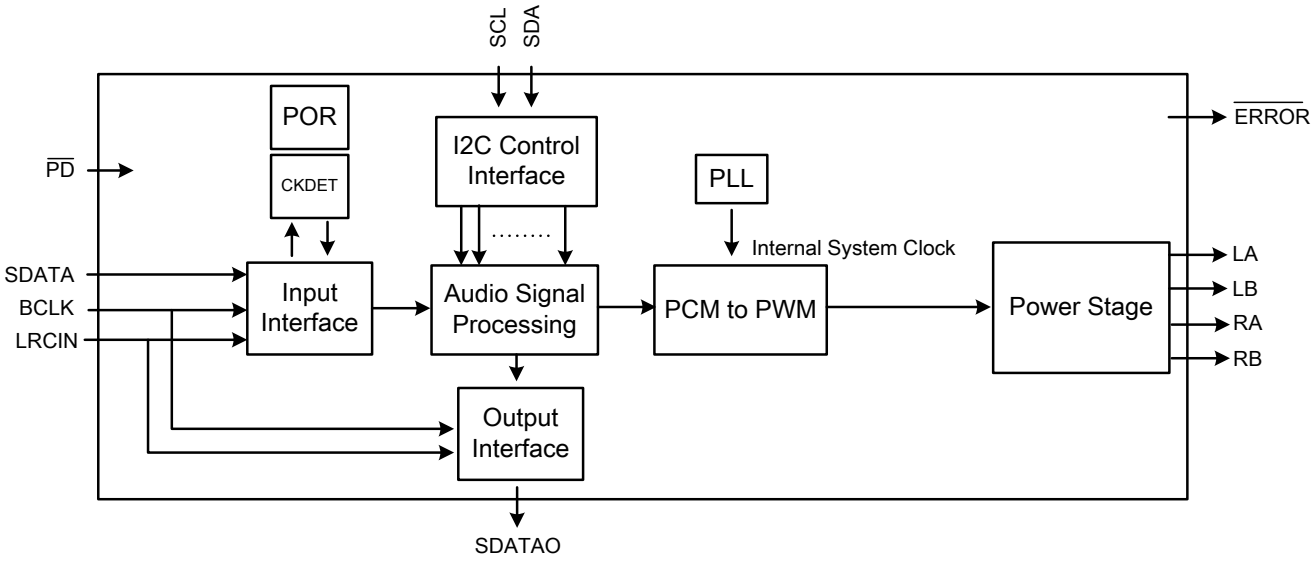
E-TSSOP-24L

Pin Description (E-TSSOP 24L)

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{ERROR}}$	I/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. It will determine the slave address of AD82178 and define in the device addressing part.
2	$\overline{\text{PD}}$	I	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
3	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
4	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
5	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	O	Serial audio data output.	Schmitt trigger TTL input buffer
9	DVDD	P	Digital Power.	
10	DGND	P	Digital Ground.	

11	VREG	O	1.5V Regulator voltage output.	
12	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_RB	P	Bootstrap supply for right channel output B.	
14	VDDR	P	Right channel supply.	
15	RB	O	Right channel output B.	
16	GNDR	P	Right channel ground.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap supply for right channel output A.	
19	BST_LB	P	Bootstrap supply for left channel output B.	
20	LB	O	Left channel output B.	
21	GNDL	P	Left channel ground.	
22	LA	O	Left channel output A.	
23	VDDL	P	Left channel supply.	
24	BST_LA	P	Bootstrap supply for left channel output A.	

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82178-QG24NRR	E-TSSOP 24L	2.5K Units / Reel 1 Reel / Small box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-TSSOP 24L	AD82178	26.8	1.83	27.1	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

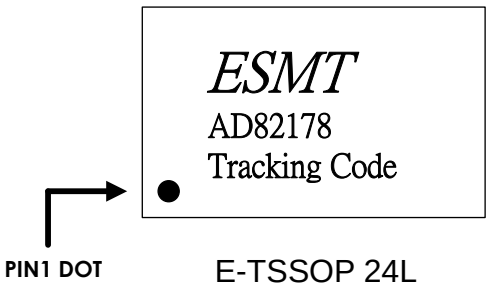
Marking Information

AD82178

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code



E-TSSOP 24L

Absolute Maximum Ratings (AMR)

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
	Output Pin (LA, LB, RA and RB) to GND		32	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	^oC
T_J	Junction Operating Temperature	-40	150	^oC
ESD	Human Body Model		±2K	V
	Charged Device Model		±750	V

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit for 3.3V	3.15~3.45	V
	Supply for Digital Circuit for 1.8V	1.65~1.95	
VDDL/R	Supply for Driver Stage	4.5~26	V
T_J	Junction Operating Temperature	-40~125	^oC
T_A	Ambient Operating Temperature	-40~85	^oC

General Electrical Characteristics

Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V		20	40	uA
I_Q(HV)	Quiescent current for PVDD (Advance quaternary mode)	PVDD=24V		6.5		mA
I_Q(LV)	Quiescent current for DVDD (Un-mute)	DVDD=3.3V,		16	25	mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			160		°C
	Temperature Hysteresis for Recovery from Shutdown			35		°C
UV_{DVDDH}	DVDD Under Voltage Release (LV_UVSEL B[1]=0, set at 1.35V)			1.5		V
UV_{DVDDL}	DVDD Under Voltage Active (LV_UVSEL B[1]=0, set at 1.35V)			1.35		V
OV_H	VDDL/R Over Voltage Active			29.5		V
OV_L	VDDL/R Under Voltage Release			28.5		V
$R_{DS(on)}$ (Note 3)	Static Drain-to-Source On-state Resistor, NMOS	PVDD=24V, Id=500mA		150		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=24V		8		A
		PVDD=12V		7.5		A
	Mono Over-Current Protection (Note 2)	PVDD=24V		12		A
		PVDD=12V		11.5		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
		DVDD=1.8V	1.26			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
		DVDD=1.8V			0.54	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
		DVDD=1.8V	1.44			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
		DVDD=1.8V			0.4	V
C_I	Input Capacitance			6.4		pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Note 3: This doesn't include bond-wire or pin resistance.