2x40W Stereo / 1x 80W Mono / 2x20W+1x40W 2.1CH Digital Audio Amplifier with 20 Bands EQ

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting)
  Stereo: 98dB (PSNR), 107dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- BCLK system supports
- Supply voltage
  3.3V for digital circuit
  7V~26V for loudspeaker driver
- Loudspeaker output power for stereo at 24V
  40W x 2CH into 4Ω @0.22% THD+N
- Loudspeaker output power for mono at 24V
  80W x 1CH into 4Ω @10% THD+N
- Loudspeaker output power for 2.1CH at 24V
  20W x 2CH into 8Ω @0.25% THD+N
  40W x 1CH into 4Ω @0.22% THD+N
- Sound processing including：
  20 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step),
  Dynamic range control
  Dual Band Dynamic range control
  Power Clipping
  3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  Bass management crossover filter
  DC-blocking high-pass filter
- Power on reset
- Anti-pop design
- I^2C control interface (without MCLK) with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Short-circuit and over-temperature protection
- Power saving mode
- Tunable surround sounds
- Support initial EEPROM setting

Applications

- CD and DVD
- TV audio
- Car audio
- Boom-box
- MP3 docking systems
- Powered speaker
- Wireless audio

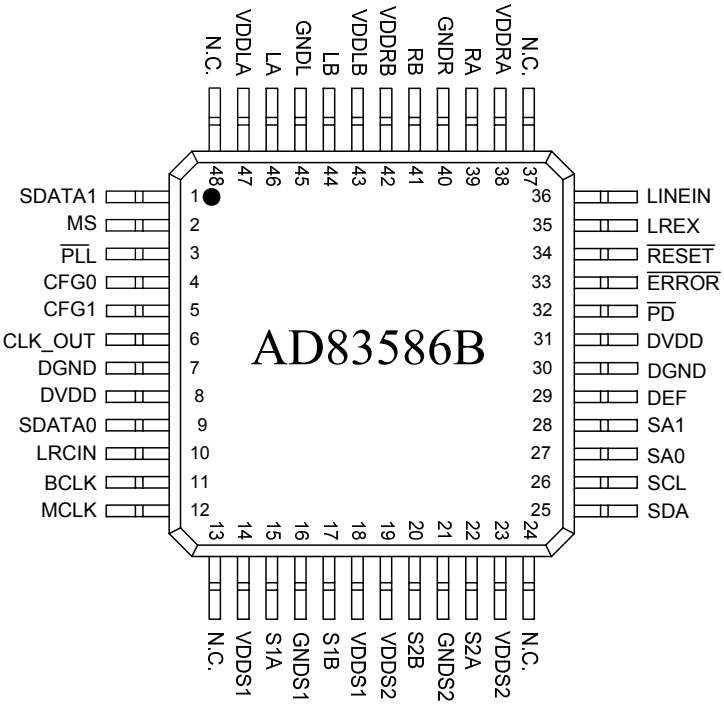
Description

AD83586B is a digital audio amplifier capable of driving a pair of 8Ω, 20W plus a single 4Ω, 40W, or a pair of 4Ω, 40W or a single 4Ω, 60W speaker operating at 24V supply with proper cooling method.

AD83586B can provide advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD83586B from damage due to accidental erroneous operating condition. AD83586B is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD83586B is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

The output stage is flexibly configurable for 2.1 channel, stereo or mono applications. Furthermore, it is possible to use three pieces of AD83586B to realize 5.1 channels for home theater applications.

Pin Assignment



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	SDATA1	I	Serial audio data input 1	Schmitt trigger TTL input buffer
2	MS	I	EEPROM selection	Schmitt trigger TTL input buffer
3	$\overline{\text{PLL}}$	I	PLL enable, low active	Schmitt trigger TTL input buffer
4	CFG0	I	2.1 Ch/Stereo/Mono configuration pin	Schmitt trigger TTL input buffer
5	CFG1	I	2.1 Ch/Stereo/Mono configuration pin	Schmitt trigger TTL input buffer
6	CLK_OUT	I/O	PLL ratio setting pin during power up, this pin is monitored on the rising edge of reset. PMF register will be default set at 1 or 4 times PLL ratio by setting this pin at High or Low. High: PMF [3:0] = [0000], 1 time of PLL ratio to avoid system MCLK over flow. Low: PMF [3:0] = [0100], 4 times of PLL ratio. This pin could be clock output pin also during normal operating if EN_CLK_OUT register bit is enabled.	TTL output buffer, internal pull Low with an 80Kohm resistor.
7	DGND	P	Digital Ground	
8	DVDD	P	Digital Power	

9	SDATA0	I	Serial audio data input 0	Schmitt trigger TTL input buffer
10	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
11	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
12	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
13	N.C.			
14	VDDS1	P	Subwoofer1 channel supply	
15	S1A	O	Subwoofer1 channel output A	
16	GNDS1	P	Subwoofer1 channel ground	
17	S1B	O	Subwoofer1 channel output B	
18	VDDS1	P	Subwoofer1 channel supply	
19	VDDS2	P	Subwoofer2 channel supply	
20	S2B	O	Subwoofer2 channel output B	
21	GNDS2	P	Subwoofer2 channel ground	
22	S2A	O	Subwoofer2 channel output A	
23	VDDS2	P	Subwoofer2 channel supply	
24	N.C.			
25	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
26	SCL	I/O	I^2C serial clock input	Schmitt trigger TTL input buffer
27	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
28	SA1	I	I^2C select address 1	Schmitt trigger TTL input buffer
29	DEF	I	Initial default volume setting (1:Un-Mute ; 0:Mute)	Schmitt trigger TTL input buffer
30	DGND	P	Digital Ground	
31	DVDD	P	Digital Power	
32	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
33	$\overline{ERROR}$	O	Error status, low active	Open-drain output
34	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
35	LREX	I	Left/Right channel exchange (0:Unchanged ; 1:Exchanged)	Schmitt trigger TTL input buffer
36	LINEIN	I	Select input data (0:SDATA0 ; 1:SDATA1)	Schmitt trigger TTL input buffer
37	N.C.			
38	VDDRA	P	Right channel supply A	
39	RA	O	Right channel output A	
40	GNDR	P	Right channel ground	
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	

43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	GNDL	P	Left channel ground	
46	LA	O	Left channel output A	
47	VDDLA	P	Left channel supply A	
48	N.C.			

Marking Information

AD83586B

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code

Line 4 : Date Code