
2x60W Stereo / 1x120W Mono / 2x30W+1x60W 2.1CH Digital Audio Amplifier with 36 bands EQ and DRC Functions

Features

- 16/18/20/24-bits input with I²S, Left-alignment and Right-alignment and TDM data format
- PSNR & DR(A-weighting)
Loudspeaker: 105dB (PSNR), 106dB (DR)@24V
- Multiple sampling frequencies (Fs)
8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2k / 96kHz
- System clock = 32x,48x, 64x,96x, 128x,192x, 256x, 384x, 512 Fs
MCLK system:
32x~512x Fs for 8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2kHz / 96kHz
BCLK system:
32x~256x Fs for 8kHz, 16kHz and 32kHz / 44.1kHz / 48kHz and 88.2kHz / 96kHz
- Supply voltage
3.3V for digital circuit
1.65~3.6V for DVDDIO
4.5V~26V for loudspeaker driver
- Speaker peak output power at 24V
60W x 2CH into 4Ω @0.4% THD+N
120W x 1CH into 2Ω @0.9% THD+N
- Speaker peak output power for 2.1CH at 24V
30W x 2CH into 8Ω @0.5% THD+N
60W x 1CH into 4Ω @0.5% THD+N
- Sound processing including :
36 bands parametric speaker EQ
Volume control (+24dB~-103dB, 0.125dB/step)
DRC, AGC and Power Clipping
Programmed 3D surround sound
Channel mixing
Compensate filter
DC-blocking high-pass filter
Pre-scale/post-scale
I²S output with user programmed gain
Crossover filter for twitter and woofer
- Anti-pop design
- Power meter
- I²S output with selectable Audio DSP point
- Short circuit and over-temperature protection
- Supports I²C control without clock

- I²C control with 4 selectable device address
- Support hardware and software reset
- Internal PLL
- LV & HV Under-voltage detection
- Over voltage protection
- Auto clock detection
- Power saving mode
- DTC

Applications

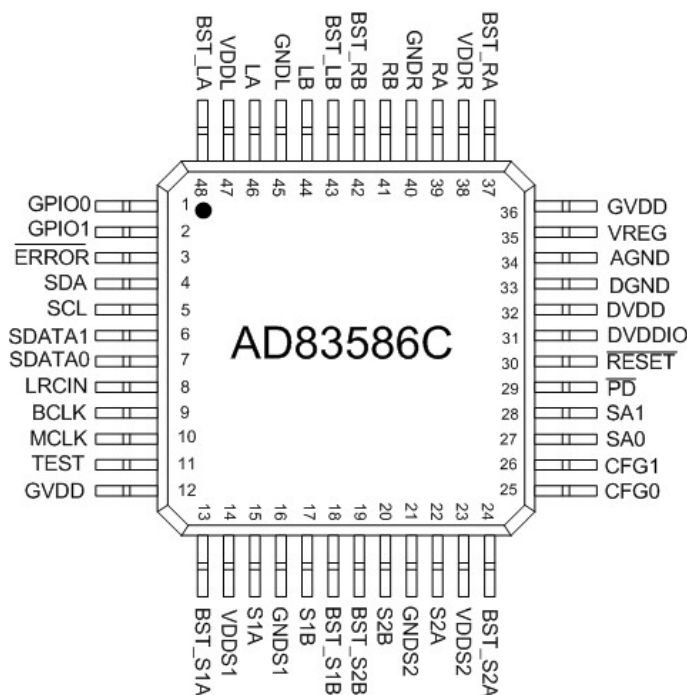
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD83586C is a digital audio amplifier capable of driving a pair of 8Ω, 25W (30W peak) plus a single 4Ω, 50W (60W peak), or a pair of 4Ω, 50W (60W peak) or a single 2Ω, 100W (120W peak) speaker operating at 24V supply with proper cooling method.

AD83586C can provide advanced audio processing capabilities, such as volume control, 36 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I²C control interface. Robust protection circuits are provided to protect AD83586C from damage due to accidental erroneous operating condition. AD83586C is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD83586C is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

The output stage is flexibly configurable for 2.1 channel, stereo or mono applications. Furthermore, it is possible to use two pieces of AD83586C to realize 5.1 channels for home theater applications.

Pin Assignment**Pin Description (E-LQFP 48L)**

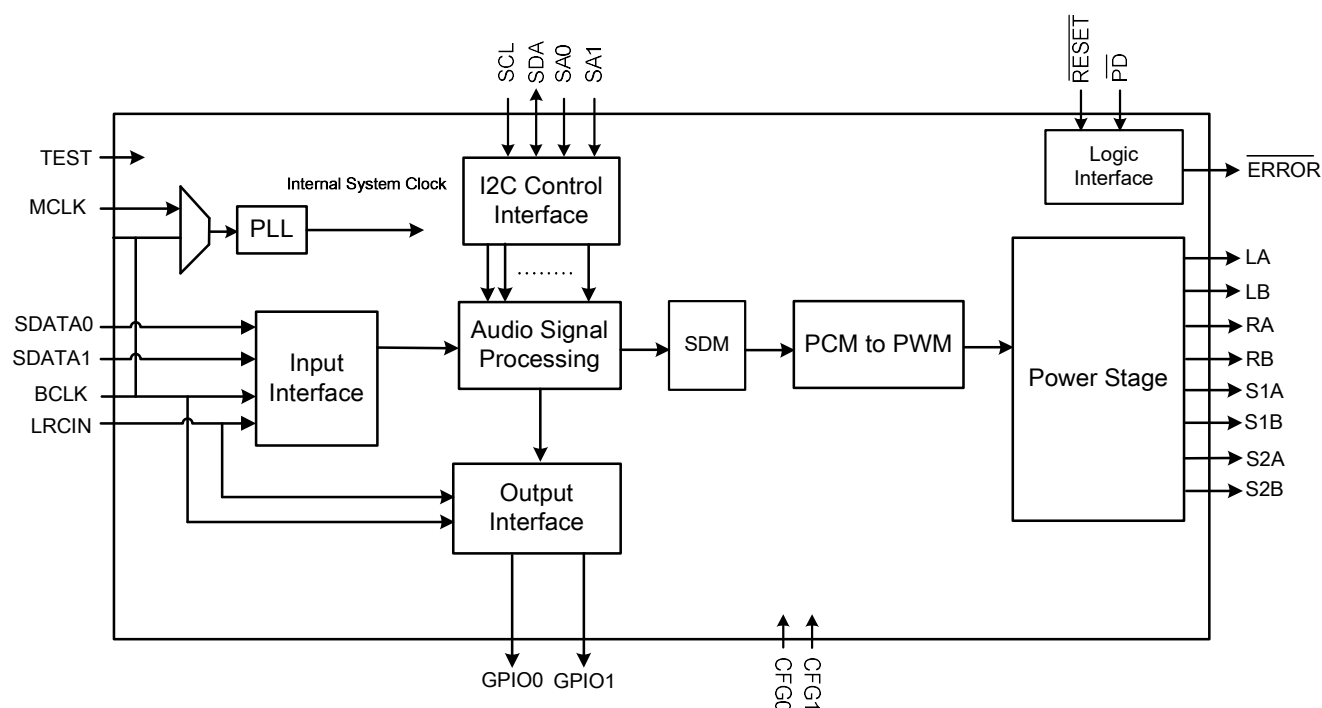
PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	GPIO0	DI/O	General purpose input0/output0.	
2	GPIO1	DI/O	General purpose input1/output1.	
3	ERROR	DO	ERROR pin is an error status report (low active), It sets by register of A_SEL_FAULT at address 0x0C B[7] to enable it.	Schmitt trigger TTL input buffer.
4	SDA	DI/O	I ² C bi-directional serial data.	Schmitt trigger TTL input buffer.
5	SCL	DI	I ² C serial clock input.	Schmitt trigger TTL input buffer.
6	SDATA1	DI	Serial audio data1 input.	Schmitt trigger TTL input buffer.
7	SDATA0	DI	Serial audio data0 input.	Schmitt trigger TTL input buffer.
8	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
9	BCLK	DI	Bit clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
10	MCLK	DI	Master clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.

11	TEST	DI	This pin must connect to GND.	
12	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_S1A	P	Bootstrap supply for sub channel1 output A.	
14	VDDS1	P	Sub1 channel supply.	
15	S1A	O	Sub1 channel output A.	
16	GNDS1	P	Sub1 channel ground.	
17	S1B	O	Sub1 channel output B.	
18	BST_S1B	P	Bootstrap supply for sub channel1 output B.	
19	BST_S2B	P	Bootstrap supply for sub channel2 output B.	
20	S2B	O	Sub2 channel output B.	
21	GNDS2	P	Sub2 channel ground.	
22	S2A	O	Sub2 channel output A.	
23	VDDS2	P	Sub2 channel supply.	
24	BST_S2B	P	Bootstrap supply for sub channel2 output A.	
25	CFG0	DI	Mono/Stereo/2.1 configuration pin.	
26	CFG1	DI	Mono/Stereo/2.1 configuration pin.	
27	SA0	DI	I ² C select address 0.	
28	SA1	DI	I ² C select address 1.	
29	$\overline{\text{PD}}$	DI	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
30	$\overline{\text{RESET}}$	DI	Reset, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
31	DVDDIO	P	Digital Power for I/O circuit.	
32	DVDD	P	Digital Power.	
33	DGND	P	Digital Ground.	
34	AGND.	P	Analog Ground.	
35	VREG	P	1.8V Regulator voltage output.	
36	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
37	BST_RA	P	Bootstrap supply for right channel output A.	
38	VDDR	P	Right channel supply.	
39	RA	O	Right channel output A.	
40	GNDR	P	Right channel ground.	
41	RB	O	Right channel output B.	

42	BST_RB	P	Bootstrap supply for right channel output B.	
43	BST_LB	P	Bootstrap supply for left channel output B.	
44	LB	O	Left channel output B.	
45	GNDL	P	Left channel ground.	
46	LA	O	Left channel output A.	
47	VDDL	P	Left channel supply.	
48	BST_LA	P	Bootstrap supply for left channel output A.	

Note: AI=Analog input; AO=Analog output; AI/O = Analog Bi-directional (input and output); DI=Digital Input; DO=Digital Output; DI/O = Digital Bi-directional (input and output); P=Power or Ground; O: PWM output

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD83586C-LG48NRY	E-LQFP 48L (7mmx7mm)	250 Units / Tray 2.5K Units / Box (10 Trays)	Green
AD83586C-LG48NRR		2K Units / Reel 1 Reel / Small box	Green