2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 36 Bands EQ Functions

Features

- 16/18/20/24-bits input with I²S, Left-alignment and Right-alignment data format
- Multiple sampling frequencies (Fs)
  8kHz and 32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system:
  256x~4096x Fs for 8kHz
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
  BCLK system:
  64xFs for 32kHz / 44.1kHz / 48kHz
  64xFs for 64kHz / 88.2kHz / 96kHz
  64xFs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  1.8V or 3.3V for digital I/O
  3.3V for analog circuit and headphone driver
  4.5V~26V for loudspeaker driver
- Speaker or headphone out selection
- Line-driver maximum output swing into 10kΩ - 2Vrms at 3.3V supply voltage
- Headphone output power
  25mW x 2ch into 32Ω @ 0.1% THD+N
- Speaker output power
  20W x 2ch into 8Ω @ <1% THD+N@24V
- Sound processing including：
  36 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
  Pre-scale/post-scale
  Virtual Bass/exciter
  Dynamic bass
- Anti-pop design
- Level meter and power meter
- I²S output with selectable audio DSP point
- Supports I²C control without clock
- I²C control interface with selectable device address
- Internal PLL
- Protection
  - OCP
  - OVP
  - UVP
  - OTP
- Closed-loop structure with good PSRR
- Supports Filter-less operating
- Superior EMC performance

Applications

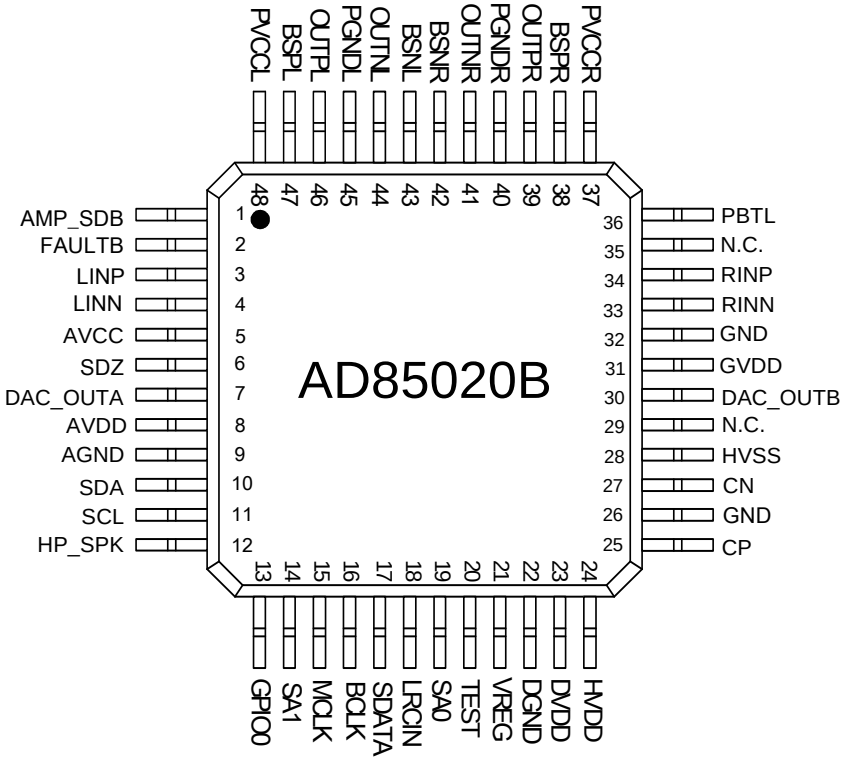
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio
- AI speaker

Description

AD85020B is a digital audio amplifier capable of driving. a pair of 8Ω,20W or a single 4Ω,40W speaker output. In headphone output mode, it can delivered 25mW into 32Ω load for head phone output.

AD85020B provides advanced audio processing functions, such as volume control, 36 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I²C control interface. Robust protection circuits are provided to protect AD85020B from damage due to accidental erroneous operating condition. The full digital circuit design of AD85020B is tolerant of noise and PVT (Process, Voltage, and Temperature) variation. AD85020B is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	AMP_SDB	I	Shut down for AMP, low active.	With pull low resistor (250Kohm).
2	FAULTB	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to AMP_SDB pin. Otherwise, dc detect faults must be reset by cycling AVCC.	
3	LINP	I	Positive audio input for left channel.	
4	LINN	I	Negative audio input for left channel.	
5	AVCC	P	Analog supply.	
6	SDZ	O	Shut down control for AMP.	
7	DAC_OUTA	O	Analog output from DAC A channel.	
8	AVDD	P	Power supply for analog circuit, 3.3V	

9	AGND	P	Ground for analog circuit.	
10	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
11	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
12	HP_SPK	I	Head phone and speaker switch.	Schmitt trigger TTL input buffer, with pull low resistor internally.
13	GPIO0	I/O	General purpose digital input and output. port 0.	Schmitt trigger TTL input buffer, with pull low resistor internally.
14	SA1	I	I^2C select address 1.	Schmitt trigger TTL input buffer, with pull low resistor internally.
15	MCLK	I	Master clock input.	Schmitt trigger TTL input buffer.
16	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer.
17	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
18	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer.
19	SA0	I	I^2C select address 0.	Schmitt trigger TTL input buffer, with pull low resistor internally.
20	TEST	I	This pin must connect to GND.	With pull low resistor internally.
21	VREG	O	1.8V Regulator voltage output.	
22	DGND	P	Digital Ground.	
23	DVDD	P	Digital I/O power, 1.8V or 3.3V.	
24	HVDD	P	Supply voltage for headphone driver, 3.3V.	
25	CP	O	Charge-pump flying capacitor positive terminal.	
26	GND	P	Power ground.	
27	CN	O	Charge-pump flying capacitor negative terminal.	
28	HVSS	P	Negative supply voltage for headphone driver.	
29	N.C.		Not connected.	
30	DAC_OUTB	O	Analog output from DAC B channel.	
31	GVDD	O	5V regulated output, also used as supply for PLIMIT function.	
32	GND	P	Power ground.	
33	RINN	I	Negative audio input for right channel.	
34	RINP	I	Positive audio input for right channel.	
35	N.C.	I	Not connected.	
36	PBTL	I	Parallel BTL mode switch, high for parallel	With pull low resistor internally.

			BTL output. Voltage compliance to AVCC.	
37	PVCCR	P	High-voltage power supply for right-channel. Channel power supply inputs are connected in chip internally.	
38	BSPR	O	Bootstrap I/O for right channel, positive high side FET	
39	OUTPR	O	Class-D H-bridge positive output for right channel	
40	PGNDR	P	Power ground for the H-bridges.	
41	OUTNR	O	Class-D H-bridge negative output for right channel.	
42	BSNR	O	Bootstrap I/O for right channel, negative high side FET.	
43	BSNL	O	Bootstrap I/O for left channel, negative high side FET.	
44	OUTNL	O	Class-D H-bridge negative output for left channel.	
45	PGNDL	P	Power ground for the H-bridges.	
46	OUTPL	O	Class-D H-bridge positive output for left channel.	
47	BSPL	O	Bootstrap I/O for left channel, positive high side FET.	
48	PVCCL	P	High-voltage power supply for left-channel. Left channel and Right channel power supply inputs are connected in chip internally.	