2X20W Stereo / 1x40W Mono Digital Audio Amplifier with 2Vrms Line Driver

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  10W x 2ch into 8Ω @ 0.16% THD+N
  15W x 2ch into 8Ω @ 0.18% THD+N
  20W x 2ch into 8Ω @ 0.24% THD+N
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Dynamic temperature control

Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

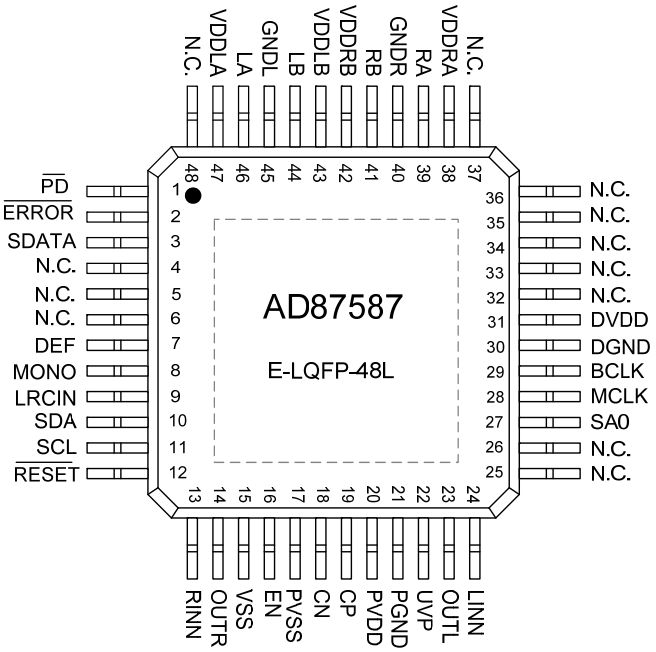
The AD87587 is an integrated audio system solution, embedding digital audio process, power stage amplifier, and a stereo 2Vrms line driver.

Using I^2C digital control interface, the user can control AD87587's input format selection, mute and volume control functions. AD87587 has many built-in protection circuits to safeguard AD87587 from connection errors.

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD87587-LG48NAY	E-LQFP-48L (7x7 mm)	2.5K Units / Small Box (250 Units / Tray, 10 Trays / Small Box	Green

Pin Assignment (Top View)



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
2	$\overline{ERROR}$	O	Error status, low active	Open-drain output
3	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
4	N.C.			
5	N.C.			
6	N.C.			
7	DEF	I	Default volume setting	Schmitt trigger TTL input buffer
8	MONO	I	MONO mode enable, high active	Schmitt trigger TTL input buffer
9	LRCIR	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
10	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
11	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
12	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
13	RINN	I	Right input for line driver	
14	ROUT	O	Right output for line driver	
15	SGND	P	Ground for line driver	
16	EN	I	Enable for line driver	
17	PVSS	P	Supply voltage for line driver	
18	CN	I/O	Charge pump flying capacitor negative connection for line driver	

19	CP	I/O	Charge pump flying capacitor positive connection for line driver	
20	PVDD	P	Supply voltage for line driver	
21	PGND	P	Ground for line driver	
22	UVP	I	Under voltage protection for line driver	
23	LOUT	O	Left output for Line driver	
24	LINN	I	Left input for Line driver	
25	N.C.			
26	N.C.			
27	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
28	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
29	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
30	DGND	P	Digital Ground (3.3V)	
31	DVDD	P	Digital Power (3.3V)	
32	N.C.			
33	N.C.			
34	N.C.			
35	N.C.			
36	N.C.			
37	N.C.			
38	VDDRA	P	Right channel supply A	
39	RA	O	Right channel output A	
40	GNDR	P	Right channel ground	
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	
43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	GNDL	P	Left channel ground	
46	LA	O	Left channel output A	
47	VDDLA	P	Left channel supply A	
48	N.C.			