2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 20 Bands EQ Functions + Capless Line Driver

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 97dB (PSNR), 105dB (DR) @24V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  3.3V for digital circuit
  10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@24V
  10W x 2ch into 8Ω @0.09% THD+N
  15W x 2ch into 8Ω @0.13% THD+N
  20W x 2ch into 8Ω @0.17% THD+N
- Loudspeaker output power for Mono@24V
  20W x 1ch into 8Ω @0.06% THD+N
  30W x 1ch into 8Ω @0.09% THD+N
  40W x 1ch into 8Ω @0.12% THD+N
- Sound processing including：
  20 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step),
  Dynamic range control (DRC)
  Dual band dynamic range control
  Power clipping
  3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  Bass management crossover filter
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Support initial EEPROM setting

Applications

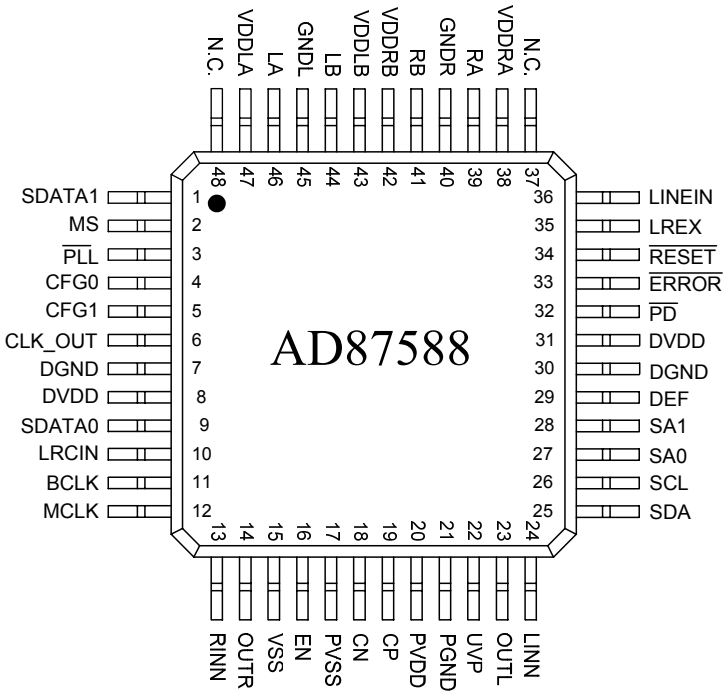
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

The AD87588 is an integrated audio system solution, embedding digital audio process, power stage amplifier, and a stereo 3Vrms line driver. AD87588 is a digital audio amplifier capable of driving a pair of 8Ω, 20W or a single 4Ω, 40W operating at 24V supply. AD87588 is also capable of driving 4Ω, 10W (SE)x2 + 8Ω, 20W (BTL)x1 at 24V supply for 2.1CH application.

AD87588 can provide advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and Dynamic Range Control (DRC). These functions are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD87588 from damage due to accidental erroneous operating condition. AD87588 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD87588 is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

Pin Assignment



Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	SDATA1	I	Serial audio data input 1	Schmitt trigger TTL input buffer
2	MS	I	EEPROM selection	Schmitt trigger TTL input buffer
3	$\overline{PLL}$	I	PLL enable, low active	Schmitt trigger TTL input buffer
4	CFG0	I	Stereo/Mono/2.1CH configuration pin	Schmitt trigger TTL input buffer
5	CFG1	I	Stereo/Mono/2.1CH configuration pin	Schmitt trigger TTL input buffer
6	CLK_OUT	O	Clock output from PLL	TTL output buffer
7	DGND	P	Digital Ground (3.3V)	
8	DVDD	P	Digital Power (3.3V)	
9	SDATA0	I	Serial audio data input 0	Schmitt trigger TTL input buffer
10	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
11	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
12	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
13	RINN	I	Right input for line driver	
14	ROUT	O	Right output for line driver	
15	SGND	P	Ground for line driver	
16	EN	I	Enable for line driver	
17	PVSS	P	Supply voltage for line driver	
18	CN	IO	Charge pump flying capacitor negative connection for line driver	

19	CP	IO	Charge pump flying capacitor positive connection for line driver	
20	PVDD	P	Supply voltage for line driver	
21	PGND	P	Ground for line driver	
22	UVP	I	Under voltage protection for line driver	
23	LOUT	O	Left output for Line driver	
24	LINN	I	Left input for Line driver	
25	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
26	SCL	I/O	I^2C serial clock input	Schmitt trigger TTL input buffer
27	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
28	SA1	I	I^2C select address 1	Schmitt trigger TTL input buffer
29	DEF	I	Initial default volume setting (1:Un-Mute ; 0:Mute)	Schmitt trigger TTL input buffer
30	DGND	P	Digital Ground (3.3V)	
31	DVDD	P	Digital Power (3.3V)	
32	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
33	$\overline{ERROR}$	O	Error status, low active	Open-drain output
34	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
35	LREX	I	Left/Right channel exchange (0:Unchanged ; 1:Exchanged)	Schmitt trigger TTL input buffer
36	LINEIN	I	Select input data (0:SDATA0 ; 1:SDATA1)	Schmitt trigger TTL input buffer
37	N.C.			
38	VDDRA	P	Right channel supply A	
39	RA	O	Right channel output A	
40	GNDR	P	Right channel ground	
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	
43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	GNDL	P	Left channel ground	
46	LA	O	Left channel output A	
47	VDDLA	P	Left channel supply A	
48	N.C.			