24 bits Audio Stereo DAC With DRC and EQ, 2Vrms Line Out

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- Multiple sampling frequencies (Fs)
  8kHz and 32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system:
  256x~4096x Fs for 8kHz
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
  BCLK system:
  64xFs for 32kHz / 44.1kHz / 48kHz
  64xFs for 64kHz / 88.2kHz / 96kHz
  64xFs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  1.8V or 3.3V for digital I/O
  3.3V for analog and digital circuit
- Maximum output voltage
  - 2Vrms at 3.3V supply voltage into 10kΩ load
  - 25mW x 2ch into 32Ω @ 0.1% THD+N
- Sound processing including：
  36 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
  Pre-scale/post-scale
  Virtual Bass/exciter
  Dynamic bass
- Anti-pop design
- Level meter and power meter
- I^2S output with selectable audio DSP point
- Supports I^2C control without clock
- I^2C control interface with 4 selectable device address
- Internal PLL
- LV Under-voltage shutdown
- Protection
  - OTP
  - UVP

Applications

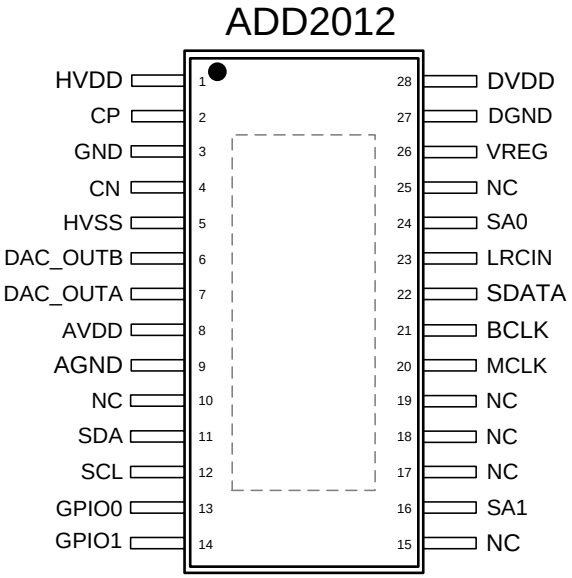
- A/V receivers
- CD and DVD players
- HDTV receivers
- Audio Output Application

Description

ADD2012 is a 2Vrms output audio stereo DAC. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

ADD2012 provides advanced audio processing functions, such as volume control, 36 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect ADD2012 from damage due to accidental erroneous operating condition. The full digital circuit design of ADD2012 is tolerant of noise and PVT (Process, Voltage, and Temperature) variation. ADD2012 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



E-TSSOP-28L

Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	HVDD	P	Supply voltage for line-driver, 3.3V.	
2	CP	O	Charge-pump flying capacitor positive terminal.	
3	GND	P	Power ground.	
4	CN	O	Charge-pump flying capacitor negative terminal.	
5	HVSS	P	Negative supply voltage for line-driver.	
6	DAC_OUTB	O	Analog output from DAC B channel.	
7	DAC_OUTA	O	Analog output from DAC A channel.	
8	AVDD	P	Analog Power.	
9	AGND	P	Analog Ground.	
10	NC		Not connected.	
11	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
12	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
13	GPIO0	I/O	General purpose digital input and output port 0.	Schmitt trigger TTL input buffer, with pull low resistor internally.
14	GPIO1	I/O	General purpose digital input and output port 1.	Schmitt trigger TTL input buffer, with pull low resistor internally.
15	NC		Not connected.	

16	SA1	I	I^2C select address 1.	Schmitt trigger TTL input buffer, with pull low resistor internally.
17	NC		Not connected.	
18	NC		Not connected.	
19	NC		Not connected.	
20	MCLK	I	Master clock input.	Schmitt trigger TTL input buffer.
21	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer.
22	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer.
23	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer.
24	SA0	I	I^2C select address 0.	Schmitt trigger TTL input buffer, with pull low resistor internally.
25	NC		Not connected.	
26	VREG	I	1.8V Regulator voltage output.	
27	DGND	P	Digital Ground.	
28	DVDD	P	Digital I/O power, 1.8V or 3.3V.	