1.5MHz 1A, Synchronous Step-Down Regulator

General Description

EML3383 is a high efficiency step down DC/DC converter. It features an extremely low quiescent current, which is suitable for reducing standby power consumption, especially for portable applications.

The device can accept input voltage from 2.6V to 5.5V and deliver up to 1A output current. High 1.5MHz switching frequency allows the use of small surface mount inductors and capacitors to reduce overall PCB board space. Furthermore, the built-in synchronous switch improves efficiency and eliminates external Schottky diode. EML3383 uses different modulation modes for various loading conditions: (1) Pulse Width Modulation (PWM) for low output voltage ripple and fixed frequency noise, (2) Pulse Frequency Modulation (PSM) for improving light load efficiency.

In addition EML3383 also build in over current and over voltage protection. The adjustable version of this device is available in SOT-23-5L packages.

Features

- Approach 95% efficiency
- Input voltage : 2.6V to 5.5V
- Output current up to 1A
- Reference voltage: 0.6V
- Quiescent current 30 μ A
- Internal switching frequency: 1.5MHz
- No Schottky diode needed
- Low dropout operation: 100% duty cycle
- Shutdown current < 1 μ A
- Excellent line and load transient response
- Over-current protection
- Over-temperature protection

Applications

- Blue-Tooth devices
- Cellular and Smart Phones
- Wireless networking
- Portable applications

Typical Application

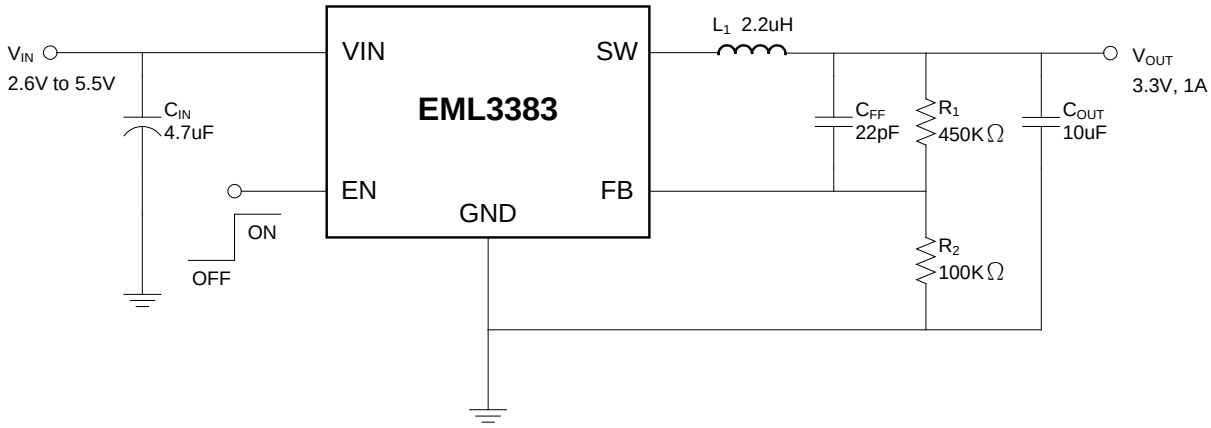
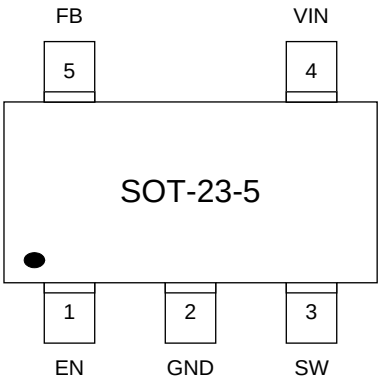


Fig.1 Typical Application

Package Configuration

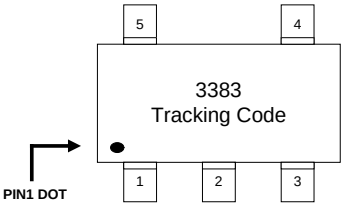


SOT-23-5L

EML3383-00VN05NRR

00	Adjustable
VN05	SOT-23-5L Package
NRR	RoHS & Halogen free package Commercial Grade Temperature Rating: -40 to 85°C Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
SOT-23-5L	Adjustable	EML3383-00VN05NRR		Tape & Reel 3K units

Pin Function Descriptions

Pin Name	SOT-23-5L	Function
EN	**1**	Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shut down the device.
GND	**2**	Ground Pin.
SW	**3**	Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VIN	**4**	Power Input Pin. Must be closely decoupled to GND pin with a 4.7uF or greater ceramic capacitor.
FB	**5**	Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.

Functional Block Diagram

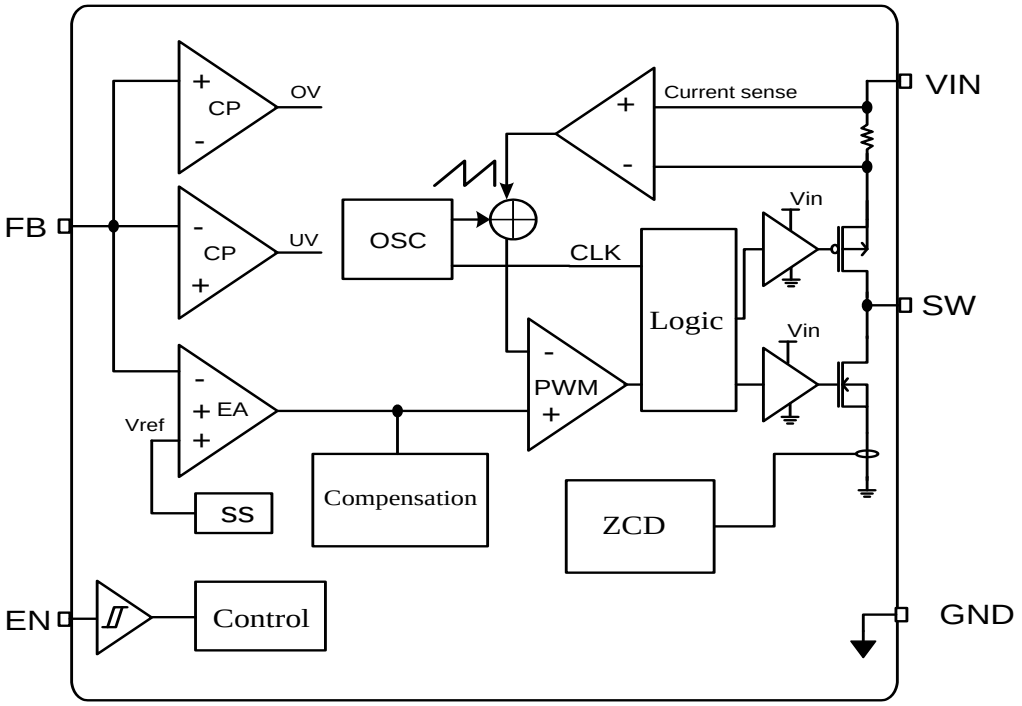


Fig.2 Functional Block Diagram

Absolute Maximum Ratings

■ **Devices are subjected to fail if they stay above absolute maximum ratings.**

Input Voltage ---------- – 0.3V to 6V
EN, FB Voltages ---------- – 0.3V to V_{IN}
SW Voltage ---------- – 0.3V to (V_{IN} + 0.3V)
Lead Temperature (Soldering, 10 sec)---------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Notes 1, 3) ---------- 150°C
Storage Temperature Range ---------- – 65°C to 150°C
ESD Susceptibility HBM ---------- 2KV
CDM ---------- 500V

Thermal data

Package	Thermal resistance	Parameter	Value
SOT-23-5L	θ_{JA} (Note 4)	Junction-ambient	134.5°C/W
	θ_{JC} (Note 5)	Junction-case	81°C/W

Electrical Characteristics

■ **VIN=3.6V, T_A=+25°C, unless otherwise specified.**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.6		5.5	V
V_{FB}	Regulated Feedback Voltage		0.588	0.600	0.612	V
I_{PK}	Peak Inductor Current	V_{FB} = 0.5V	1.5	2.2		A
I_Q	Quiescent Current	V_{FB} = 0.65V		30		uA
I_{SD}	Shutdown Current	$V_{EN=0V}$		0.1	1	uA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V	1.2	1.5	1.8	MHz
R_{ON}	$R_{DS(ON)}$ of PMOS	I_{SW} = 100mA		220		mΩ
R_{ON}	$R_{DS(ON)}$ of NMOS	I_{SW} = –100mA		170		mΩ
V_{UVLO}	VIN UVLO Threshold			2		V
D	Maximum Duty cycle		100			%
V_{EN}	Enable Threshold		1.5			V
V_{EN}	Shutdown Threshold				0.4	V
I_{EN}	EN Leakage Current				±1	uA
IFB	FB input Current			0.1		uA
I_{LSW}	SW Leakage	V_{EN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V			±1	uA
T_{SD}	Thermal Shutdown			160		℃
	Thermal Shutdown Hysteresis			30		℃
T_{SS}	Soft start time			0.8		mS

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * (74.7°C/W)$).

Note 2: Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.

Note 3: This IC has a built-in over-temperature protection to avoid damage from overloaded conditions.

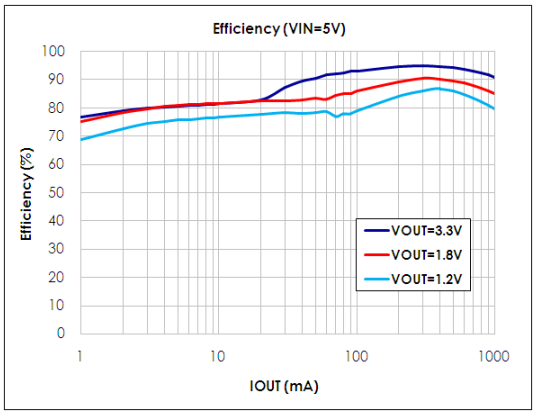
Note 4: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board(2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 5: θ_{JC} represents the heat resistance between the chip and the package top case.

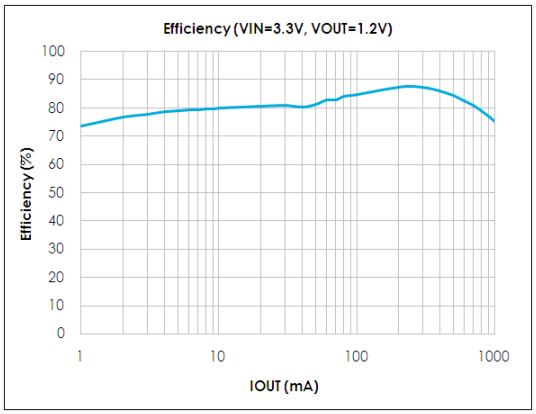
Typical Performance Characteristics

V_{IN}=3.6V, T_A=25℃, unless otherwise specified

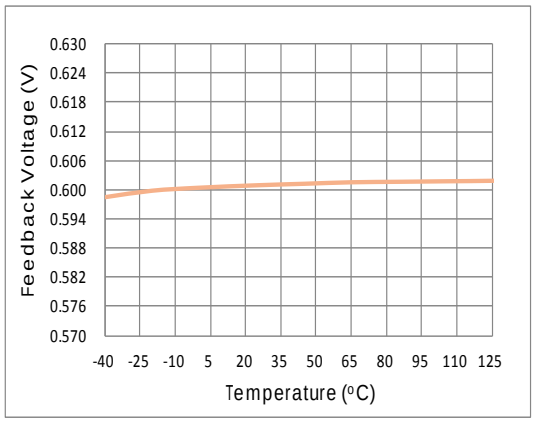
Efficiency vs. Output Current (VIN=5V)



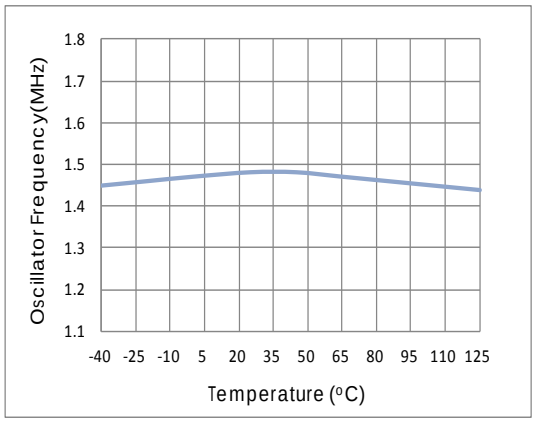
Efficiency vs. Output Current (VIN=3.3V)



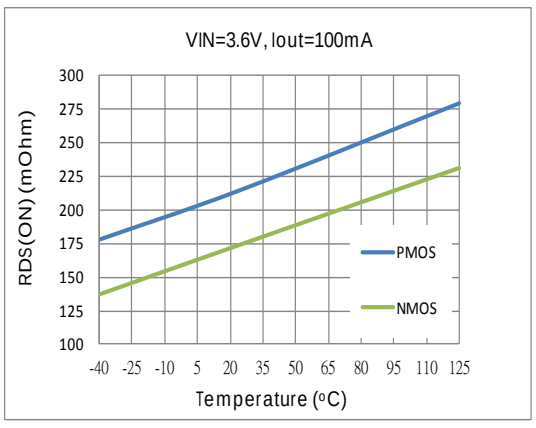
Feedback Voltage vs. Temperature



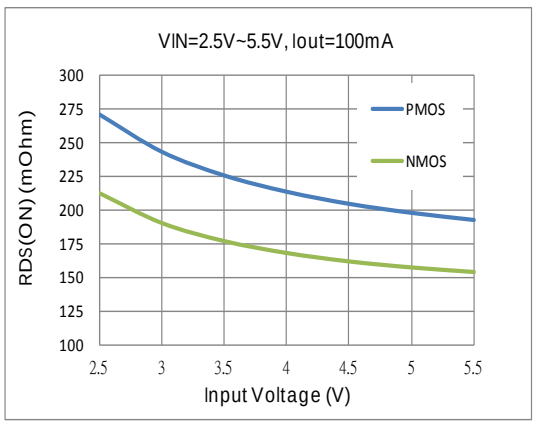
Oscillator Frequency vs. Temperature



$R_{DS(ON)}$ vs. Temperature



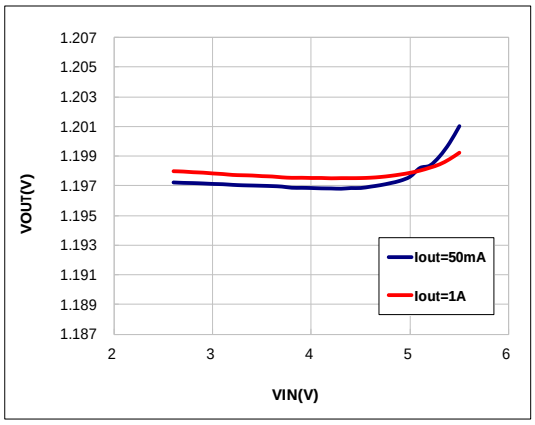
$R_{DS(ON)}$ vs. Input Voltage



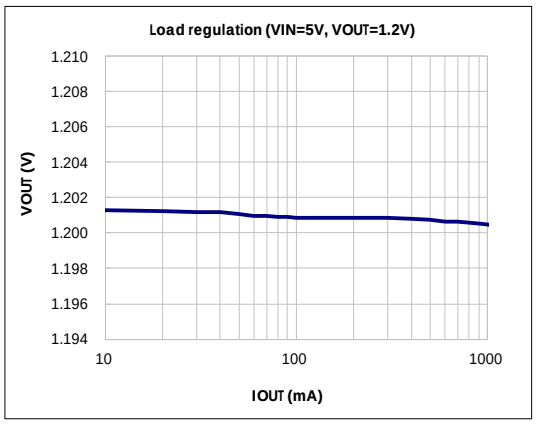
Typical Performance Characteristics (cont.)

V_{IN}=3.6V, T_A=25℃, unless otherwise specified

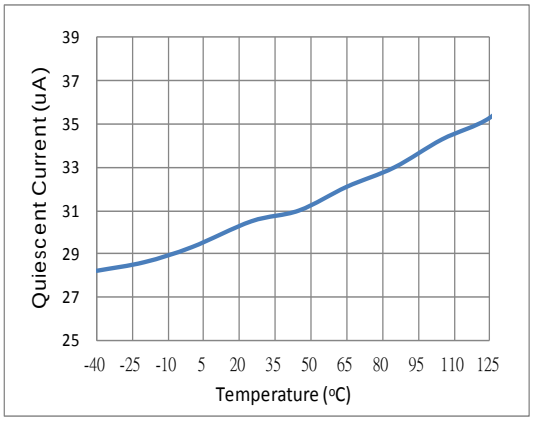
Line Regulation



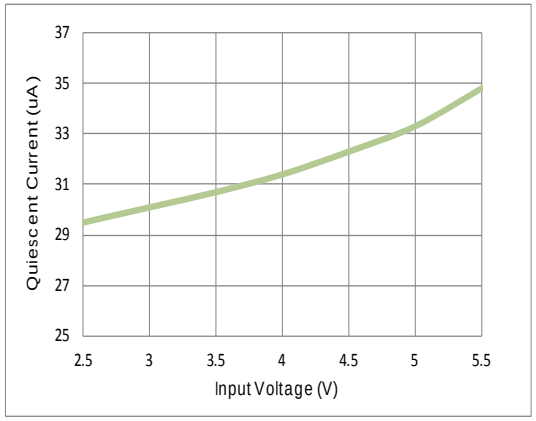
Load Regulation



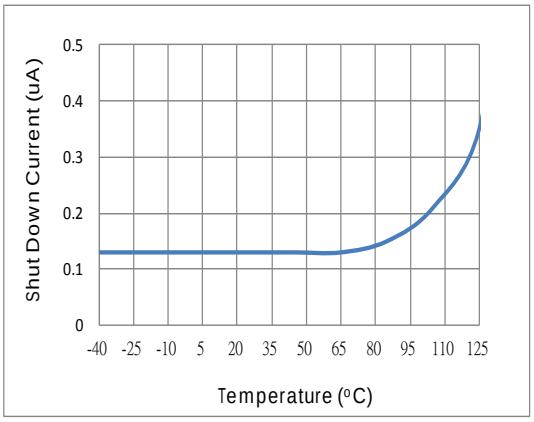
Quiescent Current vs. Temperature



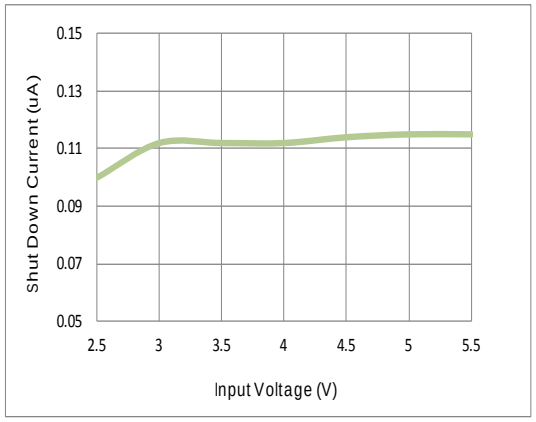
Quiescent Current vs. Input Voltage



Shutdown Current vs. Temperature



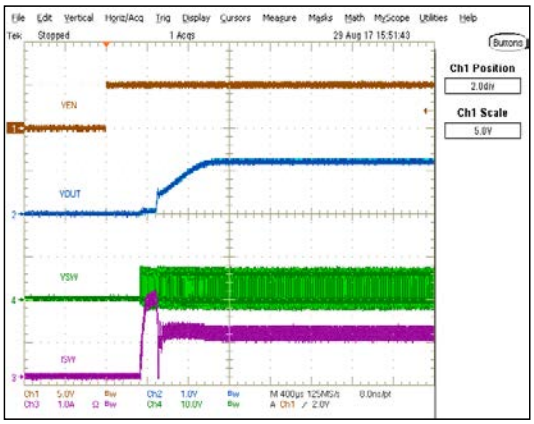
Shutdown Current vs. Input Voltage



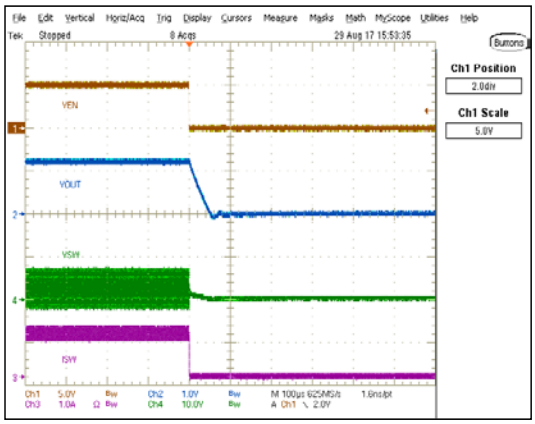
Typical Performance Characteristics (cont.)

V_{IN}=3.6V, T_A=25℃, unless otherwise specified

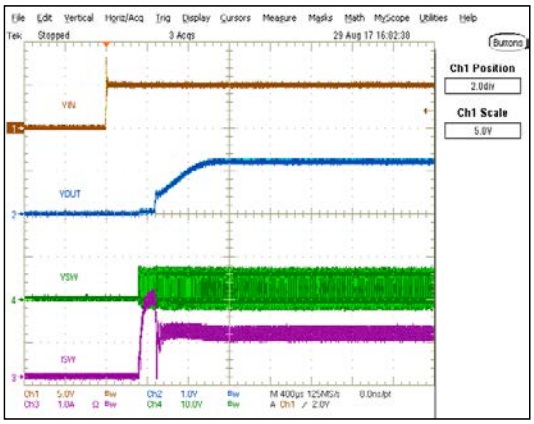
Enable from EN Pin (VIN=5V,I_{OUT}=1A)



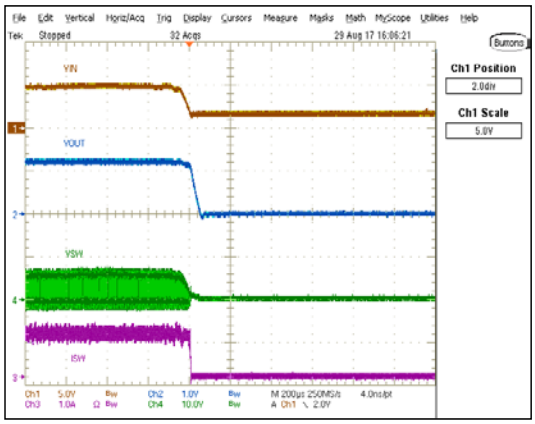
Disable from EN Pin (VIN=5V, I_{OUT}=1A)



Power-ON from VIN Pin (VIN=5V, I_{OUT}=1A)

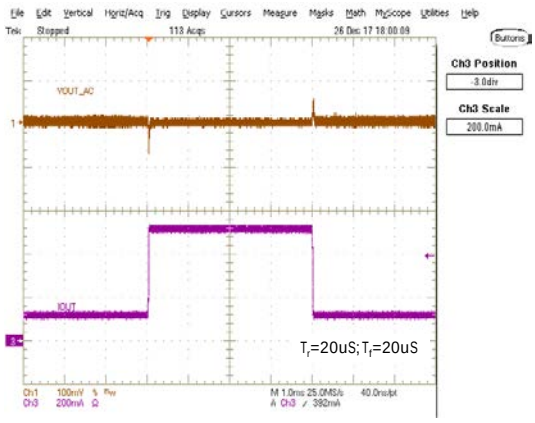


Power-OFF from VIN Pin (VIN=5V, I_{OUT}=1A)



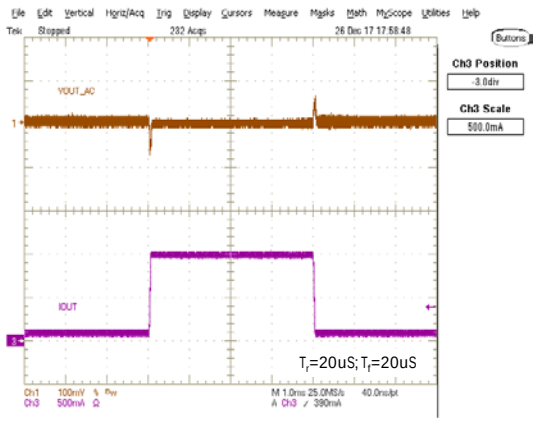
Load Step Response

(V_{OUT}=1.2V, I_{OUT} from 100mA to 500mA



Load Step Response

(V_{OUT}=1.2V, I_{OUT} from 100mA to 1A)



Applications Information

The typical application circuit of adjustable version is shown in Fig.1.

■ Inductor Selection

Inductor ripple current and core saturation current are the two main factors that decide the Inductor value. A low DCR inductor is preferred.

■ C_{IN} and C_{OUT} Selection

A low ESR input capacitor can prevent large voltage transients at V_{IN}. The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{O,MAX} \times \frac{\sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})}}{V_{IN}} \quad \ldots\ldots\ldots (1)$$

ESR is an important parameter to select C_{OUT}, which can be seen in the following output ripple V_{OUT} equation:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \quad \ldots\ldots\ldots\ldots (2)$$

Cheaper and smaller ceramic capacitors with higher capacitance values are now commercially available. These ceramic capacitors have low ripple currents, high voltage ratings and low ESR which make them suitable for switching regulator applications. It is feasible to optimize very low output ripples by Cout since Cout does not affect the internal control loop stability. X5R or X7R types are recommended since they have the best temperature and voltage characteristics of all ceramics capacitors.

■ Output Voltage

In the adjustable version, the output voltage can be determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2} \right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

■ Thermal Considerations

Although the thermal shutdown circuit is designed in EML3383 to protect the device from thermal damage, the total power dissipation that EML3383 can sustain depends on the thermal capability of the package. The formula to ensure the safe operation is shown in note 1 on page 5.

To avoid the EML3383 from exceeding the maximum junction temperature, the user should perform some thermal analysis during PCB design.

■ Guidelines for PCB Layout

To ensure proper operation of the EML3383, please note the following PCB layout guidelines:

1. The GND, SW and the VIN trace should be kept short, direct and wide.
2. FB pin must be connected directly to the feedback resistors. Resistive divider R_1/R_2 must be connected parallel to the output capacitor C_{OUT}.
3. The Input capacitor C_{IN} must be connected to the pin VIN as close as possible.
4. Keep SW node away from the sensitive VFB node since this node has high frequency and voltage swing.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Applications

■ **Typical schematic for PCB layout**

1. Schematic

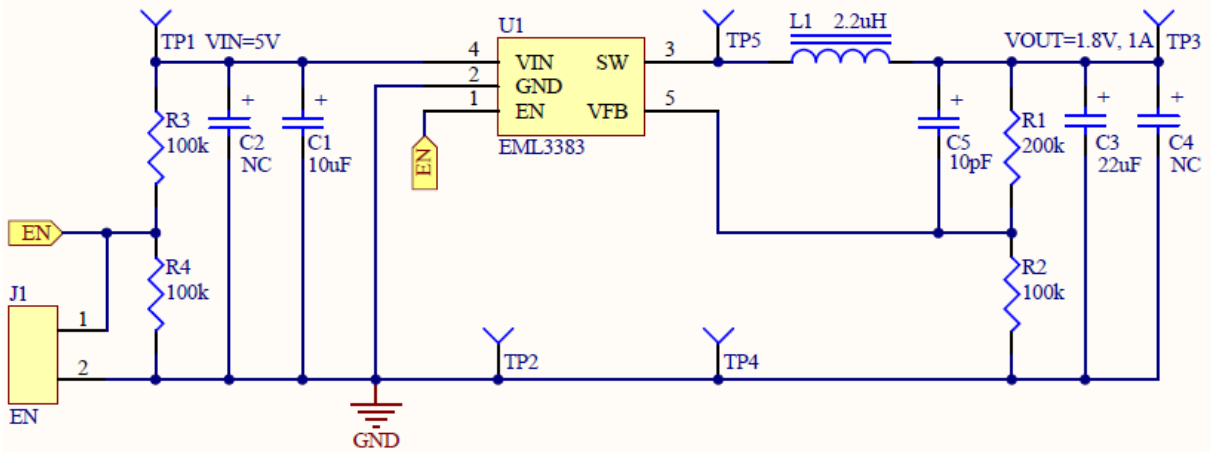
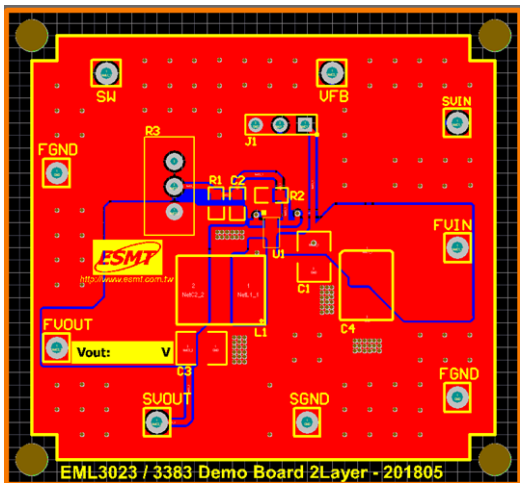
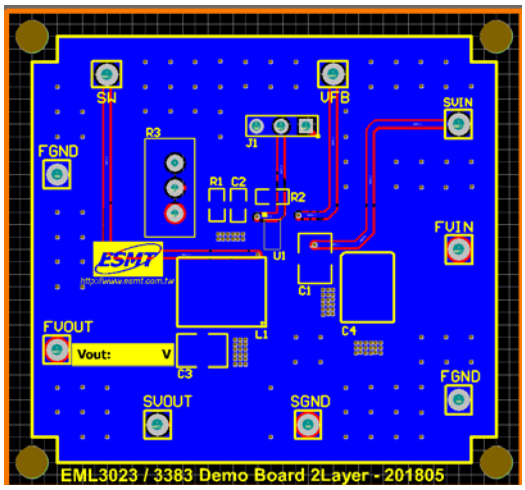
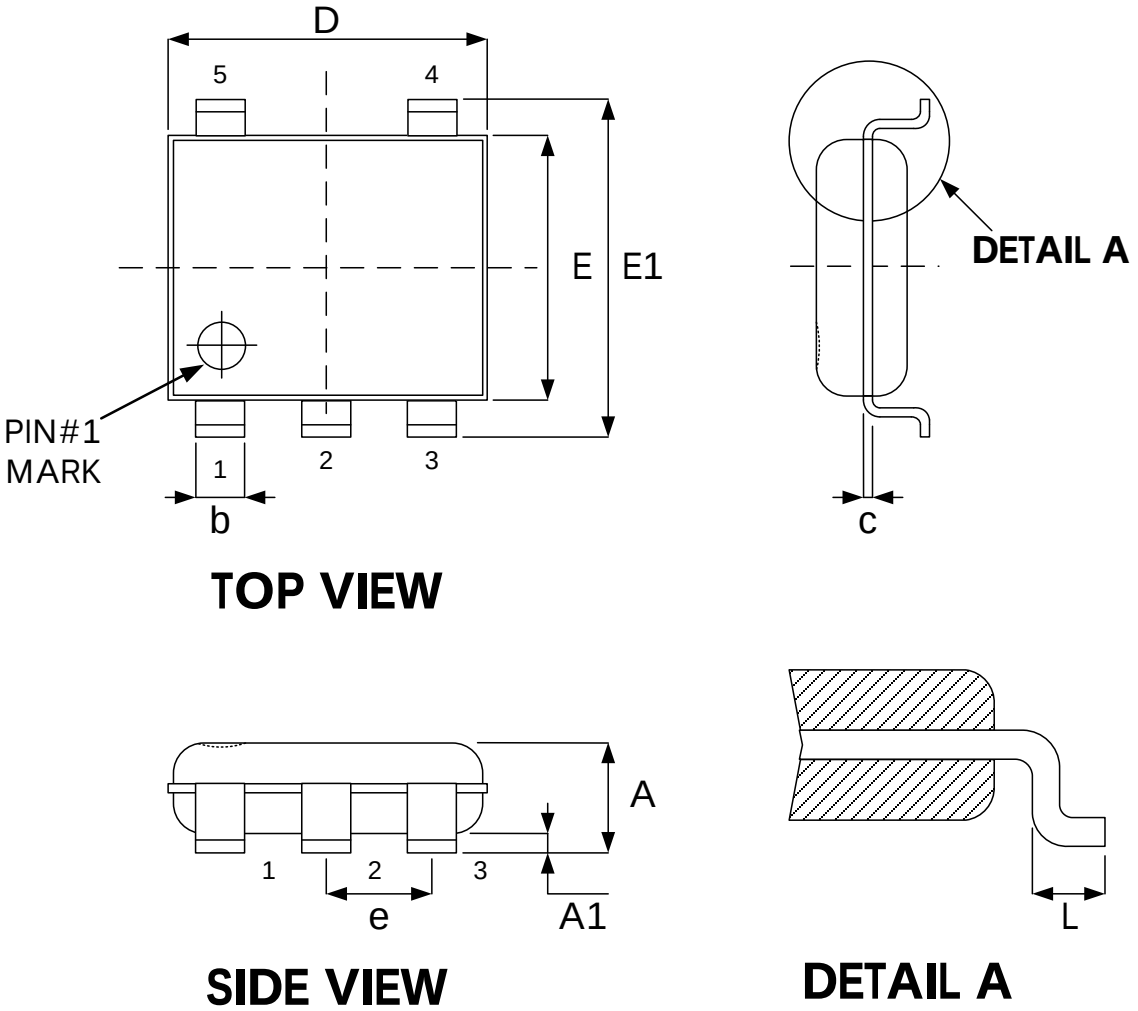


Fig.3 EML3383 PCB Schematic

2. PCB Layout

Top Layer (Fig.4)	Bottom Layer (Fig.5)
	

Package Outline Drawing
SOT-23-5L



Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Revision History

Revision	Date	Description
0.1	2018.5.31	Initial version.
0.2	2018.07.09	Update efficiency plot.
0.3	2019.01.02	1. Modified Pin name : GND description. 2. Modified VIN ceramic capacitor form 10uF to 4.7uF.
1.0	2019.05.03	1.Modified version to V1.0 and delete preliminary

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