High Input Voltage, Low Quiescent Current, Low-Dropout Linear Regulator

General Description

The EMP8042 is a high voltage, low quiescent current, low dropout regulator with 150mA output driving capacity. The EMP8042, which operates over an input range **up** to 20V, is stable with any capacitors, whose capacitance is larger than 1μF, and suitable for powering battery-management ICs because of the virtue of its low quiescent current consumption and low dropout voltage. Below the maximum power dissipation (please refer to Note. 5), It guarantees delivery of 100mA output current, and supports preset output voltages ranging from 1.3V to 6.0V with 0.1V increment.

EMP8042 also includes bandgap voltage reference, constant current limiting and thermal overload protection. It's available in both of SOT-23-5,SOT-89-3 and **SOT-23-3** miniature packages.

Applications

- Logic Supply for High Voltage Batteries
- Keep-Alive Supply
- 3-4 Cell Li-ion Batteries Powered systems

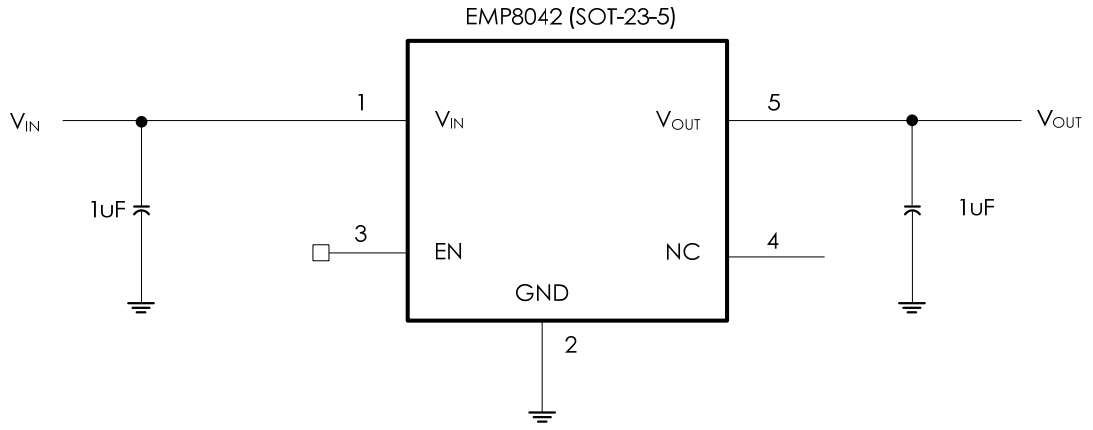
Features

- 150mA output current driving capacity
- 780mV typical dropout at Io=150mA
- 13μA typical quiescent current
- 1μA typical shutdown mode
- **Up** to 20V input range
- Stable with small ceramic output capacitors (1μF)
- Over temperature and over current protection

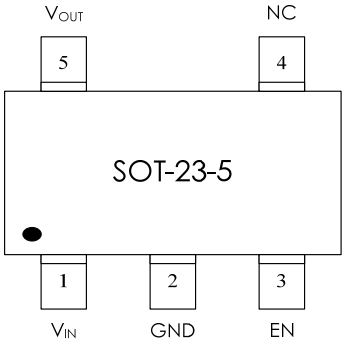
Ordering Information

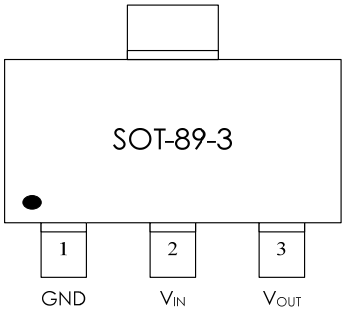
Part Number	Remark
EMP8042	**±2.5% output voltage tolerance**
EMP8042B	**±1.0% output voltage tolerance**

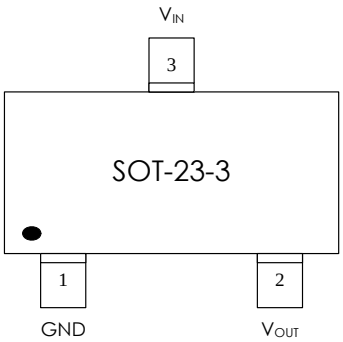
Typical Application



Connection Diagrams







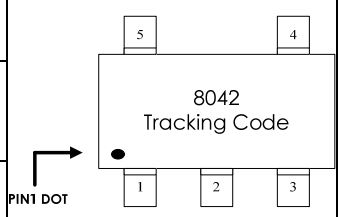
Order information

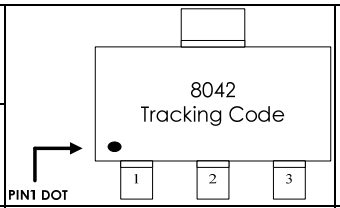
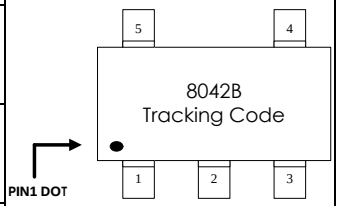
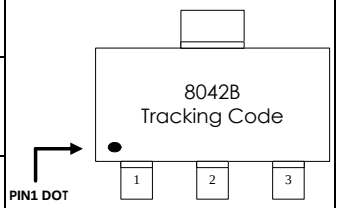
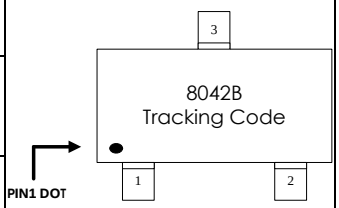
EMP8042-XXVF05NRR**/ EMP8042B-XXVF05NRR**
XX Output voltage
VF05 SOT-23-5 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

EMP8042-XXVG03NRR**/ EMP8042B-XXVG03NRR**
XX Output voltage
VG03 SOT-89-3 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

EMP8042B-XXVN03NRR
XX Output voltage
VN03 SOT-23-3 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

Order, Marking and Packing Information

Package	Vout	Product ID.	Marking	Packing
SOT-23-5	3.3V	EMP8042-33VF05NRR		Tape & Reel 3Kpcs
	5.0V	EMP8042-50VF05NRR		
	ADJ	EMP8042-00VF05NRR		

SOT-89-3	3.3V	EMP8042-33VG03NRR		Tape & Reel 1Kpcs
	5.0V	EMP8042-50VG03NRR		
SOT-23-5	**3.0V**	**EMP8042B-30VF05NRR**		**Tape & Reel** **3Kpcs**
	3.3V	**EMP8042B-33VF05NRR**		
	5.0V	**EMP8042B-50VF05NRR**		
	ADJ	**EMP8042B-00VF05NRR**		
SOT-89-3	**3.0V**	**EMP8042B-30VG03NRR**		**Tape & Reel** **1Kpcs**
	3.3V	**EMP8042B-33VG03NRR**		
	5.0V	**EMP8042B-50VG03NRR**		
SOT-23-3	**3.0V**	**EMP8042B-30VN03NRR**		**Tape & Reel** **3Kpcs**
	3.3V	**EMP8042B-33VN03NRR**		
	5.0V	**EMP8042B-50VN03NRR**		

Pin Functions

Name	SOT-23-5	SOT-89-3	SOT23-3	Function
V_{IN}	1	2	3	**Supply Voltage Input** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	1	1	**Ground Pin**
EN	3	N/A	N/A	**Shutdown Input** The EN pin is pulled "High" internally. Set the regulator into the disable mode by pulling the EN pin low.
ADJ	4	N/A	N/A	**Adjust:** Feedback input. Connect to resistive voltage-divider network. $V_{OUT} = \left(1 + \frac{R1}{R2}\right) \cdot Vref$
NC (Fixed output)				**No connection**
V_{OUT}	5	3	2	**Output Voltage**

Functional Block Diagram

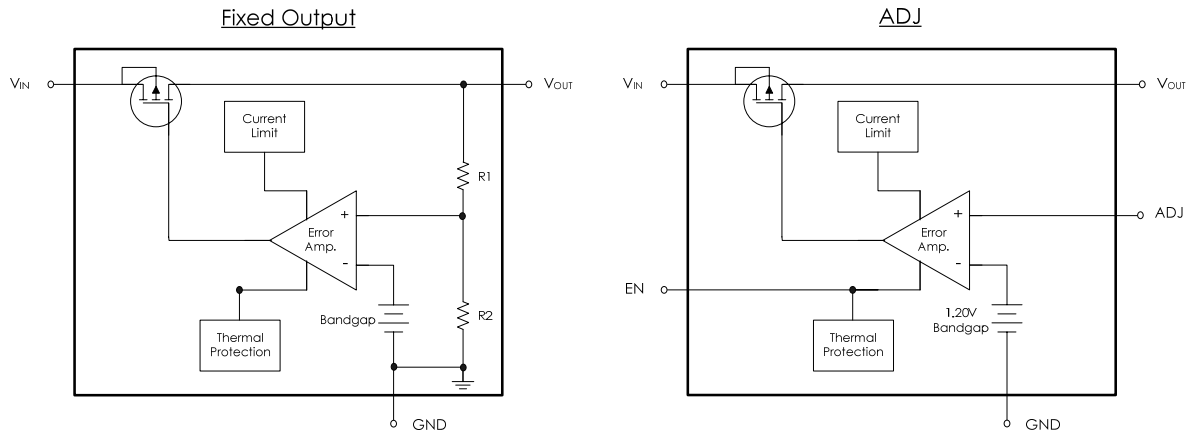


FIG.1. Functional Block Diagram of EMP8042

Absolute Maximum Ratings (Notes 1, 2)

V_{IN} ,EN	-0.3V to 22V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 5)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Model	2KV
Junction Temperature (T_J)	160°C		

Operating Ratings (Note 1, 2)

Supply Voltage (EMP8042)	3.0V to 20V	Thermal Resistance (θ_{JA} , Note 3))	152°C/W (SOT-23-5)
Supply Voltage (EMP8042B)	**2.7V to 20V**		101°C/W (SOT-89-3)
Operating Temperature Range	-40°C to 85°C	Thermal Resistance (θ_{JC} , Note 4))	81°C/W (SOT-23-5)
			54°C/W (SOT-89-3)

Electrical Characteristics

T_A = 25°C, V_{OUT}(NOM)=5V; unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V, C_{IN} = C_{OUT} =1μF.

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
ΔV_{OTL}	Output Voltage Tolerance	I_{OUT} = 10mA $V_{OUT\ (NOM)}$ +1V ≤ V_{IN} ≤ 20V	EMP8042	-2.5		+2.5	% of $V_{OUT\ (NOM)}$
			EMP8042B	**-1**		**+1**	
Vref	Reference voltage		EMP8042	1.176	1.200	1.224	V
			EMP8042B	**1.188**	**1.200**	**1.212**	
I_{OUT}	Maximum Output Current	Average DC Current Rating		150			mA
I_{LIMIT}	Output Current Limit			300			mA
I_Q	Supply Current	I_{OUT} = 0.1mA			13	50	μA
		I_{OUT} = 100mA			50	100	
		I_{OUT} = 150mA			80	130	
	Shutdown Supply Current	V_{OUT} = 0V, EN = GND			1	5	
V_{DO}	Dropout Voltage V_{OUT}=5.0V (Note. 7)	I_{OUT} = 30mA			135		mV
		I_{OUT} = 100mA			500		
		I_{OUT} = 150mA			780		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 20V			0.1		%
	Load Regulation	0.1mA ≤ I_{OUT} ≤ 100mA			0.5		%
e_n	Output Voltage Noise	I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz V_{OUT} = 5.0V			800		μV_{RMS}
V_{EN}	EN Input Threshold	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 20V		1.0			V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 20V				0.3	
I_{EN}	EN Input Bias Current	EN = GND or V_{IN}			0.1		μA
T_{SD}	Thermal Shutdown Temperature				160		℃
	Thermal Shutdown Hysteresis				30		
t_{ON}	Start-Up Time	C_{OUT} = 1.0μF, V_{OUT} at 90% of Final Value			500		μs

Note 1: Absolute maximum ratings indicate limits beyond which damage may occur.

Note 2: All voltages are in respect to the potential of the ground pin.

Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a high effectively thermal conductivity test board (2 layers, 2S0P).

Note 4: θ_{JC} represents the resistance between the chip and the top of the package case.

Note 5: Maximum power dissipation for the device is calculated using the following equation:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For example, for the SOT-89-3 package θ_{JA}=101°C/W, T_J(MAX)=160°C and using T_A=25°C, the maximum power dissipation is 1.33W.
The derating factor (-1/θ_{JA})=-9.9mW/°C. Below 25°C the power dissipation figure can be increased by 9.9mW per degree and similarly decreased by this factor for temperatures above 25°C.

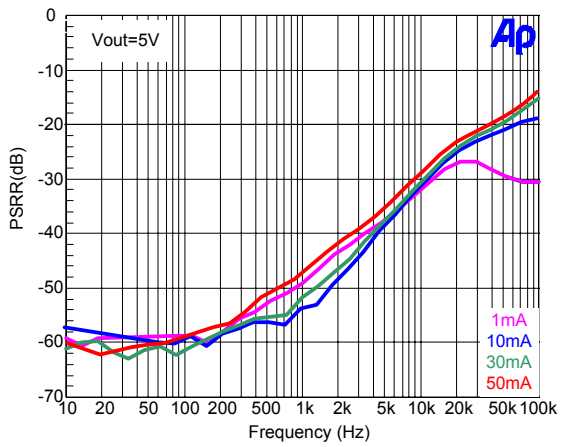
Note 6: Typical values represent the most likely parametric norm.

Note 7: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops to 98% its nominal value.

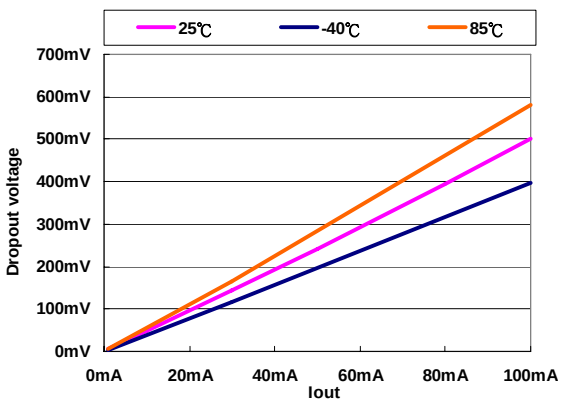
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C

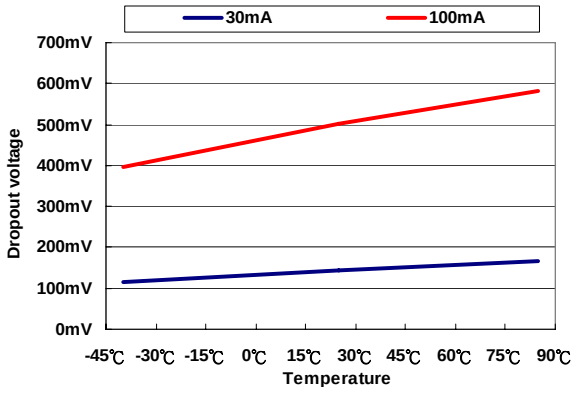
PSRR vs. Frequency (V_{OUT}=5.0V)



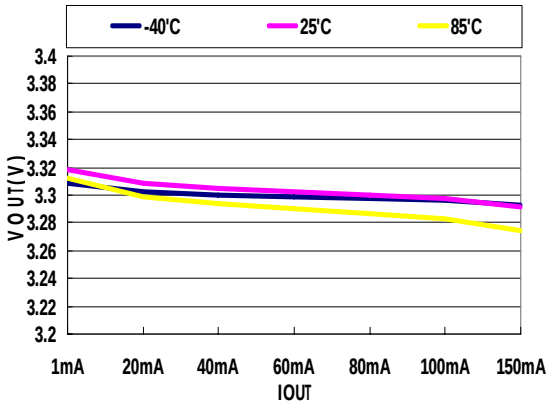
Dropout Voltage vs. Load Current (V_{OUT}=5.0V)



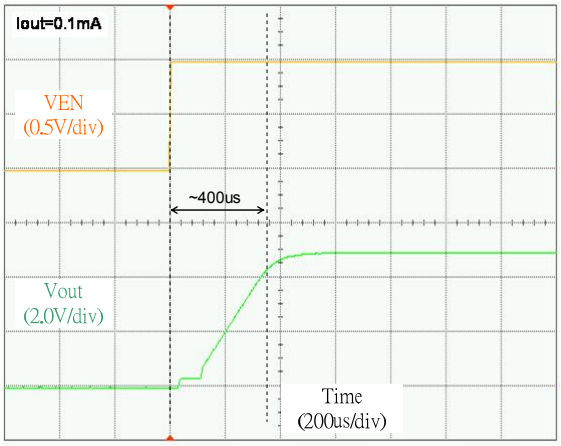
Dropout Voltage vs. Temp (V_{OUT}=5.0V)



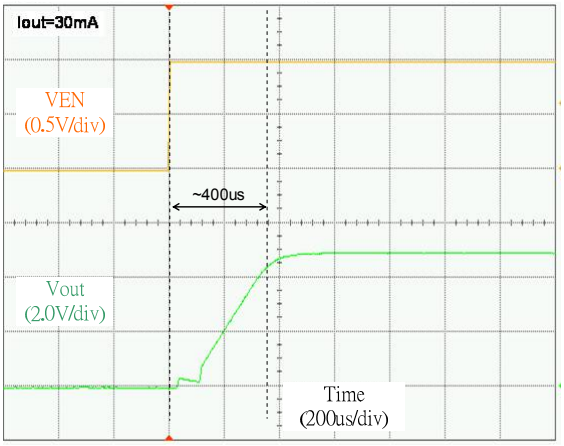
V_{OUT} vs. I_{OUT} (V_{OUT}=3.3V)



Enable Response (V_{OUT}=5.0V, I_{OUT}=0.1mA)



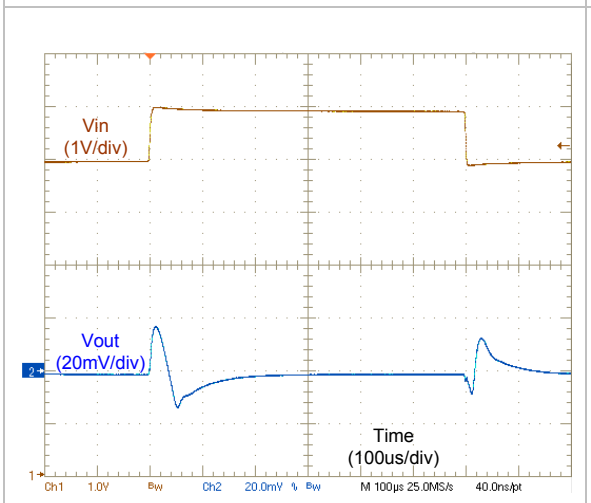
Enable Response (V_{OUT}=5.0V, I_{OUT}=30mA)



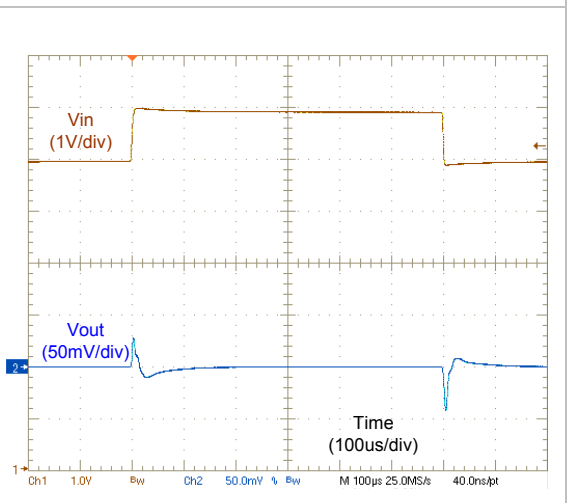
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C

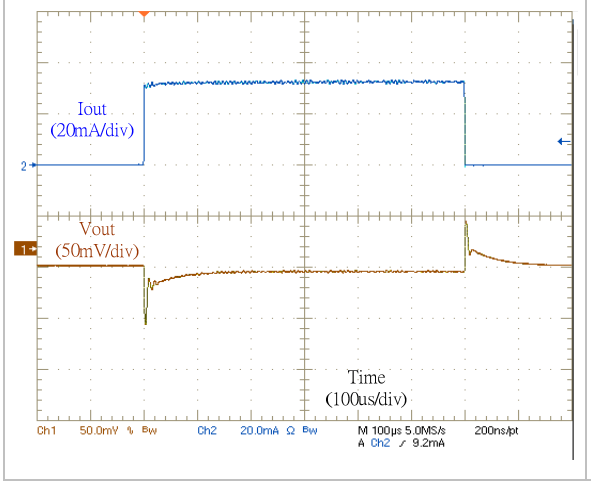
Line transient (I_{OUT}=1mA)



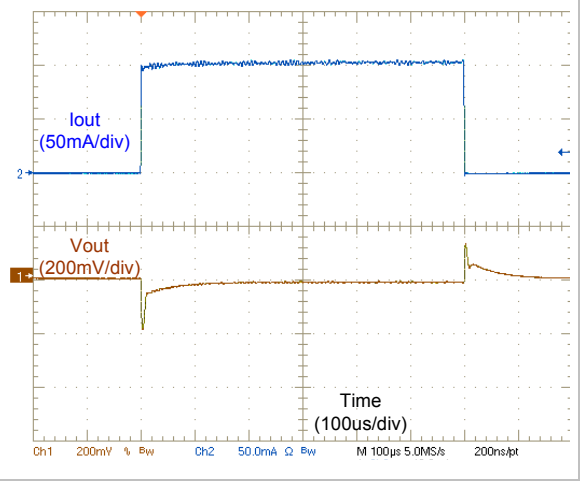
Line transient (I_{OUT}=30mA)



Load transient (V_{OUT}=5.0V)



Load transient (V_{OUT}=5.0V)



Application Information

General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the EMP8042 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By the virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

The EMP8042 is specially designed for use with ceramic output capacitors of as low as 1.0μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) is restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8042 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8042 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8042. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8042 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature T_J exceeding 160°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

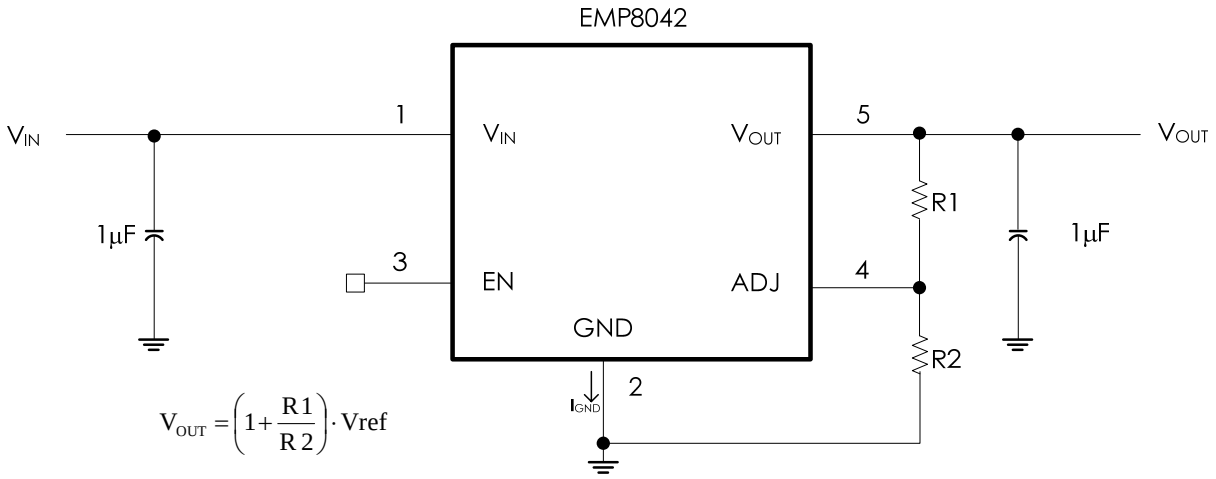
$$T_J = \theta_{JA} \times (P_D) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

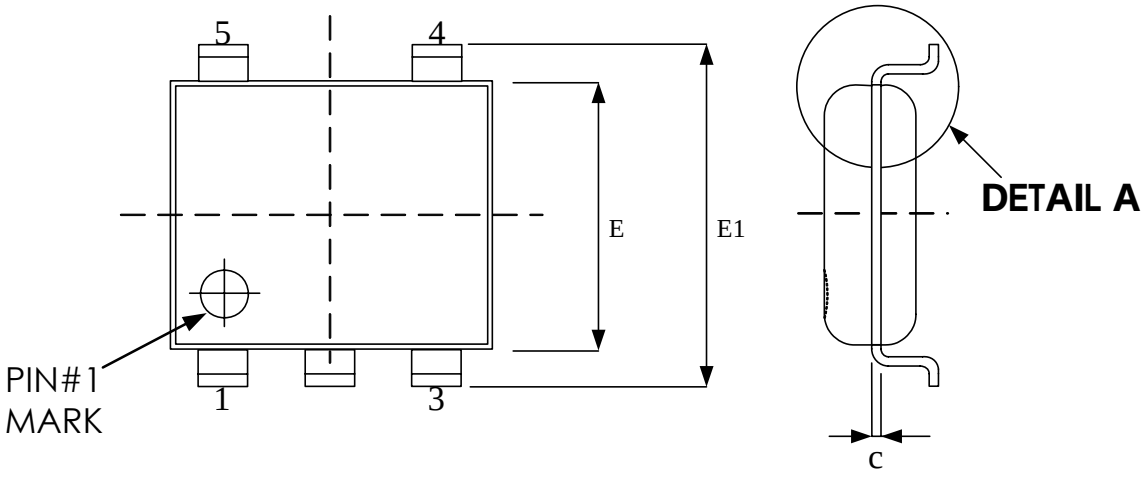
$$P_D = I_{OUT} (V_{IN} - V_{OUT})$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8042, refrain from exceeding the absolute maximum junction temperature rating of 160°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

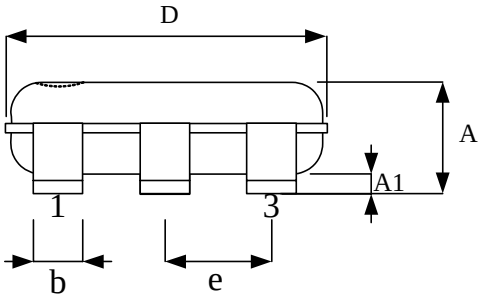
Application Circuit for ADJ output



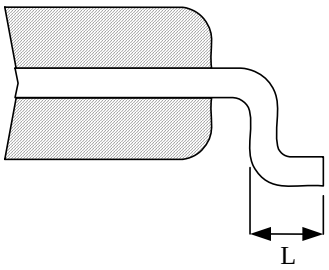
Package Outline Drawing
SOT-23-5



TOP VIEW



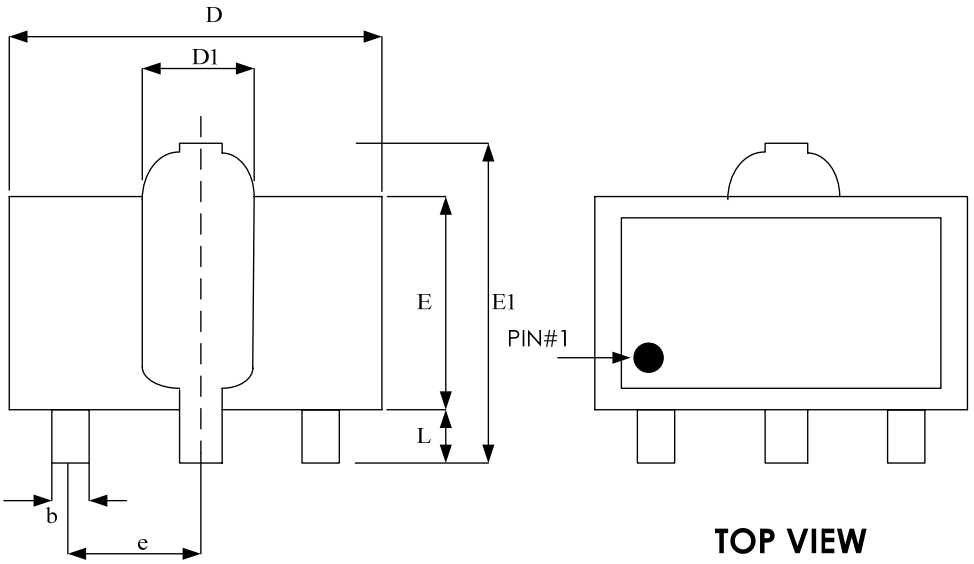
SIDE VIEW



DETAIL A

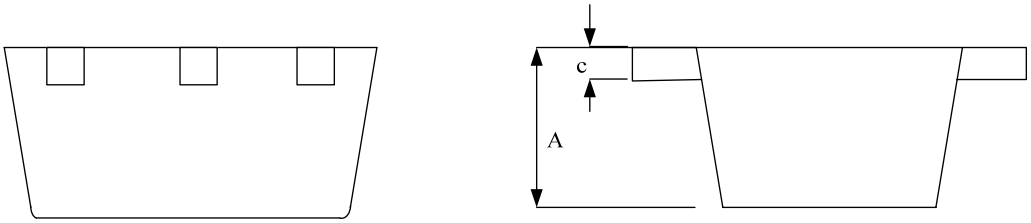
Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Package Outline Drawing
SOT-89-3



TOP VIEW

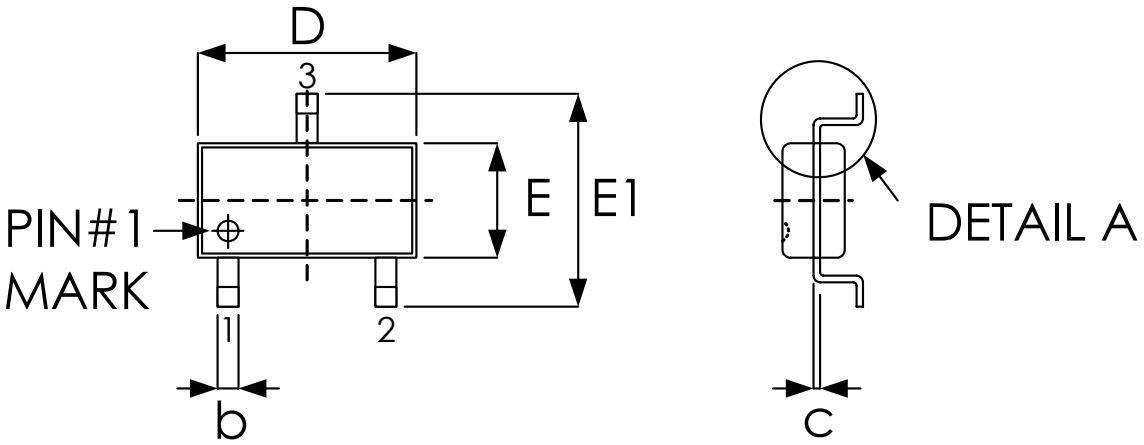
BOTTOM VIEW



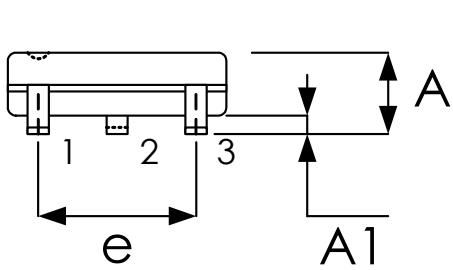
SIDE VIEW

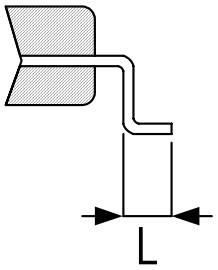
Symbol	Dimension in mm	
	Min	Max
A	1.4	1.6
b	0.4	0.56
c	0.35	0.41
D	4.4	4.6
D1	1.5	1.83
E	2.29	2.6
E1	3.94	4.25
e	1.50 BSC	
L	0.89	1.2

Package Outline Drawing
SOT-23-3



TOP VIEW





SIDE VIEW **DETAIL A**

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	1.90 BSC	
L	0.30	0.60

Revision History

Revision	Date	Description
0.1	2010.08.27	Original
1.0	2011.02.23	1. Skip “Preliminary” 2. Page1 revise “Typical Application“ 3. Page2 add SOT-23-5 package 4. Page3 add SOT-23-5 “Pin Functions”
1.1	2011.12.12	1) Added ADJ output voltage option 2) Modified 100mA output driving capacity to 150mA. 3) Modified the output voltage accuracy is based on Iout=10mA this condition. 4) Added Iout=150mA spec. into electrical characteristics table.
1.2	2012.04.20	1) Added the typical value of supply current I_Q=13uA at Iout=0.1mA. 2) Updated the maximum value of supply current I_Q=50uA at Iout=0.1mA. 3) Updated the package outline drawing.
1.3	2012.08.31	1) Added the typical value of shutdown supply current I_Q=1uA at EN=GND. 2) Added the EN input Threshold.
1.4	2013.10.04	Updated the package outline drawing.
1.5	2017.06.26	Added EMP8042B series product

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