High Input Voltage, Low Quiescent Current, Low-Dropout Linear Regulator

General Description

The EMP8045 is a high voltage, low quiescent current, low dropout regulator with 150mA output driving capacity. The EMP8045, which operates over an input range of 3V to 32V, is stable with any capacitors, whose capacitance is larger than 1μF, and suitable for powering battery-management ICs because of the virtue of its low quiescent current consumption and low dropout voltage. EMP8045 also includes bandgap voltage reference, Foldback current limiting and thermal overload protection.

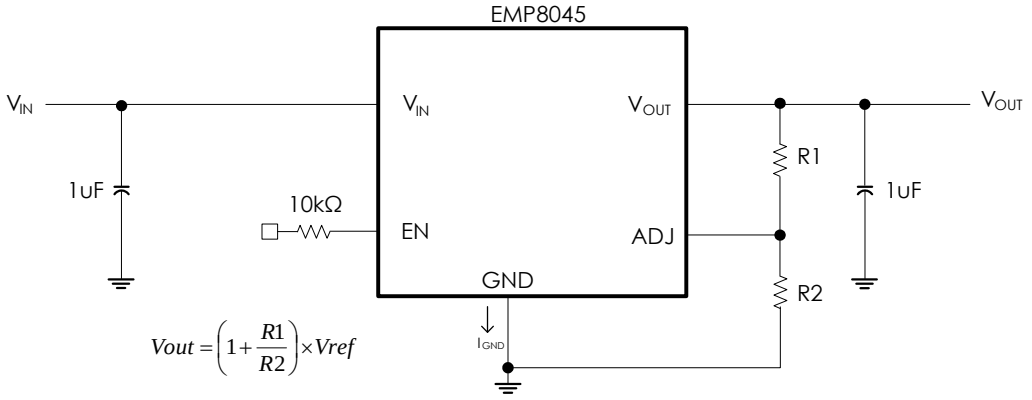
Features

- AEC-Q100 qualified
- 150mA output current driving capacity
- 780mV typical dropout at Io=150mA@V_{OUT}=5V
- 10μA typical quiescent current
- 1μA typical shutdown mode
- 3.0V to 32V input range
- Stable with small ceramic output capacitors (1μF)
- Over temperature and over current protection
- ±1.5% output voltage tolerance

Applications

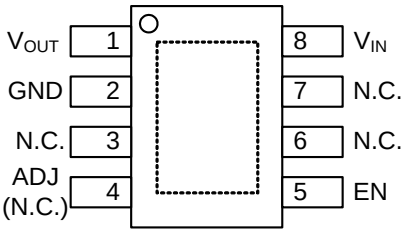
- Logic Supply for High Voltage Batteries
- Keep-Alive Supply
- 3-4 Cell Li-ion Batteries Powered systems
- Automotive

Typical Application



Note: R1≥10k is strongly recommended. Especially, Vout was set around Vref

Connection Diagrams



N.C.: No Connection
For Fixed Vout, Pin4= No Connection

Order information

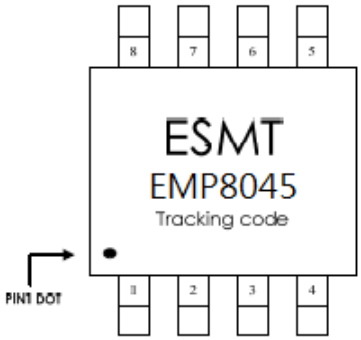
EMP8045-XXSG08VCR

XX Output voltage

SG08 E-SOP-8 Package

VCR RoHS & Halogen free package
Rating: -40 to 125°C
Package in Tape & Reel

Order, Marking & Packing Information

Package	Vout	Product ID.	Marking	Packing
E-SOP-8L	ADJ	EMP8045-00SG08VCR		Tape & Reel 3kpcs
	3.3V	EMP8045-33SG08VCR		
	5.0V	EMP8045-50SG08VCR		

Pin Functions

Pin No.	Name	Function
1	**VOUT**	**Output Voltage**
2	**GND**	**Ground Pin**
3	**N.C.**	**No connect**
4	**ADJ (N.C.)**	**Output Voltage Adjust:** Feedback input. Connect to resistive voltage-divider network. R1≥10k is strongly recommended. Especially, Vout was set as Vref No connect for Fixed Vout.
5	**EN**	**Shutdown Input** The EN pin is pulled "High" internally. Set the regulator into the disable mode by pulling the EN pin low.
6	**N.C.**	**No connect**
7	**N.C.**	**No connect**
8	**VIN**	**Supply Voltage Input** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.

Functional Block Diagram

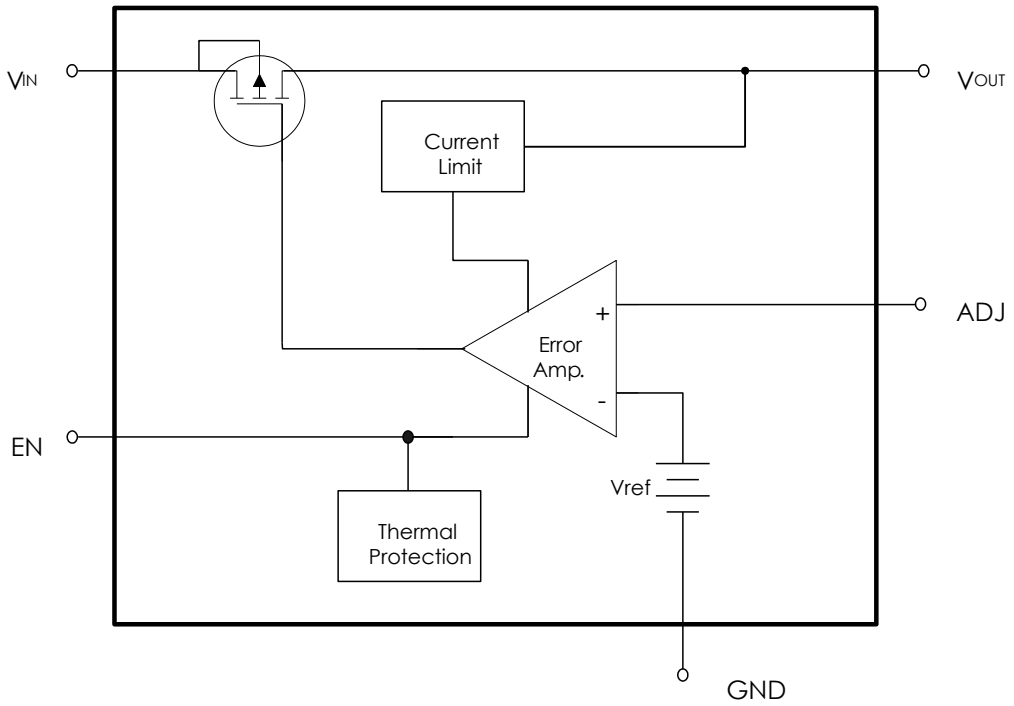


FIG.1. Functional Block Diagram of EMP8045

Absolute Maximum Ratings (Notes 1, 2)

V_{IN}, EN	-0.3V to 36V	Lead Temperature (Soldering, 10 sec.)	260°C
V_{OUT}	-0.3V to 8V	ESD Rating	
Power Dissipation	(Note 3)	Human Body Model	+-2KV
Storage Temperature Range	-65°C to 150°C	Charged Device Model	+-750V
Junction Temperature (T_J)	150°C	Latch up	+-100mA

Operating Ratings (Note 1, 2)

Supply Voltage	3.0V to 32V	Operating Temperature Range	-40°C to 125°C

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 4)	Junction-to-ambient	50°C/W
	$\theta_{JC(top)}$ (Note 5)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 6)	Junction-case (bottom)	10°C/W

Electrical Characteristics

V_{OUT}(NOM)=5V; unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V, EN = 2V, C_{IN} = C_{OUT} =1μF. T_A=-40°C to 125°C, typical value is T_A=+25°C

Symbol	Parameter	Conditions	Min	Typ (Note7)	Max	Units
Vref	Reference voltage	I_{OUT} = 0.1mA V_{IN}=$V_{OUT(NOM)}$ +1V ≤ V_{IN} ≤ 36V T_A= 25°C	1.228	1.24	1.252	V
		I_{OUT} = 0.1mA V_{IN}=$V_{OUT(NOM)}$ +1V ≤ V_{IN} ≤ 36V T_A= -40°C ~ 125°C	1.222	1.24	1.258	
TC	Vref temperature coefficient	V_{IN} = V_{OUT} +1V, EN = 2V, I_{OUT} = 0.1mA Refer to T_A= 25°C	-100	±50	100	ppm/℃
I_{OUT}	Maximum Output Current	Average DC Current Rating	150			mA
I_{LIMIT}	Output Current Limit	V_{IN} = 6V; T_A= -40°C ~ 125°C Over-Loading	180	240	300	mA
I_{Short}	Short Circuit Current	V_{IN} = 6V; T_A= -40°C ~ 125°C V_{OUT} Short to GND	70	100	130	mA
I_Q	Supply Current	I_{OUT} = 0.1mA		12	30	μA
		I_{OUT} = 100mA		50	100	
	Shutdown Supply Current	V_{OUT} = 0V, EN = GND		1.5	5	
V_{DO}	Dropout Voltage V_{OUT}=5.0V (Note. 8)	I_{OUT} = 30mA, T_A= -40°C ~ 125°C		135	250	mV
		I_{OUT} = 100mA, T_A= -40°C ~ 125°C		450	900	
		I_{OUT} = 150mA, T_A= -40°C ~ 125°C		780	1500	
ΔV_{OUT}	Line Regulation	I_{OUT} = 0.1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 36V		0.1	0.2	%
	Load Regulation	0.1mA ≤ I_{OUT} ≤ 100mA		0.5	1	%
e_n	Output Voltage Noise	I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz V_{OUT} = 5.0V		800		μV_{RMS}

V_{EN}	EN Input Threshold	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 36V	1.0			V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 36V			0.3	
I_{EN}	EN Input Bias Current	EN = GND or V_{IN} (V_{IN}<6V)		0.15	0.3	μA
T_{SD}	Thermal Shutdown Temperature(Note. 9)			160		℃
	Thermal Shutdown Hysteresis (Note. 9)			30		
t_{ON}	Start-Up Time	C_{OUT} = 1.0μF, V_{OUT} at 90% of Final Value		500		μs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the E-SOP-8 packageθ_{JA} = 50°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 2.5W. The derating factor (-1/θ_{JA}) = -20mW/°C, thus below 25°C the power dissipation figure can be increased by 20mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 4: θ_{JA} is simulated in the natural convection at T_A=25℃ on a highly effective thermal conductivity (thermal land area completed with >3x3cm^2 area) board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 5: $\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.

Note 6: $\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.

Note 7: Typical Values represent the most likely parametric norm

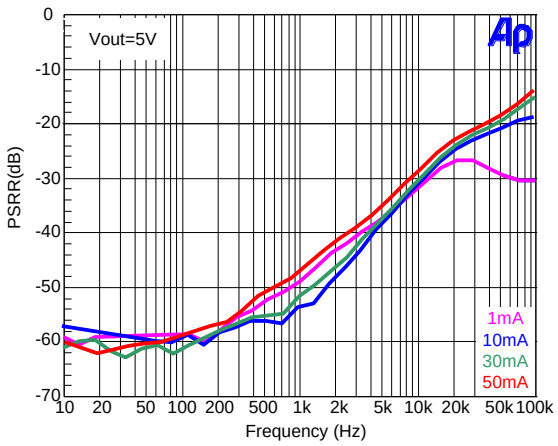
Note 8: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops to 98% its nominal value.

Note 9: Design Guarantee

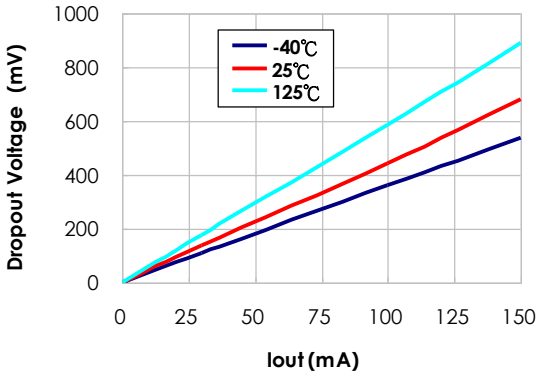
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

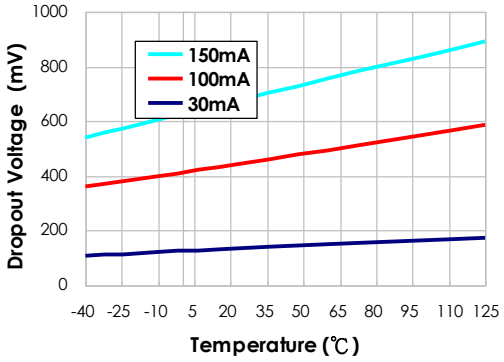
PSRR vs. Frequency (V_{IN}=6V, V_{OUT}=5V)



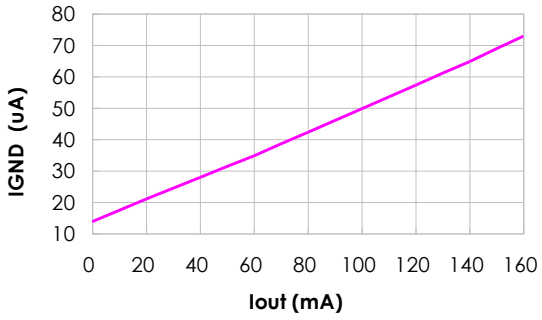
Dropout Voltage vs. Load Current (V_{OUT}=5.0V)



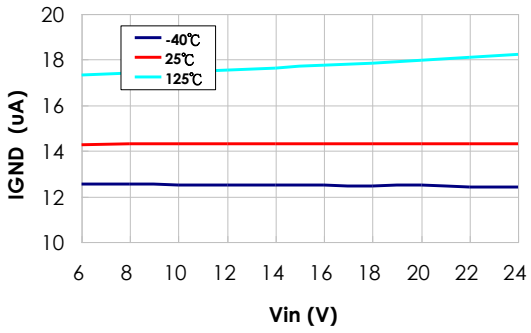
Dropout Voltage vs. Temp (V_{OUT}=5.0V)



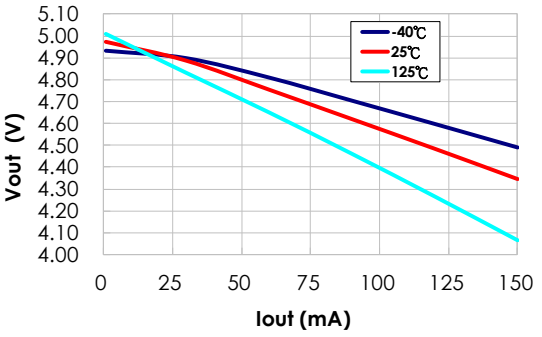
Ground Current vs. Iout (V_{OUT}=5.0V, T_A=25'C)



Ground Current vs. V_{IN} (V_{OUT}=5.0V)



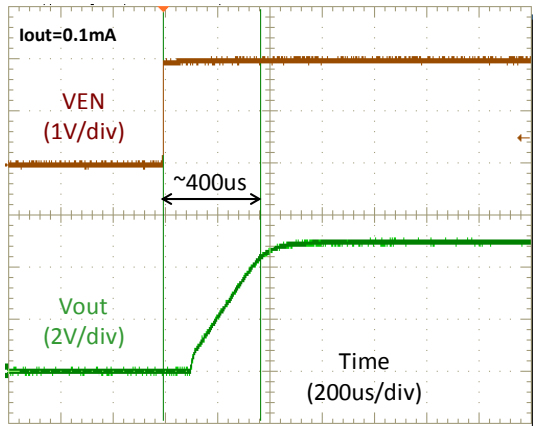
V_{OUT} vs. Iout (V_{OUT}=5.0V)



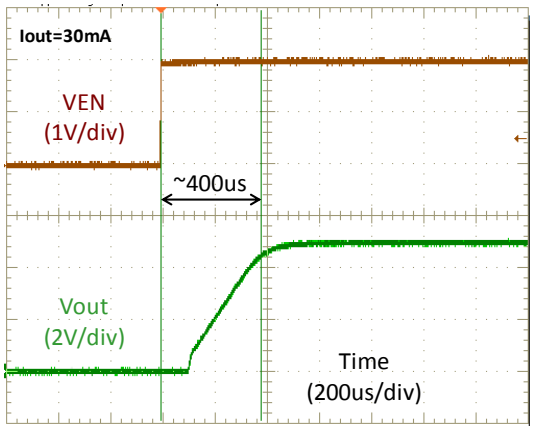
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

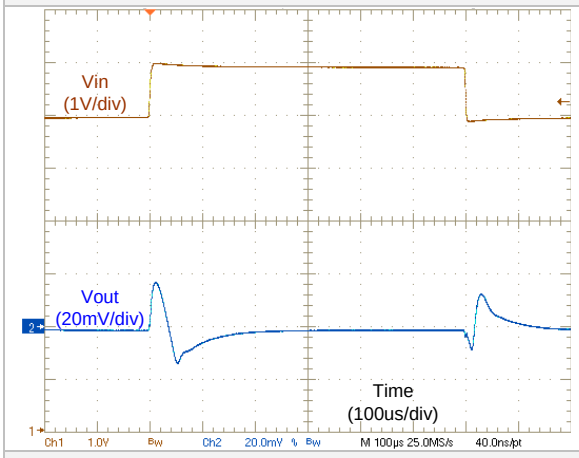
Enable Response (V_{OUT}=5.0V, IOUT=0.1mA)



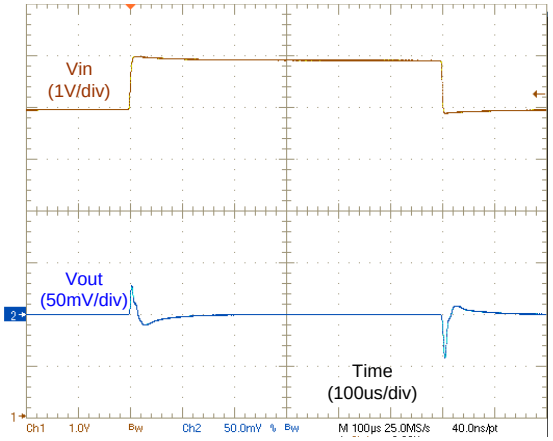
Enable Response (V_{OUT}=5.0V, IOUT=30mA)



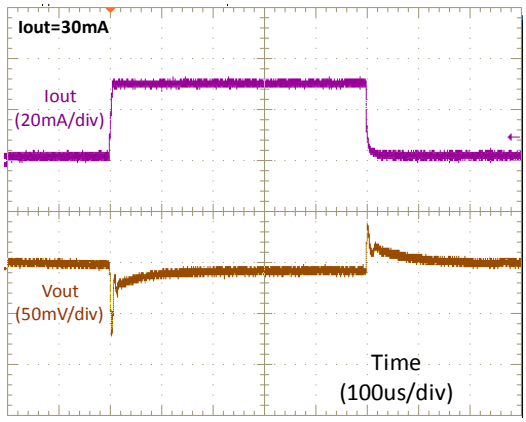
Line transient (Iout=1mA)



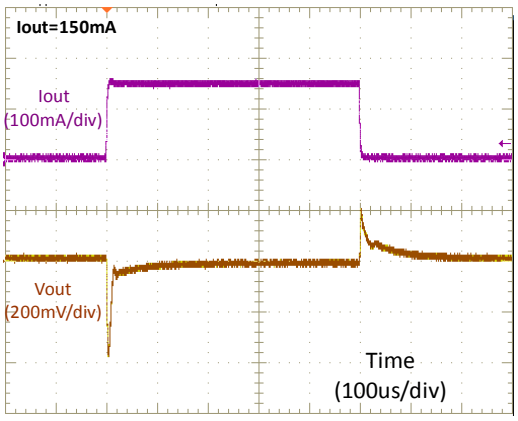
Line transient (Iout=30mA)



Load transient (V_{OUT}=5.0V)



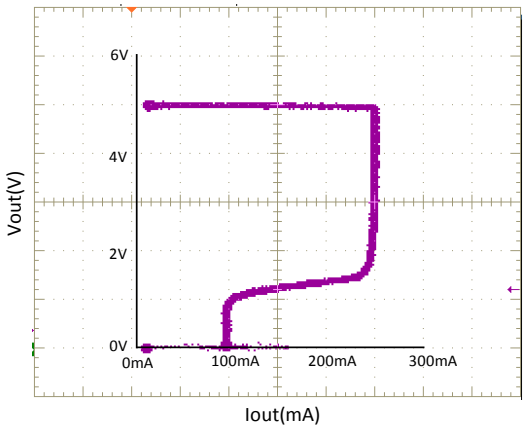
Load transient (V_{OUT}=5.0V)



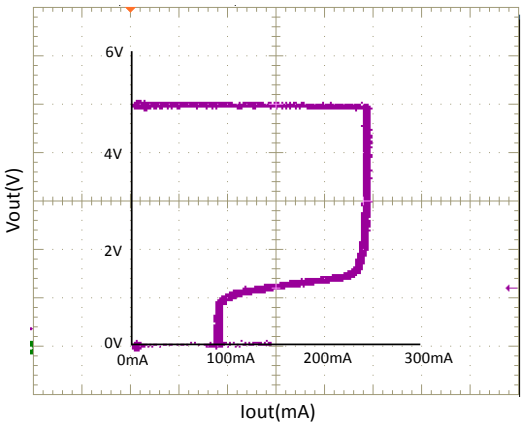
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{OUT}=5V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, EN = 2V

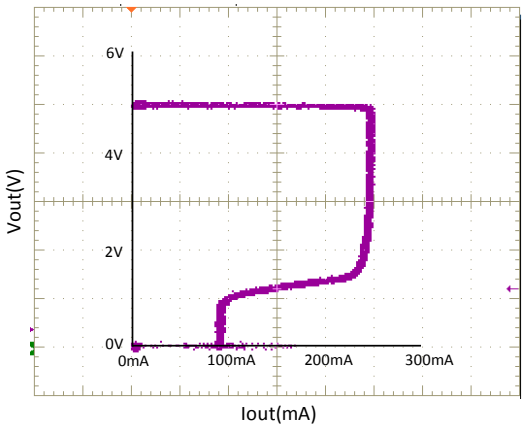
Current Limit Vin=12V (Note 10)



Current Limit Vin=24V (Note 10)



Current Limit Vin=36V (Note 10)



Note 10 : The Foldback current limit waveform is tested by enabling on EMP8045 with Cout=1000uF.

Application Information

General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the EMP8045 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By the virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry. With sensing output voltage, the current limit level would be Foldback to lower level during Vout shorted to GND

Output Capacitor

The EMP8045 is specially designed for use with ceramic output capacitors of as low as 1.0μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) is restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8045 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8045 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8045. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8045 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature T_J exceeding 150°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA} \times (P_D) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

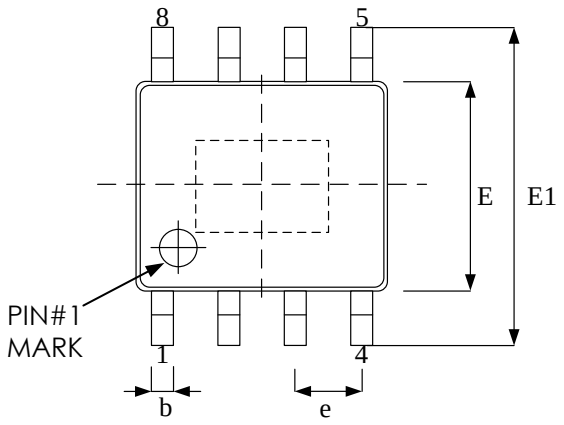
$$P_D = I_{OUT} (V_{IN} - V_{OUT})$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8045, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

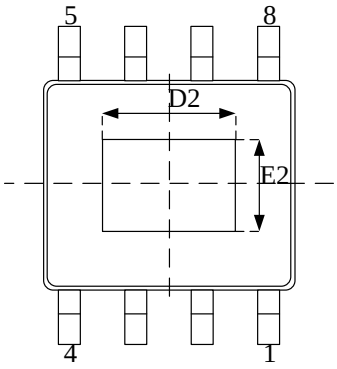
Shutdown

The EMP8045 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1μA. Such a low supply current makes the EMP8045 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.3V. The EN pin is pulled high internally.

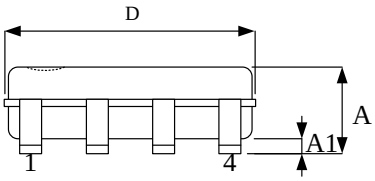
Package Outline Drawing
E-SOP-8



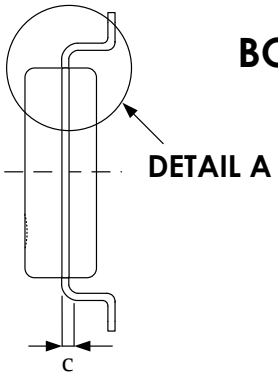
TOP VIEW

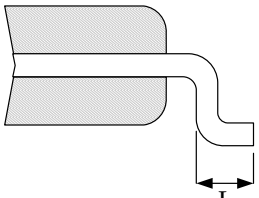


BOTTOM VIEW



SIDE VIEW





DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	1.35	1.75
A1	0.00	0.25
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.84	3.30
E2	2.06	2.41

Revision History

Revision	Date	Description
0.1	2017.07.19	Initial version (Preliminary).
0.2	2017.08.29	Update application circuit
0.3	2018.01.25	Update Vout max to 8V
0.4	2018.08.01	Delete 3.0V option
1.0	2018.09.06	Remove preliminary and change version to 1.0
1.1	2018.10.17	1. Modified EN pin description. 2. Added ESD charge device mode and latch up pass level.

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