

3-W/CH Stereo Filter-less Class-D Audio Power Amplifier with Auto-Recovery

DESCRIPTION

The EUA2034 is a high efficiency, 3W/channel stereo class-D audio power amplifier. A low noise, filterless PWM architecture eliminates the output filter, requiring only two external components for operation.

Operating from a single 5V supply, EUA2034 is capable of delivering 3W/ channel of continuous output power to a 4Ω load with 10% THD+N.

The EUA2034 is available in space-saving SOP-16 package.

FEATURES

- Unique Modulation Schema Reduces EMI Emissions
- 3W Output at 10% THD with a 4Ω Load and 5V Power Supply
- Low Quiescent Current and Shutdown Current
- Low THD+N and Low Noise
- Efficiency up to 87%
- Short Circuit Protection with Auto-Recovery
- Thermal Protection
- Optimized PWM Output Stage Eliminates LC Output Filter
- Available in Space-Saving SOP-16 Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- LCD Monitors / TV Projectors
- Notebook Computers
- Portable Speakers
- Portable DVD Players, Game Machines
- Cellular Phones/Speaker Phones

Typical Application Circuit

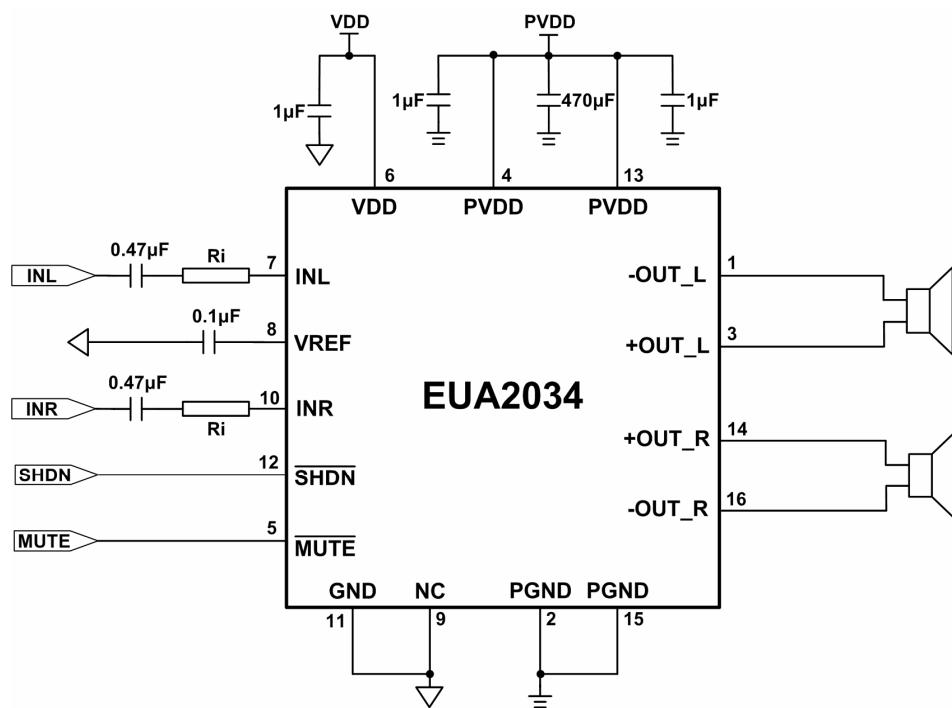
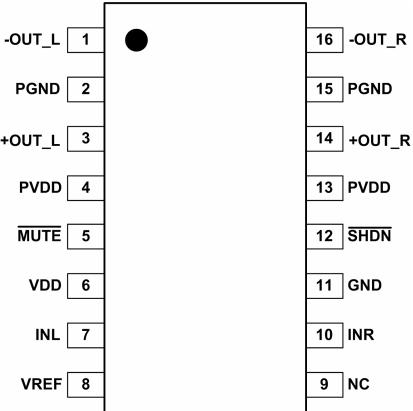


Figure1.

Pin Configurations

Package Type	Pin Configurations
SOP-16	 <p>The diagram shows a top-down view of a 16-pin SOP package. Pin 1 is at the top left, followed by PGND (2), +OUT_L (3), PVDD (4), MUTE (5), VDD (6), INL (7), and VREF (8) on the left side. On the right side, starting from the top, are -OUT_R (16), PGND (15), +OUT_R (14), PVDD (13), SHDN (12), GND (11), INR (10), and NC (9).</p>

Pin Description

PIN	SOP-16	DESCRIPTION
-OUT_L	1	Left Channel Negative Output
PGND	2	Power GND
+OUT_L	3	Left Channel Positive Output
PVDD	4	Power GND
MUTE	5	Mute Control Input (active low)
VDD	6	Analog VDD
INL	7	Left Channel Input
VREF	8	Internal analog reference, connect a bypass capacitor from VREF to GND
NC	9	No connect
INR	10	Right Channel Input
GND	11	Analog GND
SHDN	12	Shutdown Control Input (active low)
PVDD	13	Power VDD
+OUT_R	14	Right Channel Positive Output
PGND	15	Power GND
-OUT_R	16	Right Channel Negative Output

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2034DIR1	SOP-16	 XXXXX A2034	-40 °C to +85°C

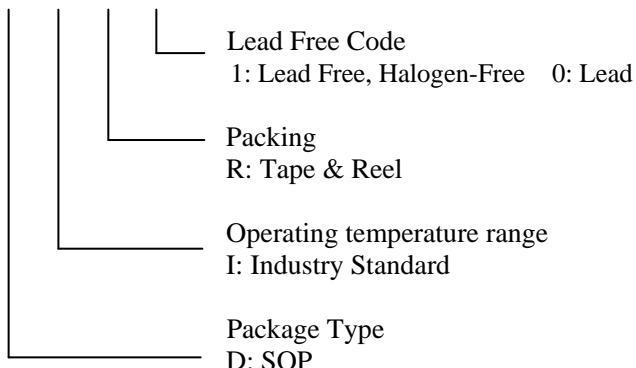
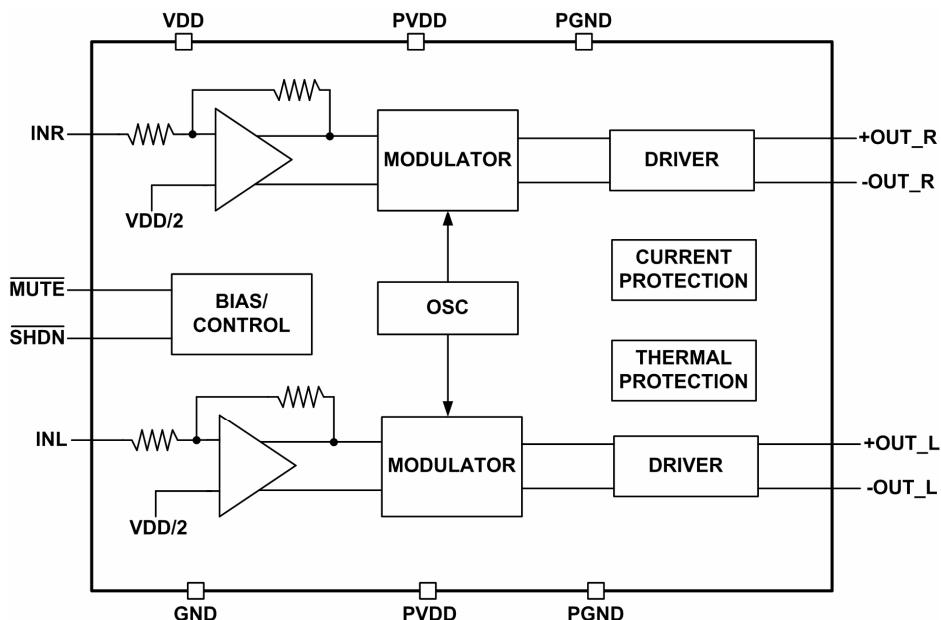
EUA2034 **Block Diagram**

Figure2.

Absolute Maximum Ratings (1)

■ Supply Voltage, AVDD,PVDD -----	-0.3 V to 6V
■ Input Voltage, V_I -----	-0.3 V to V_{DD} +0.3V
■ Junction Temperature, T_J -----	-40°C to 150°C
■ Storage Temperature Rang, T_{stg} -----	-65°C to 85°C
■ ESD Susceptibility -----	2kV
■ Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds -----	260°C
■ Thermal Resistance θ_{JA} (SOP-16) -----	80°C/W

Recommended Operating Conditions (2)

	Min	Max	Unit
Supply voltage	2.5	5.5	V
High-level input voltage	1.4		V
Low-level input voltage		0.35	V
Operating free-air temperature, T_A	-40	85	°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics $V_{DD}=5V$, Gain=24dB, $R_L=8\Omega$, $T_A = +25^\circ C$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2034			Unit
			Min.	Typ.	Max.	
V_{IN}	Supply Power		2.5		5.5	V
P_O	Output Power	THD+N=10%, f=1kHz, $R_L=4\Omega$	$V_{DD}=5V$		3	
			$V_{DD}=3.6V$		1.42	
			$V_{DD}=3V$		1	
		THD+N=1%, f=1kHz, $R_L=4\Omega$	$V_{DD}=5V$		2.3	
			$V_{DD}=3.6V$		1.15	
			$V_{DD}=3V$		0.8	
		THD+N=10%, f=1kHz, $R_L=8\Omega$	$V_{DD}=5V$		1.72	
			$V_{DD}=3.6V$		0.85	
			$V_{DD}=3V$		0.6	
		THD+N=1%, f=1kHz, $R_L=8\Omega$	$V_{DD}=5V$		1.4	
			$V_{DD}=3.6V$		0.7	
			$V_{DD}=3V$		0.48	
THD+N	Total Harmonic Distortion Plus Noise	$V_{DD}=5V, P_O=0.5W, R_L=8\Omega$	f=1kHz		0.21	
		$V_{DD}=3.6V, P_O=0.5W, R_L=8\Omega$			0.19	
		$V_{DD}=5V, P_O=1W, R_L=4\Omega$	f=1kHz		0.27	
		$V_{DD}=3.6V, P_O=1W, R_L=4\Omega$			0.28	
Gv	Gain				24	
PSRR	Power Supply Ripple Rejection	$V_{DD}=5V$, Inputs ac-grounded with $C_{IN}=0.47\mu F$	f=100Hz		-50	
			f=1kHz		-50	

Electrical Characteristics $V_{DD}=5V$, Gain=24dB, $R_L=8\Omega$, $T_A = +25^\circ C$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2034			Unit	
			Min	Typ	Max.		
Cs	Crosstalk	$V_{DD}=5V$, $P_0=0.5W$, $R_L=8\Omega$, $Gv=24dB$	f=1kHz	-90		dB	
SNR	Signal-to-noise ratio	$V_{DD}=5V$, $V_{ORMS}=1V$, $Gv=24dB$	f=1kHz	80		dB	
Vn	Output noise	$V_{DD}=5V$, Inputs ac-grounded with $C_{IN}=0.47\mu F$	A-weighting	100		μV	
			No A-weighting	130			
η	Efficiency	$R_L=8\Omega$, THD=10%	f=1kHz	87		%	
		$R_L=4\Omega$, THD=10%		83			
I _Q	Quiescent Current	$V_{DD}=5V$	No load	9.3		mA	
		$V_{DD}=3.6V$		8			
I _{MUTE}	Mute current	$V_{DD}=5V$		3.8		mA	
		$V_{DD}=3.6V$		3.3			
I _{SHDN}	Shutdown current	$V_{DD}=5V$		3	10	μA	
		$V_{DD}=3.6V$		1			
f _{SW}	Switching Frequency	$V_{DD}=5V$		250	350	400	KHz
V _{OS}	Output offset Voltage	$V_{DD}=5V$			25	50	mV
R _{DSON}	Static drain-source on-state resistance	$V_{DD}=5V$	NMOS	200	350	$m\Omega$	
			PMOS	300	400		
I _{IH}	High-level input current	$V_{DD}=5V$ $VI= V_{DD}$				1	μA
I _{IL}	Low-level input current	$V_{DD}=5V$ $VI= 0V$				1	μA

Typical Operating Characteristics

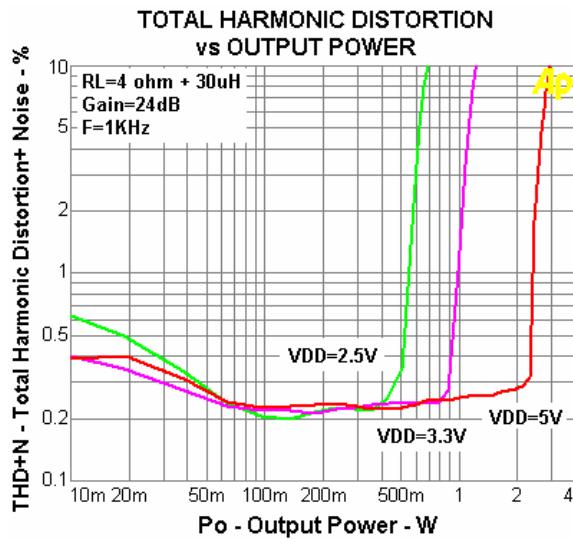


Figure3.

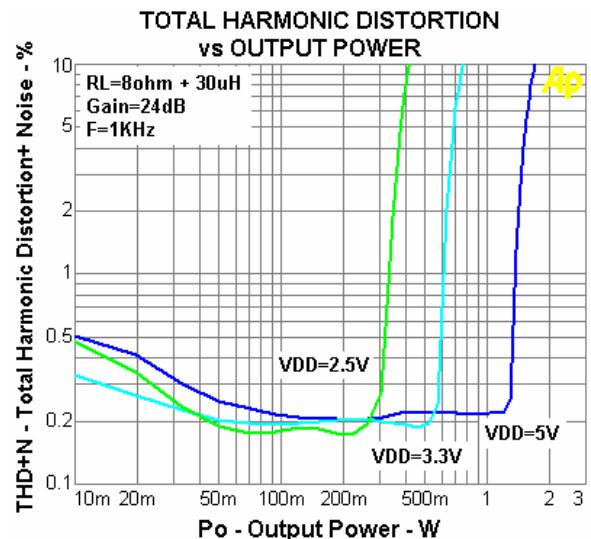


Figure4.

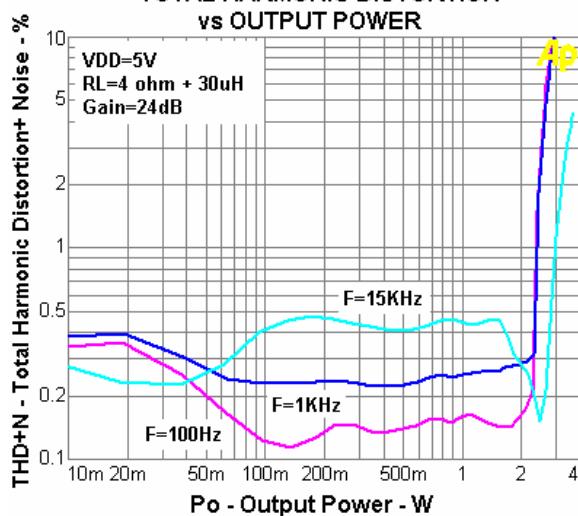


Figure5.

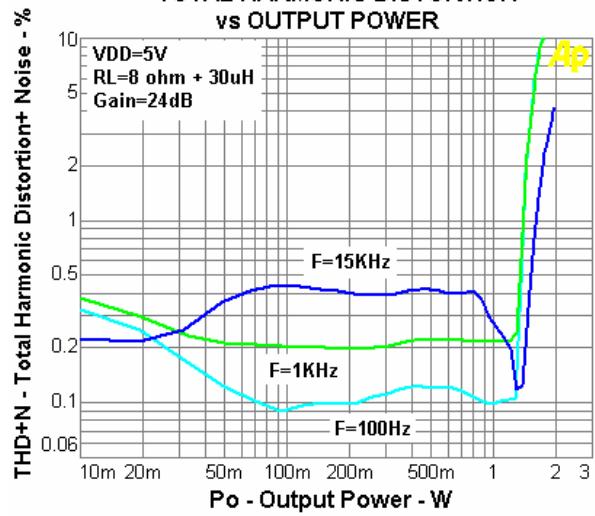


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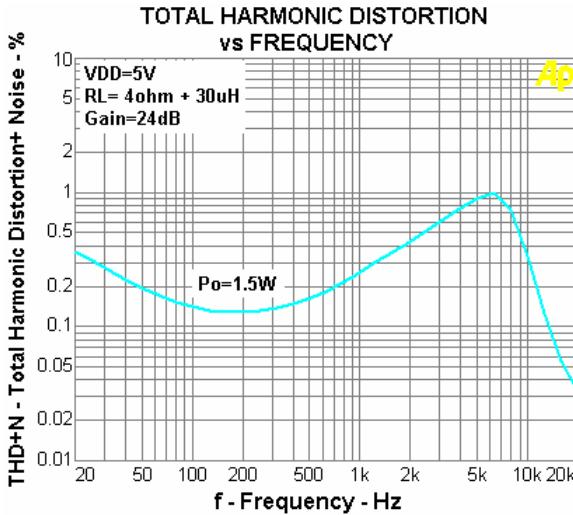


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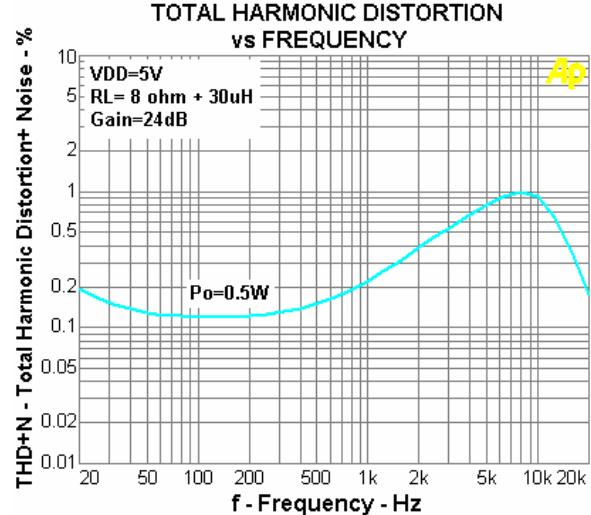


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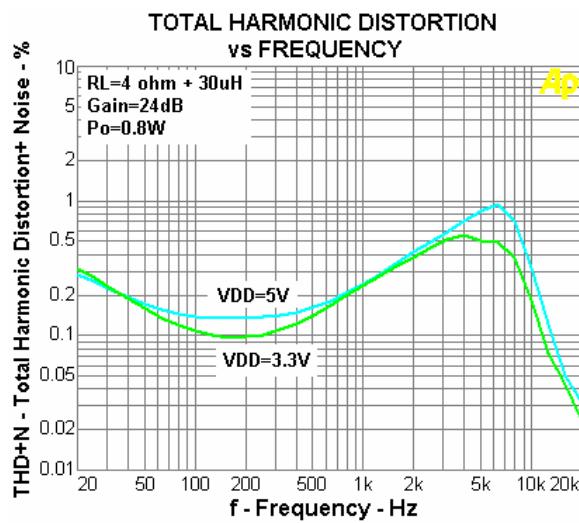


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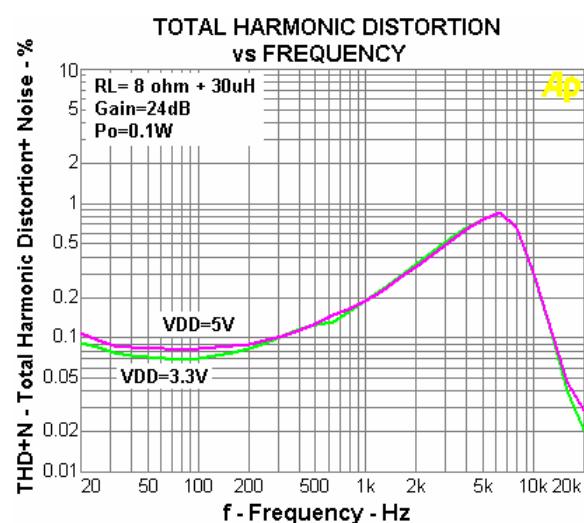


Figure10.

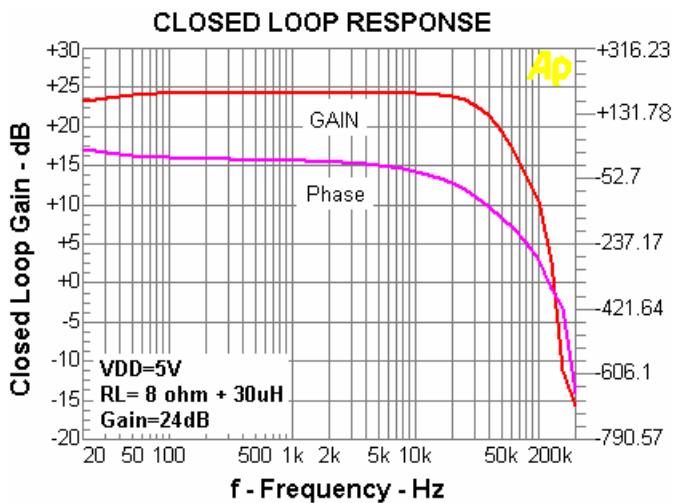


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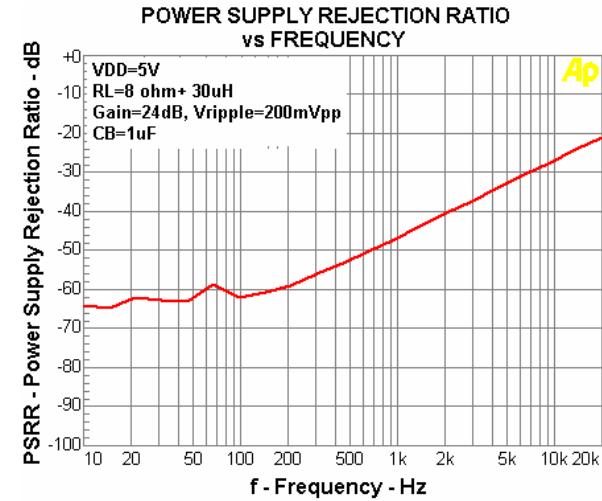


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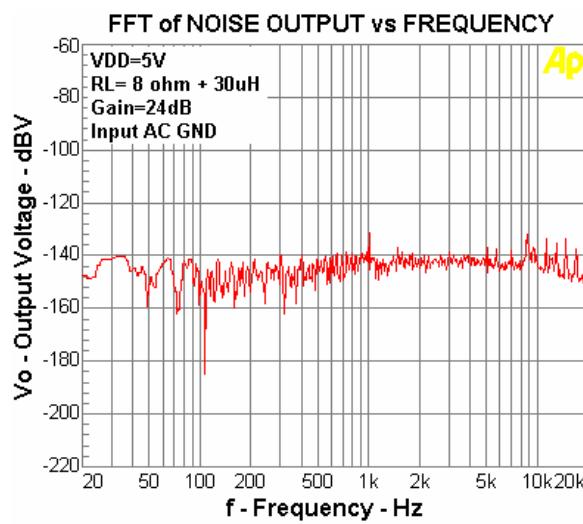


Figure13.

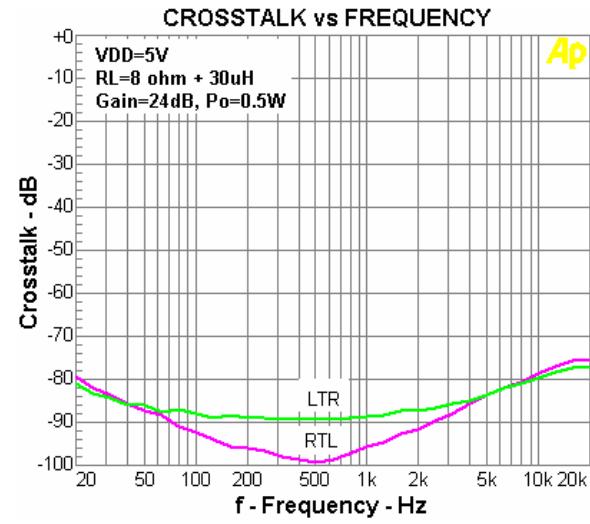


Figure14.

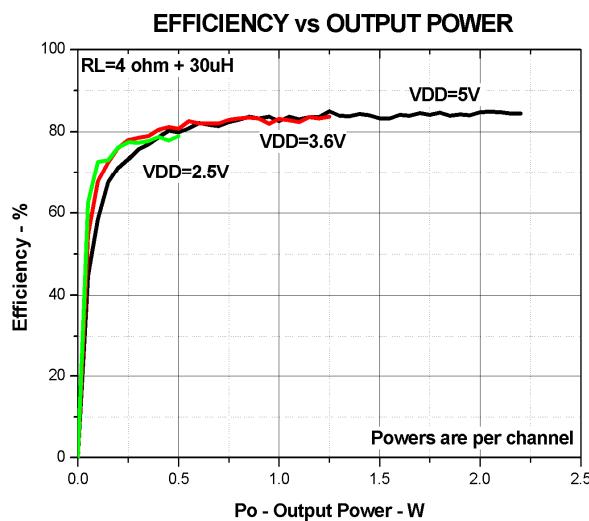


Figure15.

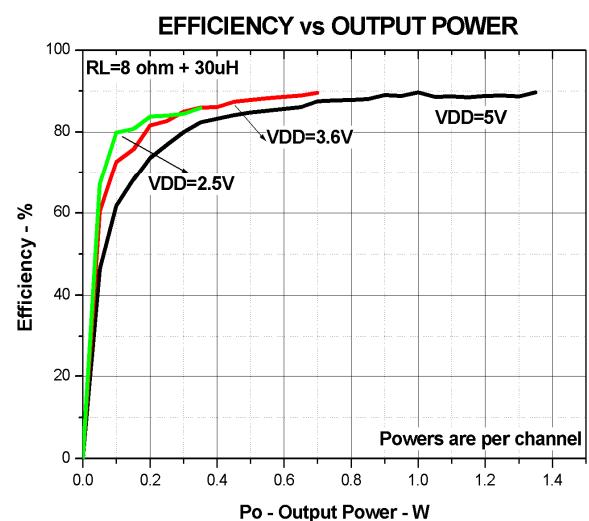


Figure16.

Application Information

Input Resistors (R_I)

The input resistors (R_I) set the gain of the amplifier according to equation (1).

$$A_{VD} = 20 * \log \left[2 * \left(R_f / R_i \right) \right] \quad \text{---(1)}$$

The EUA2034 sets maximum $R_f = 142\text{k}\Omega$, minimum $R_i = 18\text{k}\Omega$, so the maximum closed-gain is 24dB.

Decoupling Capacitor (C_S)

The EUA2034 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line a good low equivalent-series-resistance (ESR) ceramic capacitor, typically $1\mu\text{F}$, placed as close as possible to the device PV_{DD} lead works best. Placing this decoupling capacitor close to the EUA2034 is important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a $20\mu\text{F}$ or greater capacitor placed near the audio power amplifier would also help.

Input Capacitors (C_I)

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c , determined in equation (2).

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad \text{---(2)}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset.

Equation (3) is used to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad \text{---(3)}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of $\pm 10\%$ or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

SHDN Operation

Connect SHDN to a logic high for normal operation. Pulling SHDN low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SHDN unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown or mute mode prior to removing the power supply voltage.

MUTE Operation

The MUTE pin only control the output state and does not shutdown the EUA2034. A logic low on this terminal disables the outputs. A logic high on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources. The MUTE pin can be left floating due to the internal pull-up.

Component Location

Place all the external components very close to the EUA2034. Placing the decoupling capacitor, C_S , close to the EUA2034 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Filter Free Operation and Ferrite Bead Filters

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and very low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 17 shows typical ferrite bead and LC output filters.

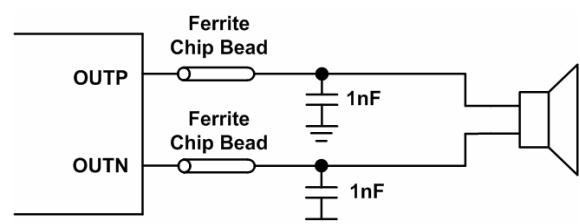
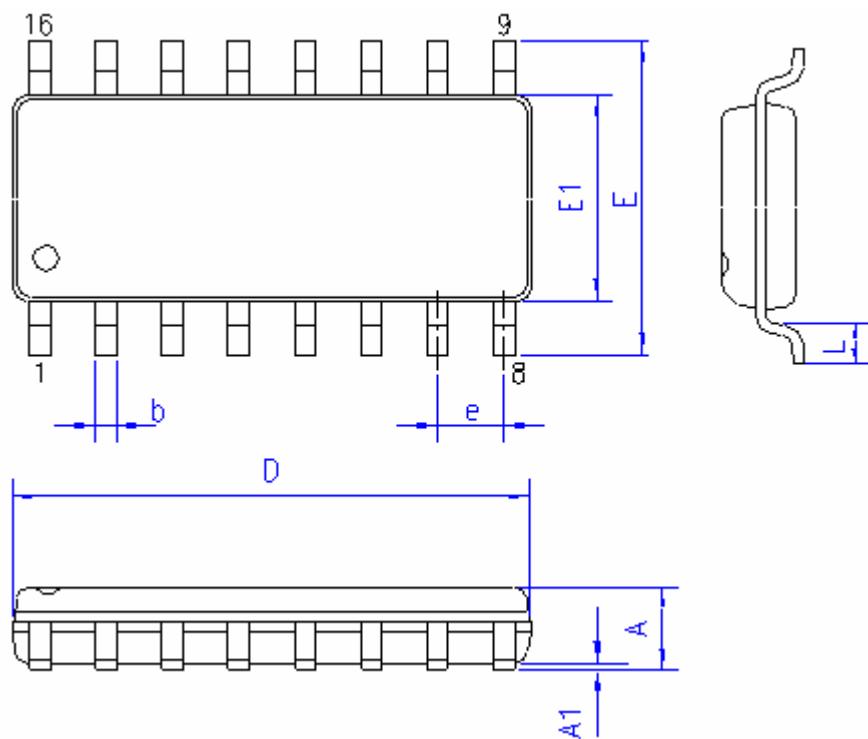


Figure 17. Typical Ferrite Chip Bead Filter

Short Circuit Auto-Recovery

When a short circuit event happens, the EUA2034 goes to shutdown mode and tries to reactivate itself after 4ms. This auto-recovery will continue until the short circuit events is removed.

Packaging Information**SOP-16**

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.31	0.51	0.012	0.020
D	9.90		0.389	
E1	3.90		0.153	
E	5.79	6.20	0.228	0.244
e	1.27		0.050	
L	0.38	1.27	0.015	0.050