

3W/CH Stereo Filterless Class-D Audio Amplifier with 64-Step DC Volume Control, AGC and Headphone Output

DESCRIPTION

The EUA2035 is a high efficiency, 2 channel bridged-tied load (BTL), class-D audio power amplifier with headphone output. Operating from a 5V power supply, EUA2035 is capable of delivering 3W/ channel of continuous output power to a 4Ω load with 10% THD+N. The EUA2035 features an advanced 64-step DC volume control which offers a range of speaker gain from -70dB to 25dB and a range of HP gain from -95dB to 3.5dB. The AGC detects output signal clip due to the over level input signal and suppresses it automatically. Moreover the AGC can adapt the output clip caused by power supply voltage down with battery. The new filterless architecture allows the device to drive the speaker directly, without low-pass output filters, which will save system cost and PCB area.

The EUA2035 also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2035 is available in 24-pin SSOP package.

FEATURES

- Wide Supply Voltage: 2.7V to 5.5V
- Unique Modulation Scheme Reduces EMI Emission
- 3W/ch into an 4Ω Load From 5V Supply
- Efficient, Class-D Operation Eliminates Heatsinks
- 64-Step DC Volume Control
- Headphone Output Function
- Auto Gain Control
- Thermal and Short-Circuit Protection
- Integrated Click and Pop Suppression
- 24-pin SSOP Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- LCD Monitors/TVs
- All-in-One PCs
- Portable Audio
- Notebook PC

Typical Application Circuit

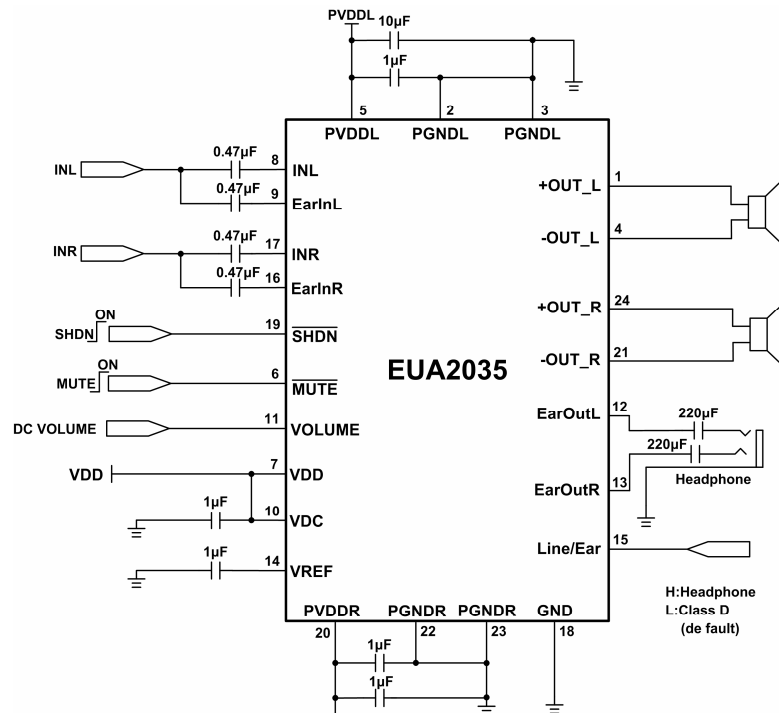


Figure1.

Pin Configurations

Package Type	Pin Configurations
SSOP-24	<p>(TOP VIEW)</p> <p>The diagram shows a top view of the SSOP-24 package with pins numbered 1 through 24. Pin 1 is +OUT_L, pin 2 is PGNDL, pin 3 is PGNDL, pin 4 is -OUT_L, pin 5 is PVDDL, pin 6 is MUTE, pin 7 is VDD, pin 8 is INL, pin 9 is EarInL, pin 10 is VDC, pin 11 is VOLUME, pin 12 is EarOutL, pin 13 is EarOutR, pin 14 is VREF, pin 15 is LINE/EAR, pin 16 is EarInR, pin 17 is INR, pin 18 is GND, pin 19 is SHDN, pin 20 is PVDDR, pin 21 is -OUT_R, pin 22 is PGNDR, pin 23 is PGNDR, and pin 24 is +OUT_R.</p>

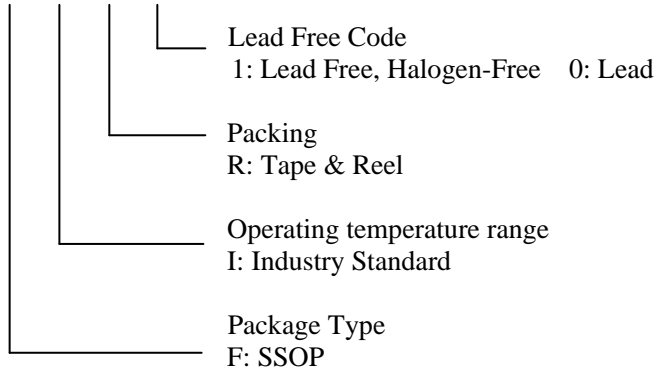
Pin Description

PIN	SSOP-24	DESCRIPTION
+OUT_L	1	Left Channel Positive Output
PGNDL	2,3	Left Channel Power GND
-OUT_L	4	Left Channel Negative Output
PVDDL	5	Left Channel Power GND
$\overline{\text{MUTE}}$	6	Mute Control Input
VDD	7	Analog VDD
INL	8	Left Channel Input
EarInL	9	Left Earphone Input
VDC	10	Analog reference for gain control section
VOLUME	11	DC volume control to set the gain of Class-D
EarOutL	12	Left Earphone Output
EarOutR	13	Right Earphone Output
VREF	14	Internal analog reference, connect a bypass capacitor from VREF to GND
LINE/EAR	15	Line/Earphone detect
EarInR	16	Right Earphone Input
INR	17	Right Channel Input
GND	18	Analog GND
$\overline{\text{SHDN}}$	19	Shutdown Control Input
PVDDR	20	Right Channel Power Supply
-OUT_R	21	Right Channel Negative Output
PGNDR	22,23	Right Channel Power GND
+OUT_R	24	Right Channel Positive Output

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2035FIR1	SSOP-24	 xxxxx EUA2035	-40 °C to +85°C

EUA2035 □ □ □ □



Block Diagram

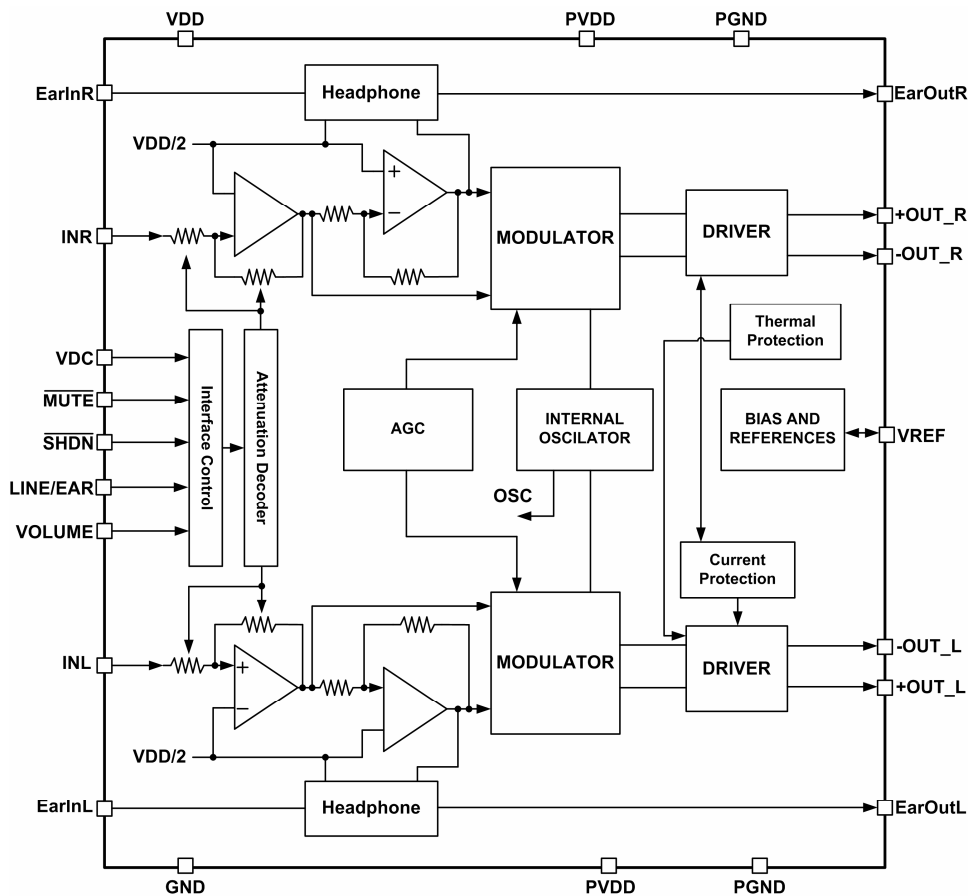


Figure2.

Absolute Maximum Ratings (1)

- Supply Voltage ----- 6V
- Input Voltage ----- -0.3 V to $V_{DD} + 0.3V$
- Junction Temperature, T_J ----- -40°C to 125°C
- Storage Temperature Rang, T_{stg} ----- -65°C to 150°C
- ESD Susceptibility ----- 2kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ----- 260°C
- Thermal Resistance
 θ_{JA} (SSOP-24) ----- 90°C/W

Recommended Operating Conditions (2)

	Min.	Max.	Unit
Supply voltage	2.7	5.5	V
Operating free-air temperature, T_A	-40	85	°C

Note (1): Stress beyond those listed under “Absolute Maximum Ratings” may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

$V_{DD}=5V$, Gain=Maximum, $R_L=8\Omega$, $T_A = +25^\circ C$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2035			Unit
			Min.	Typ.	Max.	
Class D Stage						
V_{DD}	Supply Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	No Load		15	25	mA
V_{OS}	Output Offset Voltage	No Load		10	50	mV
$R_{DS(ON)}$	Drain-Source On-State Resistacne	$I_{DS}=0.5A$	P MOSFET	0.35		Ω
			N MOSFET	0.25		
P_O	Output Power	THD+N=10%, f=1kHz	$R_L=8\Omega$	1.55	1.7	W
			$R_L=4\Omega$	2.85	3.0	
THD+N	Total Harmonic Distortion Plus Noise	$R_L=8\Omega, P_O=0.85W$	f=1kHz		0.2	%
		$R_L=4\Omega, P_O=1.75W$			0.2	
PSRR	Power Supply Ripple	Input AC-GND, f=1kHz, $V_{pp}=200mV$		40		dB
C_S	Channel Separation	$P_O=1W, f=1kHz$		-80		dB
f_{OSC}	Oscillator Frequency		250	300	350	kHz
η	Efficiency	$P_O=1.7W, f=1kHz, R_L=8\Omega$	87	90		%
		$P_O=3.0W, f=1kHz, R_L=4\Omega$	85	88		%
V_n	Noise	Input AC-GND	A-weighting		275	μV
			No A-weighting		450	
SNR	Signal Noise Ratio	F=20-20kHz, THD=1%		85		dB
Earphone Stage						
I_Q	Quiescent Current	No Load		7.5	12	mA
V_{OS}	Output Offset Voltage	No Load		2.5		V
P_O	Output Power	THD+N=1%, $R_L=32\Omega, f=1kHz$		95		mW

Electrical Characteristics (continued)

$V_{DD}=5V$, Gain=Maximum, $R_L=8\Omega$, $T_A = +25^\circ C$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2035			Unit
			Min.	Typ.	Max.	
THD+N	Total Harmonic Distortion Plus Noise	$R_L=32\Omega, P_O=10mW, f=1kHz$		0.05		%
PSRR	Power Supply Ripple Rejection	Input AC-GND, $f=1kHz, V_{pp}=200mV$		40		dB
C_S	Channel Separation	$P_O=1W, f=1kHz$		-85		dB
V_n	Noise	Input AC-GND	A-weighting	15		μV
			No A-weighting	26		
SNR	Signal Noise Ratio	$f=20-20kHz, THD=1\%$		90		dB
Control Section						
UVLO	Under Voltage Lock-out			2		V
I_{MUTE}	Mute Current	$V_{MUTE}=0V$		5	8	mA
I_{SHDN}	Shutdown Current	$V_{SHDN}=0V$		0.2	1	μA
V_{SH}	\overline{SHDN} Input High		1.2			V
V_{SL}	\overline{SHDN} Input Low				0.5	
V_{MH}	\overline{MUTE} Input High		1.2			V
V_{ML}	\overline{MUTE} Input Low				0.5	
OTP	Over Temperature Protection			165		$^\circ C$
OTH	Over Temperature Hysteresis			45		$^\circ C$

Table 1. DC Volume Control

VOLUME POSITION	INCREASING VOLUME (VOLUME PIN VOLTAGE AS A PERCENTAGE OF VDC) (%)			DECREASING VOLUME (VOLUME PIN VOLTAGE AS A PERCENTAGE OF VDC) (%)			Class D Gain (dB)	HP Gain (dB)
0	0.0	-	3.8	2.8	-	0.0	-70.0	-96.6
1	3.8	-	5.4	4.4	-	2.8	-41.6	-40.0
2	5.4	-	6.8	5.8	-	4.4	-35.1	-37.9
3	6.8	-	8.2	7.2	-	5.8	-26.9	-35.9
4	8.2	-	9.6	8.6	-	7.2	-19.4	-33.9
5	9.6	-	11.0	10.0	-	8.6	-14.5	-31.9
6	11.0	-	12.4	11.4	-	10.0	-8.5	-29.9
7	12.4	-	13.8	12.8	-	11.4	-6.0	-28.9
8	13.8	-	15.2	14.2	-	12.8	-3.6	-27.8
9	15.2	-	16.4	15.6	-	14.2	-1.1	-26.8
10	16.4	-	17.8	17.0	-	15.6	1.3	-25.8
11	17.8	-	19.2	18.4	-	17.0	2.8	-24.8
12	19.2	-	20.6	19.8	-	18.4	4.3	-23.9
13	20.6	-	22.0	21.2	-	19.8	5.3	-22.9
14	22.0	-	23.4	22.6	-	21.2	5.7	-22.1
15	23.4	-	24.8	24.0	-	22.6	6.1	-21.3
16	24.8	-	26.2	25.4	-	24.0	6.5	-20.5
17	26.2	-	27.6	26.8	-	25.4	6.9	-19.7
18	27.6	-	29.0	28.2	-	26.8	7.3	-18.9
19	29.0	-	30.4	29.6	-	28.2	7.7	-18.1
20	30.4	-	31.6	31.0	-	29.6	8.1	-17.3
21	31.6	-	33.2	32.4	-	31.0	8.6	-16.5
22	33.2	-	34.6	33.8	-	32.4	9.0	-15.8
23	34.6	-	36.0	35.2	-	33.8	9.4	-15.1
24	36.0	-	37.6	36.6	-	35.2	9.8	-14.4
25	37.6	-	39.0	38.0	-	36.6	10.2	-13.7
26	39.0	-	40.4	39.4	-	38.0	10.6	-13.1
27	40.4	-	41.8	40.8	-	39.4	11.0	-12.4
28	41.8	-	43.2	42.2	-	40.8	11.4	-11.7
29	43.2	-	44.6	43.6	-	42.2	11.8	-11.0
30	44.6	-	46.0	45.0	-	43.6	12.2	-10.4
31	46.0	-	47.4	46.4	-	45.0	12.6	-9.8
32	47.4	-	48.8	47.8	-	46.4	13.0	-9.2
33	48.8	-	50.2	49.2	-	47.8	13.4	-8.6
34	50.2	-	51.6	50.6	-	49.2	13.8	-8.0
35	51.6	-	53.0	52.0	-	50.6	14.2	-7.4
36	53.0	-	54.4	53.4	-	52.0	14.6	-6.8
37	54.4	-	55.8	54.8	-	53.4	15.0	-6.2
38	55.8	-	57.2	56.2	-	54.8	15.4	-5.7
39	57.2	-	58.6	57.4	-	56.2	15.8	-5.2
40	58.6	-	60.0	59.0	-	57.4	16.2	-4.7
41	60.0	-	61.4	60.4	-	59.0	16.6	-4.2
42	61.4	-	62.8	61.8	-	60.4	17.0	-3.7
43	62.8	-	64.2	63.2	-	61.8	17.4	-3.2
44	64.2	-	65.6	64.6	-	63.2	17.8	-2.7
45	65.6	-	67.0	66.0	-	64.6	18.2	-2.2
46	67.0	-	68.4	67.4	-	66.0	18.6	-1.8
47	68.4	-	69.8	68.8	-	67.4	19.0	-1.4
48	69.8	-	71.2	70.2	-	68.8	19.4	-1.0
49	71.2	-	72.6	71.6	-	70.2	19.8	-0.6
50	72.6	-	74.0	73.0	-	71.6	20.2	-0.2
51	74.0	-	75.4	74.4	-	73.0	20.6	0.2
52	75.4	-	76.8	75.8	-	74.4	21.0	0.6
53	76.8	-	78.2	77.2	-	75.8	21.4	0.9
54	78.2	-	79.6	78.6	-	77.2	21.8	1.2
55	79.6	-	81.0	80.0	-	78.6	22.2	1.5
56	81.0	-	82.4	81.4	-	80.0	22.6	1.8
57	82.4	-	83.8	82.8	-	81.4	23.0	2.1
58	83.8	-	85.2	84.2	-	82.8	23.4	2.4
59	85.2	-	86.6	85.6	-	84.2	23.8	2.7
60	86.6	-	88.0	87.0	-	85.6	24.2	2.9
61	88.0	-	89.4	88.4	-	87.0	24.6	3.1
62	89.4	-	90.8	89.8	-	88.4	25.0	3.3
63	90.8	-	100.0	100.0	-	89.8	25.4	3.5

Typical Characteristics

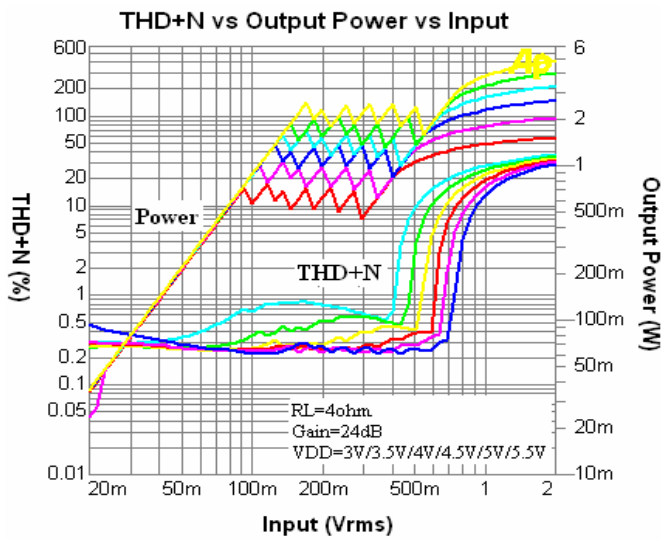


Figure3.

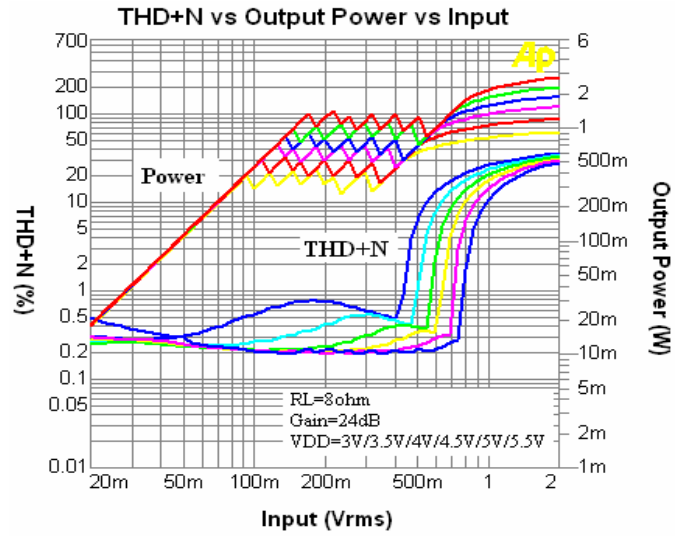


Figure4.

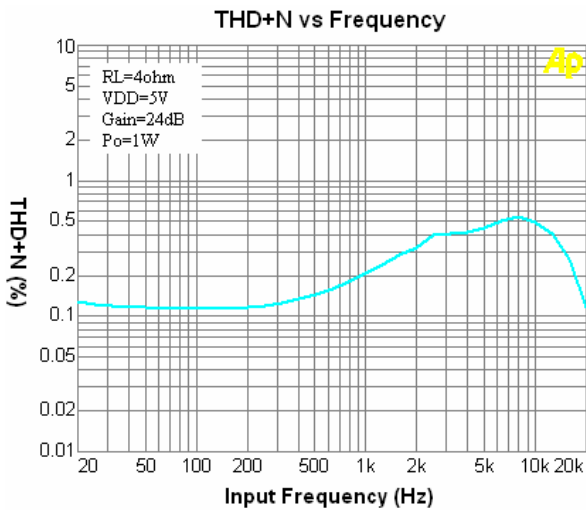


Figure5.

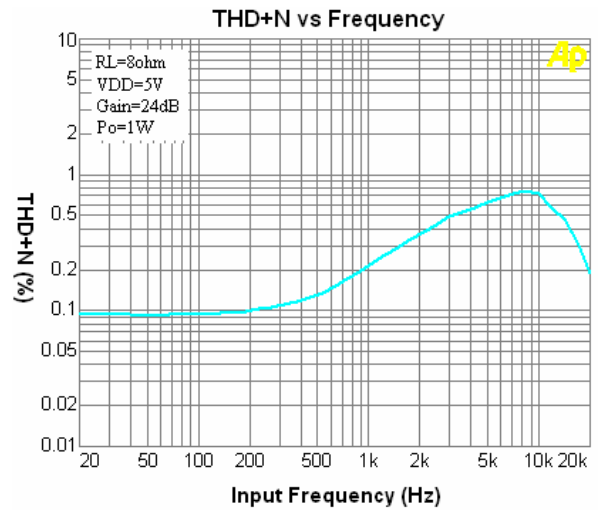


Figure6

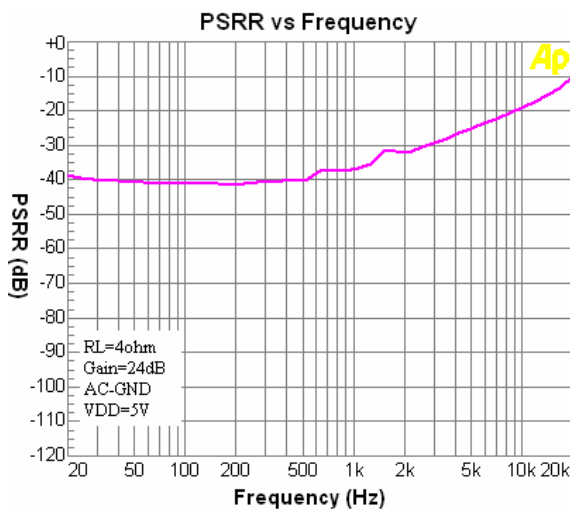


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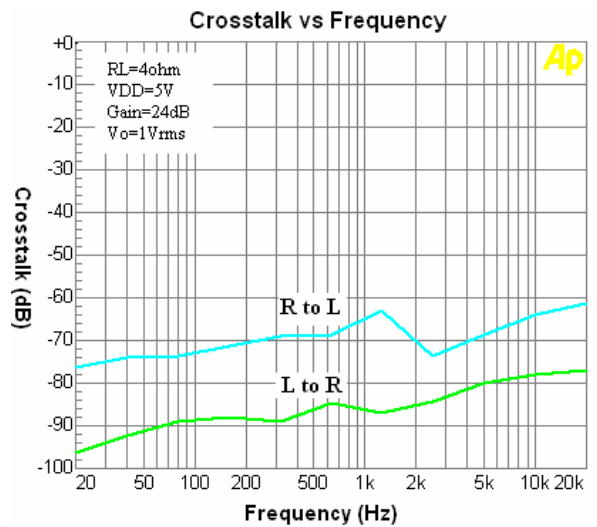


Figure8.

Typical Characteristics (continued)

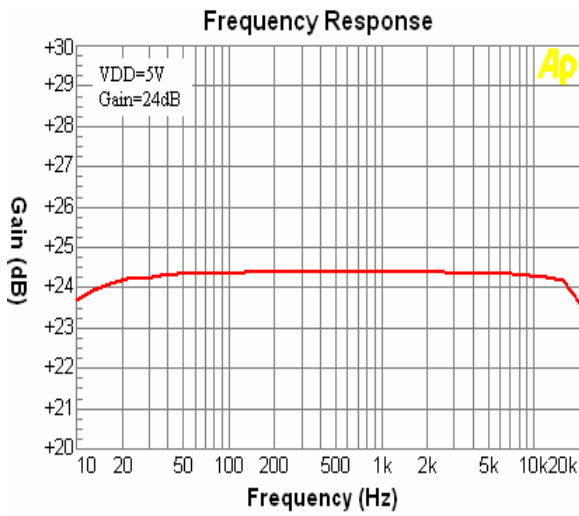


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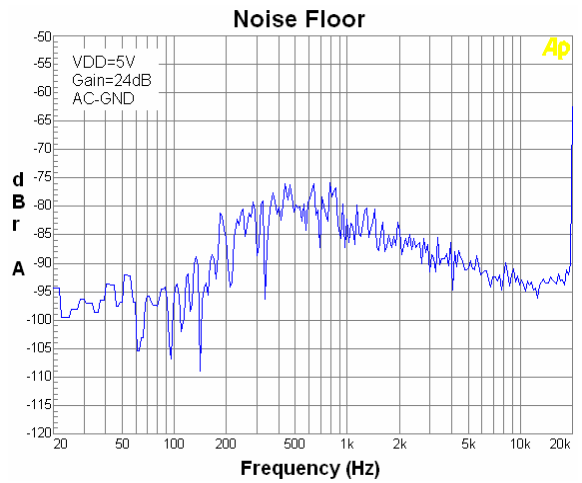


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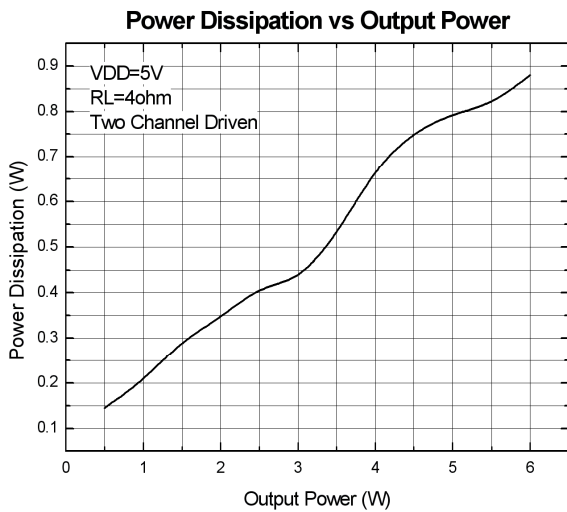


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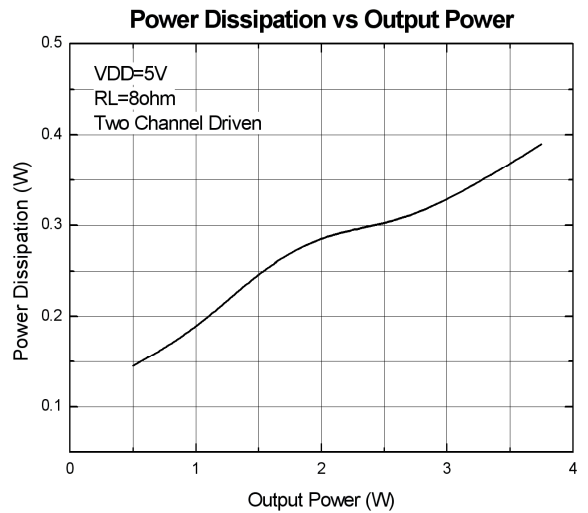


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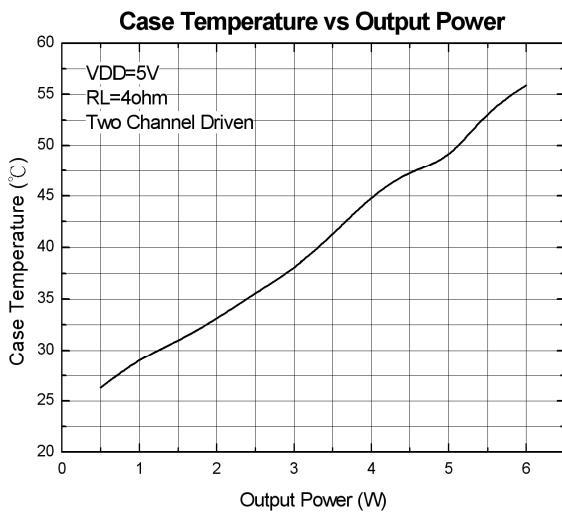


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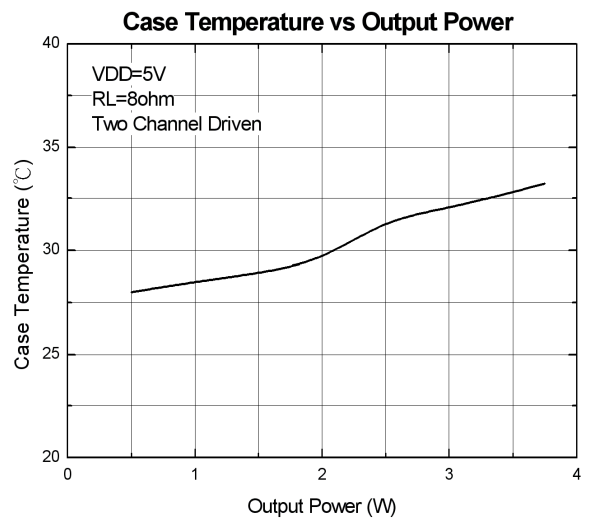


Figure14.

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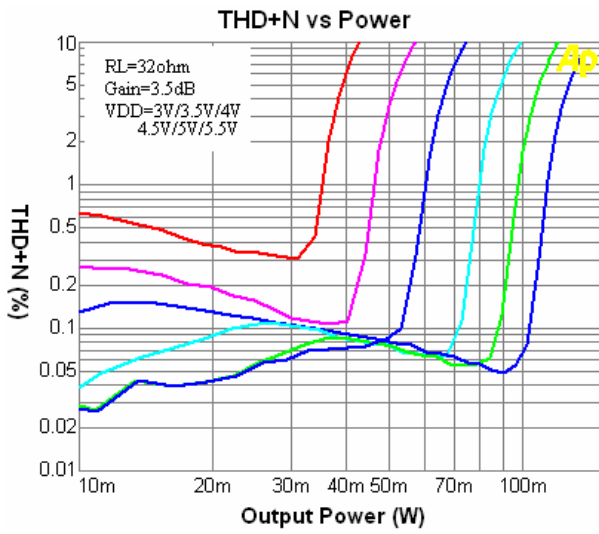


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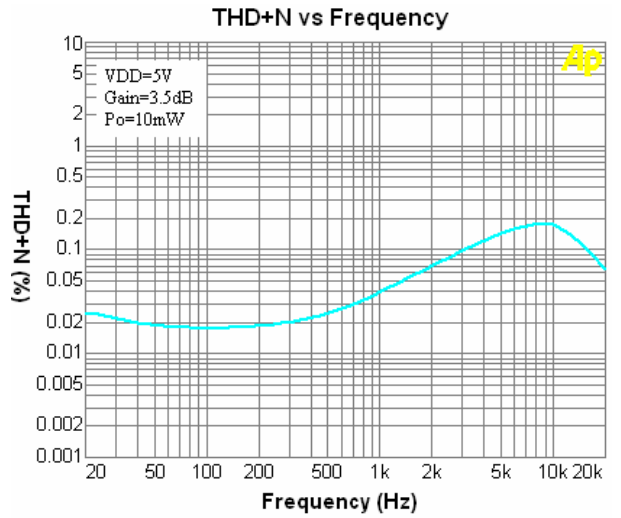


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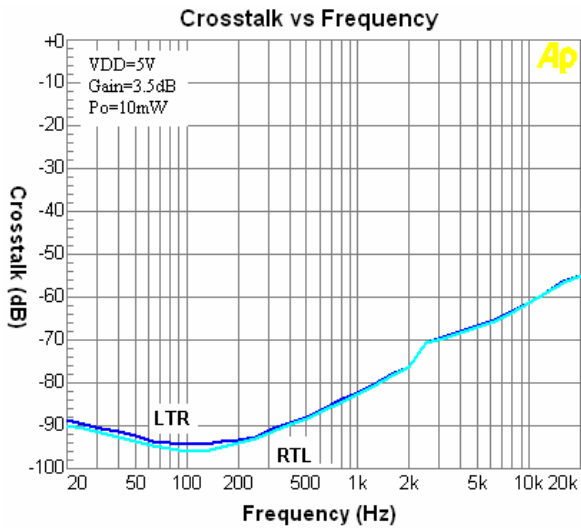


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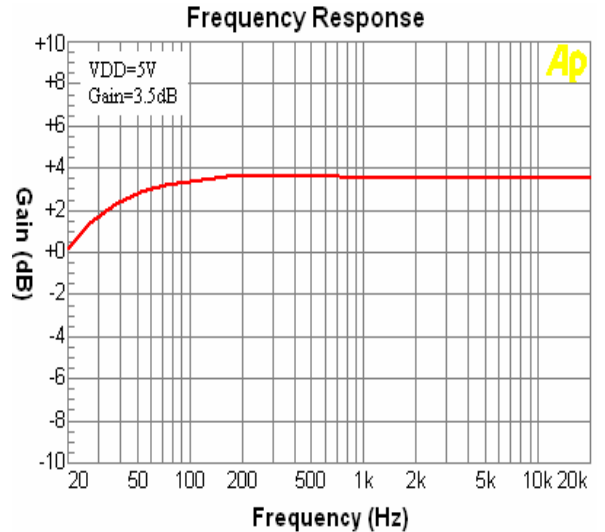


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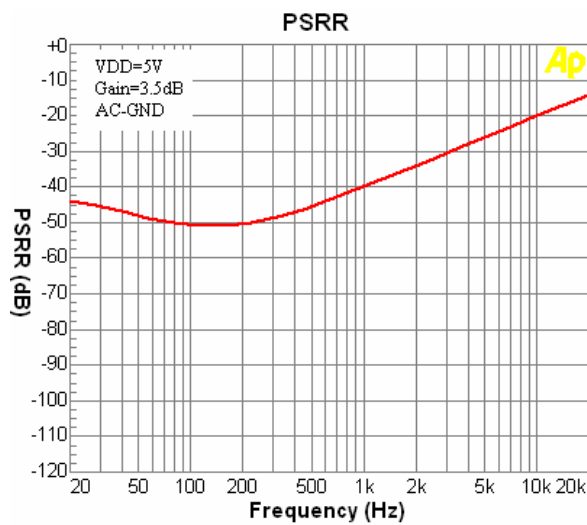


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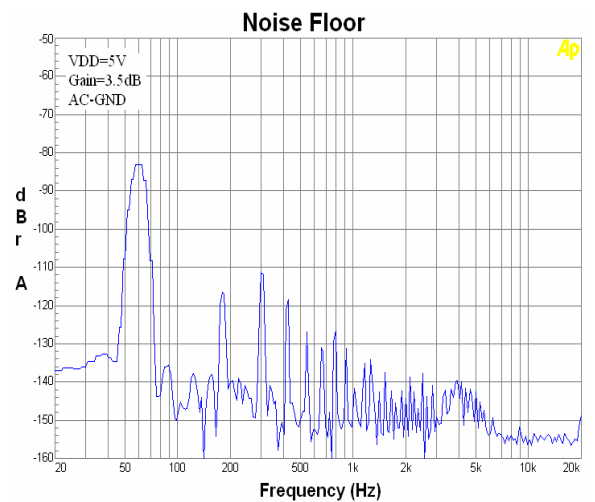


Figure20.

Typical Characteristics (continued)

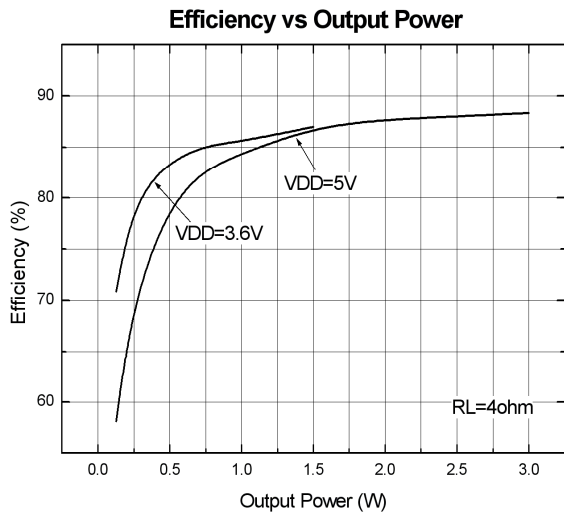


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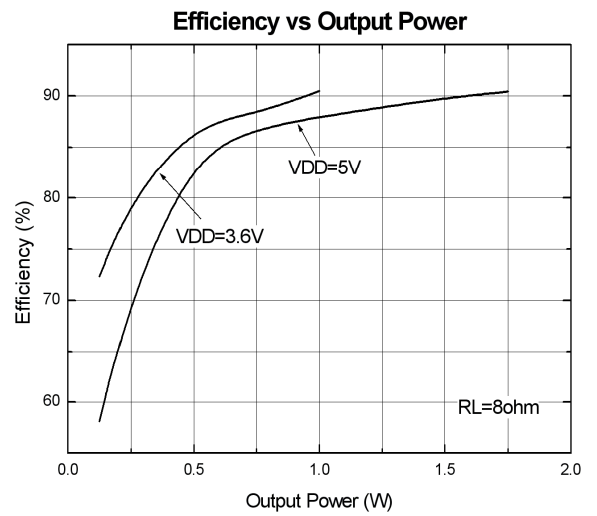


Figure22.

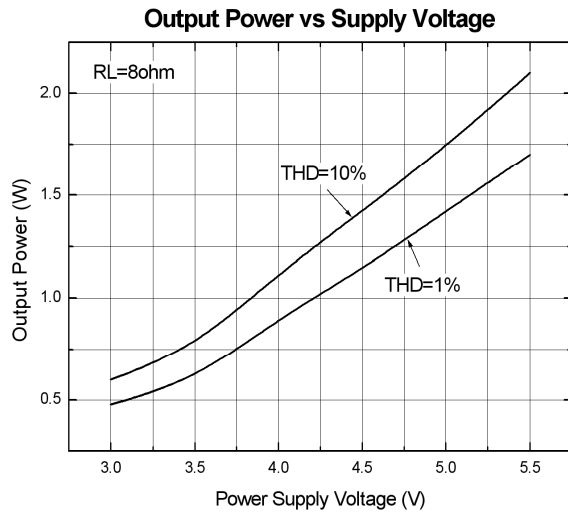


Figure23.

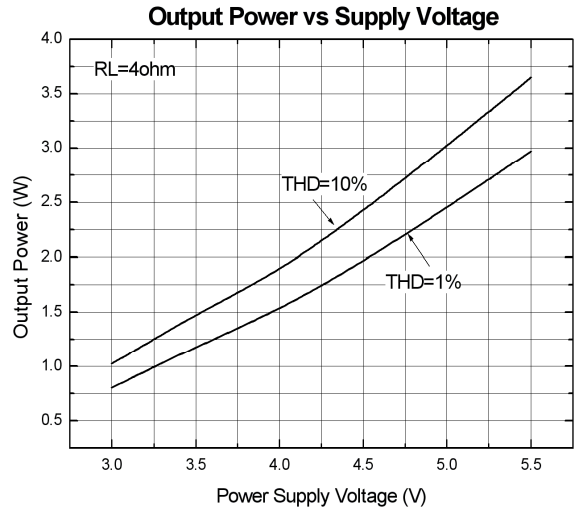


Figure24.

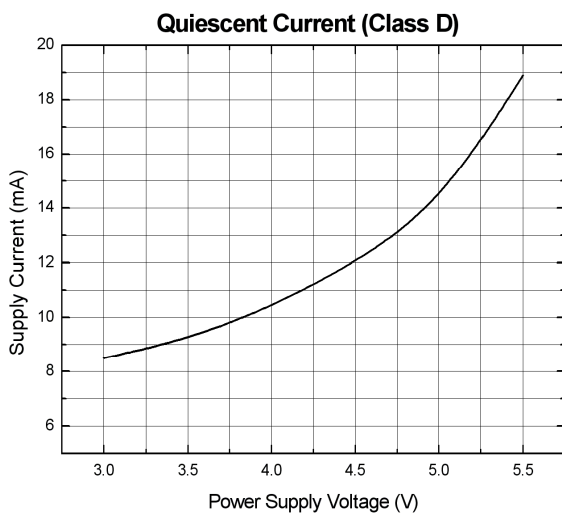


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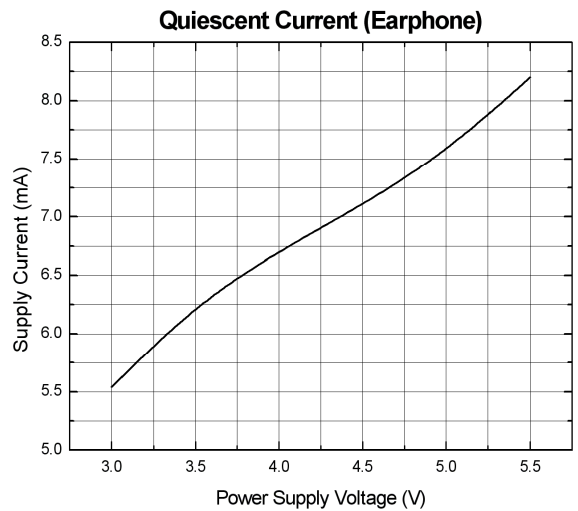


Figure26.

Typical Characteristics (continued)

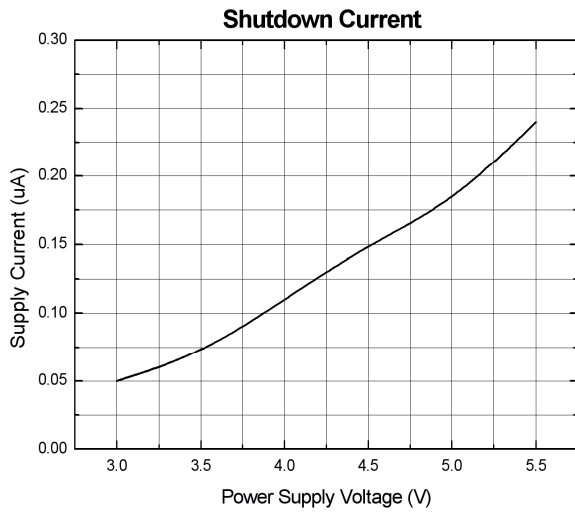


Figure27.

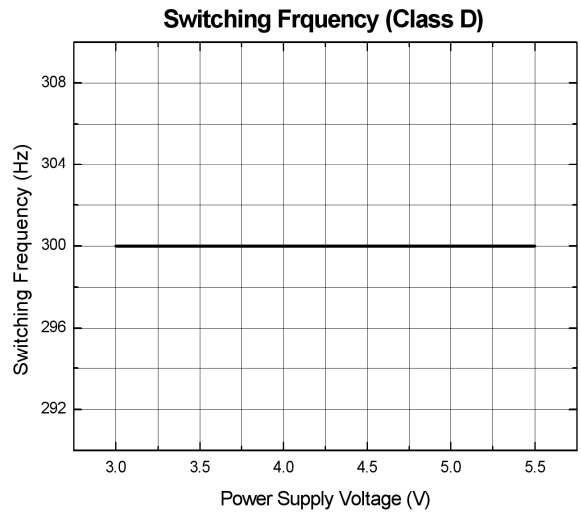


Figure28.

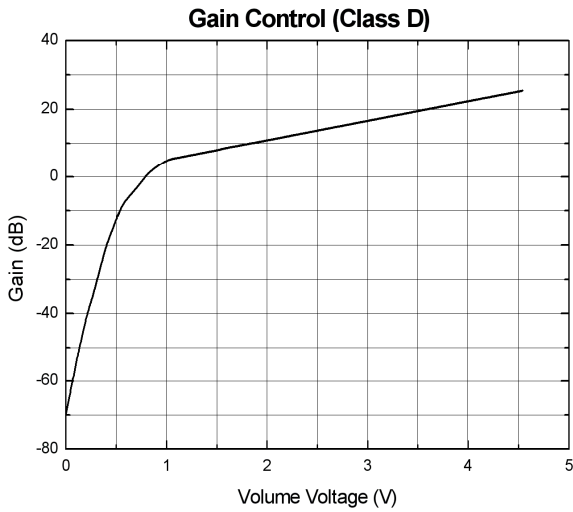


Figure29.

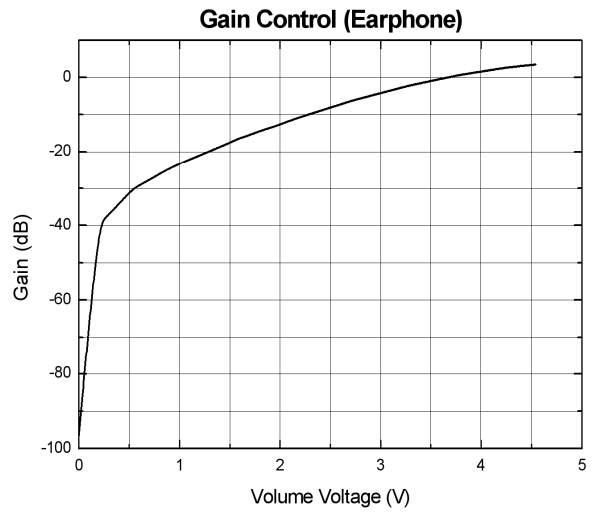


Figure30.

Application Information

Volume Control Operation

The VOLUME terminal controls the internal amplifier gain. This pin is controlled with a dc voltage, which should not exceed VDC. Table 1 lists the gain as determined by the voltage on the VOLUME pin in reference to the voltage on VDC.

If using a resistor divider to fix the gain of the amplifier, the VDC terminal can be directly connected to VDD and a resistor divider can be connected across VDC and AGND. For fixed gain, calculate the resistor divider values necessary to center the voltage between the two percentage points given in the first column of Table 1.

If using a DAC to control the class-D gain, VDC and AGND should be connected to the reference voltage for the DAC and the GND terminal of the DAC, respectively. For the DAC application, VDD would be left unconnected to VDC. The reference voltage of the DAC provides the reference to the internal gain circuitry through the VDC input and any fluctuations in the DAC output voltage will not affect the EUA2035 gain. The percentages in the first column of Table 1 should be used for setting the voltages of the DAC when the voltage on the VOLUME terminal is increased. The percentages in the second column should be used for the DAC voltages when decreasing the voltage on the VOLUME terminal. Two lookup tables should be used in software to control the gain based on an increase or decrease in the desired system volume.

If using an analog potentiometer to control the gain, it should be connected between VDC and AGND. VDC can be connected to VDD or an external voltage source, if desired. The 2nd and 3rd column in Table 1 should be used to determine the point at which the gain changes depending on the direction that the potentiometer is turned. If the voltage on the center tap of the potentiometer is increasing, the 2nd column in Table 1 should be referenced to determine the trip points. If the voltage is decreasing, the trip points in the 3rd column should be referenced.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 31.

The timing of the volume control circuitry is controlled by an internal 30-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every clock cycle (nominally 32 ms) to the next step until the final desired gain is reached. For example, if the EUA2035 is currently in the 0 dB gain step and the VOLUME pin is adjusted for maximum gain at +25 dB,

the time required for the gain to reach +25 dB is 54 steps x 32ms/step = 1.728 seconds.

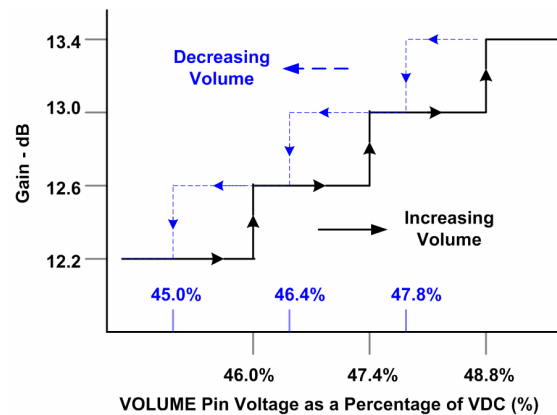


Figure 31. DC Volume Control Operation

FADE Operation

During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SHDN}}$ terminal), the volume is smoothly ramped up from the mute state, -70 dB, to the desired volume setting determined by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the $\overline{\text{SHDN}}$ terminal.

Auto Gain Control Function

The AGC works by detecting the audio input envelope. The gain changes depending on the amplitude, the power supply level, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases to suppress the clipped output signal. The gain step size for the AGC is 2dB. The maximum attenuation is -12dB (preset gain=24dB). The attack time is 24ms and the released time is 1.5Sec per step.

$\overline{\text{MUTE}}$ Operation

The $\overline{\text{MUTE}}$ pin is an input for controlling the output state of the EUA2035. A logic low on this pin disables the outputs, and a logic high on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade. Quiescent current is listed in the electrical characteristic table. The $\overline{\text{MUTE}}$ pin can't be left floating.

$\overline{\text{SHDN}}$ Operation

In order to reduce power consumption while not in use, the EUA2035 contains shutdown circuitry to turn off the amplifier's bias circuitry. The amplifier is turned off when logic low is placed on the $\overline{\text{SHDN}}$ pin. By switching the $\overline{\text{SHDN}}$ pin connected to GND, the EUA2035 supply current draw will be minimized in idle mode. The $\overline{\text{SHDN}}$ pin can't be left floating.

For the best power on/off pop performance, the amplifier should be placed in the Mute mode prior to turning on/off the power supply.

Power Supply Decoupling

The EUA2035 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Power supply decoupling affects low frequency response on the power supply leads. For higher frequency response. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0 μ F, placed as close as possible to the device V_{DD} terminal works best. For filtering lower-frequency noise signals, a large capacitor of 10 μ F (ceramic) or greater placed near the audio power amplifier is recommended.

Input Capacitor (C_i)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. In this case, input capacitor (C_i) and input resistance (R_i) of the amplifier form a high-pass filter with the corner frequency determined equation below,

$$f_C = \frac{1}{2\pi R_i C_i}$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_i . A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Analog Reference Bypass Capacitor (C_{BYP})

The Analog Reference Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

A ceramic bypass capacitor (C_{BYP}) of 0.47 μ F to 1.0 μ F is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Under Voltage Lock-Out (UVLO)

The EUA2035 incorporates circuitry designed to detect when the supply voltage is low. when the supply voltage drops to 1.9V or below, the eua2035 outputs are disable, and the device comes out of this state and starts to normal functional once $V_{DD} > 2.0V$.

Short Circuit Protection (SCP)

The EUA2035 has short circuit protection circuitry on the outputs that prevents the device from damage when output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disable immediately. If the short was removed, the device activates again.

Over Temperature Protection

Thermal protection on the EUA2035 prevents the device from damage when the internal die temperature exceeds 165°C. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. This large hysteresis will prevent motor boating sound well. The device begins normal operation at this point without external system interaction.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000 μ F at power supply terminal for power line coupling if the traces from amplifier to speakers are short (<20CM).

Most applications require a ferrite bead filter as shown at Figure 32. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at low frequencies.

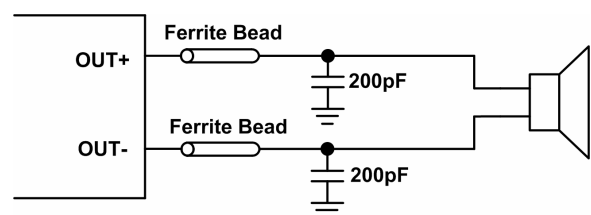
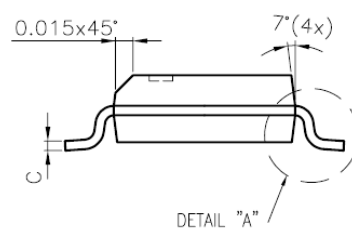
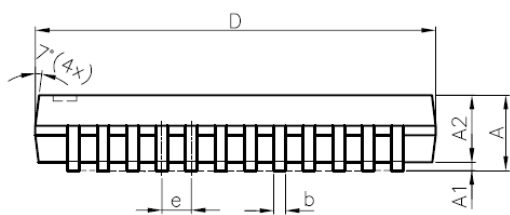
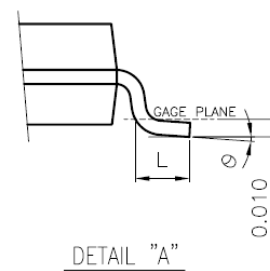
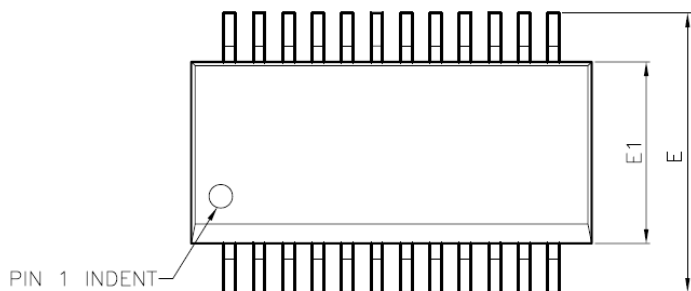


Figure 32.

Packaging Information

SSOP-24



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.37	1.45	1.52	0.054	0.057	0.060
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.18	0.20	0.25	0.007	0.008	0.010
D	8.56	8.66	8.74	0.337	0.341	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	0.64 BSC			0.025 BSC		
L	0.41	0.64	1.27	0.016	0.025	0.050
θ	0°	—	8°	0°	—	8°