

2.8W/CH Stereo Filterless Class-D Audio Amplifier with 64-Step DC Volume Control, AGC and Headphone Output

DESCRIPTION

The EUA2075 is a high efficiency, 2 channel bridged-tied load (BTL), class-D audio power amplifier with headphone output. Operating from a 5V power supply, EUA2075 is capable of delivering 2.8W/channel of continuous output power to a 4Ω load with 10% THD+N. The EUA2075 features an advanced 64-step DC volume control which offers a range of speaker gain from -70dB to 20dB and a range of HP gain from -80dB to 3.5dB. The AGC detects output signal clip due to the over level input signal and suppresses it automatically. Moreover the AGC can adapt the output clip caused by power supply voltage down with battery. The new filter-less architecture allows the device to drive the speaker directly, without low-pass output filters, which will save system cost and PCB area.

The EUA2075 also features short-circuit and thermal protection preventing the device from being damaged during a fault condition. The EUA2075 is available in 24-pin SOP and 20-pin 4x4 TQFN package.

FEATURES

- Wide Supply Voltage: 2.7V to 5.5V
- Unique Modulation Scheme Reduces EMI Emission
- 2.8W/ch into an 4Ω Load From 5V Supply
- 64-Step DC Volume Control
- Headphone Output Function
- Auto Gain Control
- Thermal and Short-Circuit Protection
- Integrated Click and Pop Suppression
- Available in SOP-24 and TQFN-20 Packages
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- LCD Monitors/TVs
- All-in-One PCs
- Portable Audio
- Notebook PC

Typical Application Circuit

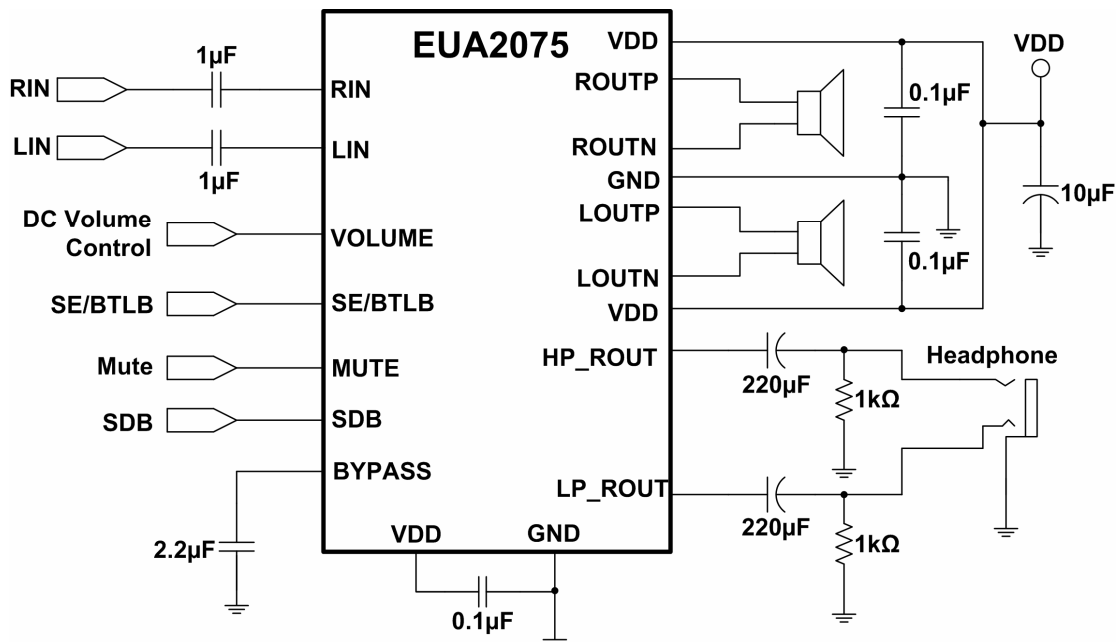


Figure1.


Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
SOP-24	<p>(TOP VIEW)</p> <p> SDB 1 BYPASS 2 RIN 3 GND 4 GND 5 LIN 6 VOLUME 7 MUTE 8 SE/BTLB 9 AGC 10 UVP 11 VDD 12 24 ROUTN 23 VDD 22 ROU TP 21 GND 20 GND 19 LOU TP 18 VDD 17 LOU TN 16 NC 15 HP_ ROUT 14 NC 13 HP_ LOU T </p>	TQFN-20	<p>(TOP VIEW)</p> <p> 20 VDD 19 ROU TP 18 GND 17 LOU TP 16 VDD 15 LOU TN 14 HP_ LOU T 13 VDD 12 UVP 11 AGC 10 SE/BTLB 9 MUTE 8 VOLUME 7 LIN 6 GND 5 RIN 4 BYPASS 3 SDB 2 HP_ ROUT 1 ROUTN </p>

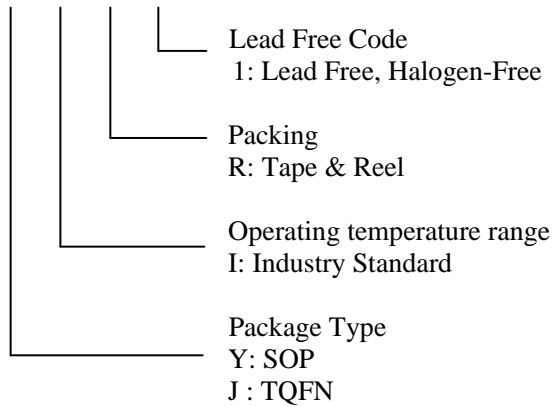
Pin Description

PIN	SOP-24	TQFN-20	DESCRIPTION
SDB	1	3	Shutdown mode control input. Pulling low the voltage on this pin shuts off the IC.
BYPASS	2	4	Bias voltage for power amplifier.
RIN	3	5	Input of right channel power amplifier.
GND	4,5,20,21	6,18	Ground.
LIN	6	7	Input of left channel power amplifier.
VOLUME	7	8	Gain setting input. Connect to GND to set max gain=20dB.
MUTE	8	9	Mute control signal input, hold low for normal operation, hold high to mute.
SE/BTLB	9	10	Output mode control input, high for SE output mode and low for BTL mode.
NC	14,16	--	No connection.
AGC	10	11	VDD~0.45VDD or AGC floating, disable this function.
UVP	11	12	Under voltage protection input. Floating or pull "H" disable this function.
VDD	12,18,23	13,16,20	Power.
HP_LOUT	13	14	Headphone output of left channel power amplifier.
HP_ROUT	15	2	Headphone output of right channel power amplifier.
LOUTN	17	15	Negative output of left channel power amplifier.
LOUTP	19	17	Positive output of left channel power amplifier.
ROU TP	22	19	Positive output of right channel power amplifier.
ROUTN	24	1	Negative output of right channel power amplifier.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2075YIR1	SOP-24	 xxxxx EUA2075	-40 °C to +85°C
EUA2075JIR1	TQFN-20	xxxxx A2075	-40 °C to +85°C

EUA2075 □ □ □ □



Block Diagram

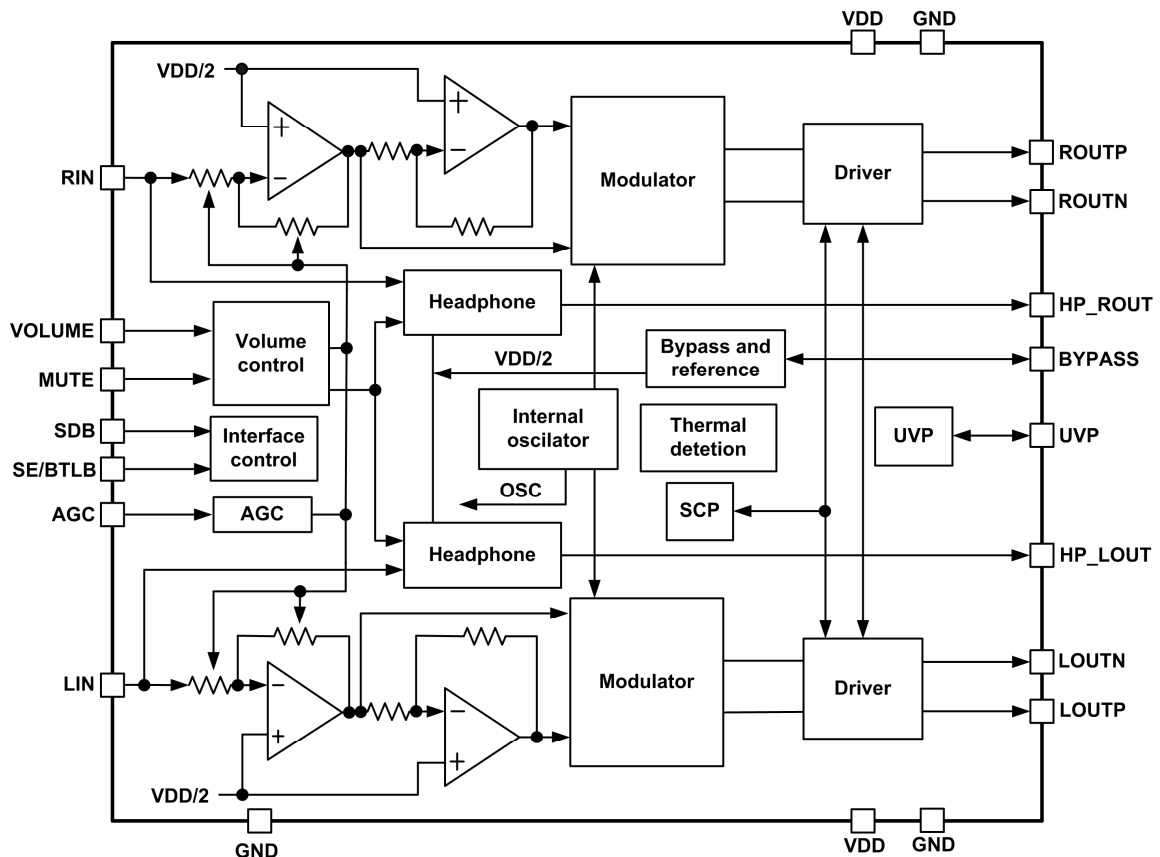


Figure2.

Absolute Maximum Ratings (1)

▪ Supply Voltage	0.3 V to 6V
▪ Input Voltage	-0.3 V to $V_{DD} + 0.3V$
▪ Junction Temperature, T_J	-40°C to 125°C
▪ Storage Temperature Rang, T_{stg}	-65°C to 150°C
▪ ESD Susceptibility	2kV
▪ Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
▪ Thermal Resistance	
θ_{JA} (SOP-24)	65°C/W
θ_{JA} (TQFN-20)	45°C/W

Recommended Operating Conditions (2)

	Min.	Max.	Unit
Supply voltage	2.7	5.5	V
Operating free-air temperature, T_A	-40	85	°C

Note (1): Stress beyond those listed under “Absolute Maximum Ratings” may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

$V_{DD}=5V$, Gain=Maximum, $R_L=4\Omega$, $T_A = +25^\circ C$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2075			Unit
			Min.	Typ.	Max.	
BTL Mode						
V_{DD}	Supply Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	$V_{MUTE}=0V$, $V_{SDB}=5V$, No Load		6.5	15	mA
I_{MUTE}	Mute Current	$V_{MUTE}=5V$, $V_{SDB}=5V$, No Load		3.5	6	mA
I_{SD}	Shutdown Current	$V_{MUTE}=0V$, $V_{SDB}=0V$, No Load			1	μA
$ V_{OS} $	Output Offset Voltage	No Load		10	50	mV
$R_{DS(on)}$	Drain-Source On-State Resistance	$I_{DS}=0.5A$	P MOSFET		350	m Ω
			N MOSFET		250	
P_O	Output Power	THD+N=10%, f=1kHz	$R_L=4\Omega$		2.8	W
			$R_L=8\Omega$		1.7	
THD+N	Total Harmonic Distortion Plus Noise	f=1kHz	$R_L=4\Omega, P_O=1.6W$		0.2	%
			$R_L=8\Omega, P_O=0.8W$		0.2	
PSRR	Power Supply Ripple Rejection	Input AC-GND, f=1kHz, $V_{pp}=200mV$		-60		dB
C_S	Channel Separation	$P_O=1W$, f=1kHz		-80		dB
f_{OSC}	Oscillator Frequency		400	500	600	kHz
V_n	Noise	A-weighting		70	110	μV_{rms}
SNR	Signal Noise Ratio	F=20-20kHz, THD=1%		-88		dB
SE Mode						
I_Q	Quiescent Current	$V_{MUTE}=0V$, $V_{SDB}=5V$, No Load		3.5	6	mA
$ V_{OS} $	Output Offset Voltage	No Load		2.5		V

Electrical Characteristics (continued)

$V_{DD}=5V$, Gain=Maximum, $R_L=4\Omega$, $T_A = +25^\circ C$ (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2075			Unit	
			Min.	Typ.	Max.		
SE Mode							
P_O	Output Power	THD+N=1%	$R_L= 32\Omega$		60	mW	
		THD+N=10%	$R_L= 32\Omega$		75		
THD+N	Total Harmonic Distortion Plus Noise	f=1kHz	$R_L= 32\Omega$ $P_O=10mW$		0.05	%	
PSRR	Power Supply Ripple Rejection	Input AC-GND, f=1kHz, $V_{pp}=200mV$			-60	dB	
C_S	Channel Separation	$P_O=$, f=1kHz			-85	dB	
V_n	Noise	Input AC-GND, A-weighting			20	μV_{rms}	
SNR	Signal Noise Ratio	F=20-20kHz, THD=1%			-90	dB	
Control Section							
V_{IH}	High Level Threshold Voltage	SDB, MUTE, SE/BTLB			2	V	
V_{IL}	Low Level Threshold Voltage	SDB, MUTE, SE/BTLB				0.8	V
OTP	Over Temperature Protection				165	$^\circ C$	
OTH	Over Temperature Hysteresis				30	$^\circ C$	

Table 1. DC Volume Control

Step	Decreasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	Increasing Volume (Volume Pin Voltage As A Percentage of VDD) (%)	BTL Gain (dB)	SE Gain (dB)
1	0.0 - 3.4	2.4 - 0.0	20.0	3.5
2	3.4 - 4.8	3.8 - 2.4	19.6	3.2
3	4.8 - 6.2	5.2 - 3.8	19.2	2.9
4	6.2 - 7.6	6.6 - 5.2	18.8	2.6
5	7.6 - 9.0	8.0 - 6.6	18.4	2.3
6	9.0 - 10.4	9.4 - 8.0	18.0	2.0
7	10.4 - 11.8	10.8 - 9.4	17.6	1.7
8	11.8 - 13.2	12.2 - 10.8	17.2	1.4
9	13.2 - 14.6	13.6 - 12.2	16.8	1.1
10	14.6 - 16.0	15.0 - 13.6	16.4	0.8
11	16.0 - 17.4	16.4 - 15.0	16.0	0.5
12	17.4 - 18.8	17.8 - 16.4	15.6	0.2
13	18.8 - 20.2	19.2 - 17.8	15.2	-0.2
14	20.2 - 21.6	20.6 - 19.2	14.8	-0.5
15	21.6 - 23.0	22.0 - 20.6	14.4	-0.8
16	23.0 - 24.4	23.4 - 22.0	14.0	-1.2
17	24.4 - 25.8	24.8 - 23.4	13.6	-1.5
18	25.8 - 27.2	26.2 - 24.8	13.2	-1.8
19	27.2 - 28.6	27.6 - 26.2	12.8	-2.2
20	28.6 - 30.0	29.0 - 27.6	12.4	-2.5
21	30.0 - 31.4	30.4 - 29.0	12.0	-2.9
22	31.4 - 32.8	31.8 - 30.4	11.6	-3.2
23	32.8 - 34.2	33.2 - 31.8	11.2	-3.6
24	34.2 - 35.6	34.6 - 33.2	10.8	-3.9
25	35.6 - 37.0	36.0 - 34.6	10.4	-4.3
26	37.0 - 38.4	37.4 - 36.0	10.0	-4.6
27	38.4 - 39.8	38.8 - 37.4	9.6	-5.0
28	39.8 - 41.2	40.2 - 38.8	9.2	-5.4
29	41.2 - 42.6	41.6 - 40.2	8.8	-5.7
30	42.6 - 44.0	43.0 - 41.6	8.4	-6.1
31	44.0 - 45.4	44.4 - 43.0	8.0	-6.4
32	45.4 - 46.8	45.8 - 44.4	7.6	-6.8
33	46.8 - 48.2	47.2 - 45.8	7.2	-7.2
34	48.2 - 49.6	48.6 - 47.2	6.8	-7.5
35	49.6 - 51.0	50.0 - 48.6	6.4	-7.9
36	51.0 - 52.4	51.4 - 50.0	6.0	-8.3
37	52.4 - 53.8	52.8 - 51.4	5.6	-8.6
38	53.8 - 55.2	54.2 - 52.8	5.2	-9.0
39	55.2 - 56.6	55.6 - 54.2	4.8	-9.4
40	56.6 - 58.0	57.0 - 55.6	4.4	-9.8
41	58.0 - 59.4	58.4 - 57.0	4.0	-10.1
42	59.4 - 60.8	59.8 - 58.4	3.6	-10.5
43	60.8 - 62.2	61.2 - 59.8	3.2	-10.9
44	62.2 - 63.6	62.6 - 61.2	2.8	-11.3
45	63.6 - 65.0	64.0 - 62.6	2.4	-11.6
46	65.0 - 66.4	65.4 - 64.0	2.0	-12.0
47	66.4 - 67.8	66.8 - 65.4	1.6	-12.4
48	67.8 - 69.2	68.2 - 66.8	1.2	-12.8
49	69.2 - 70.6	69.6 - 68.2	0.8	-13.1
50	70.6 - 72.0	71.0 - 69.6	0.4	-13.5
51	72.0 - 73.4	72.4 - 71.0	0.0	-13.9
52	73.4 - 74.8	73.8 - 72.4	-1.0	-14.9
53	74.8 - 76.2	75.2 - 73.8	-2.0	-15.8
54	76.2 - 77.6	76.6 - 75.2	-3.0	-16.8
55	77.6 - 79.0	78.0 - 76.6	-5.0	-18.8
56	79.0 - 80.4	79.4 - 78.0	-7.0	-20.7
57	80.4 - 81.8	80.8 - 79.4	-9.0	-22.7
58	81.8 - 83.2	82.2 - 80.8	-11.0	-24.7
59	83.2 - 84.6	83.6 - 82.2	-17.0	-30.7
60	84.6 - 86.0	85.0 - 83.6	-23.0	-36.9
61	86.0 - 87.4	86.4 - 85.0	-29.0	-43.0
62	87.4 - 88.8	87.8 - 86.4	-35.0	-49.3
63	88.8 - 90.2	89.2 - 87.8	-41.0	-55.3
64	90.2 - 100.0	100.0 - 89.2	-70.0	-80

Typical Characteristics

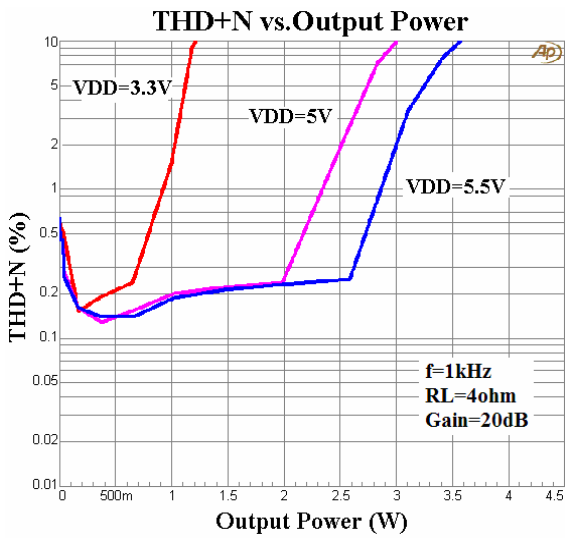


Figure3.

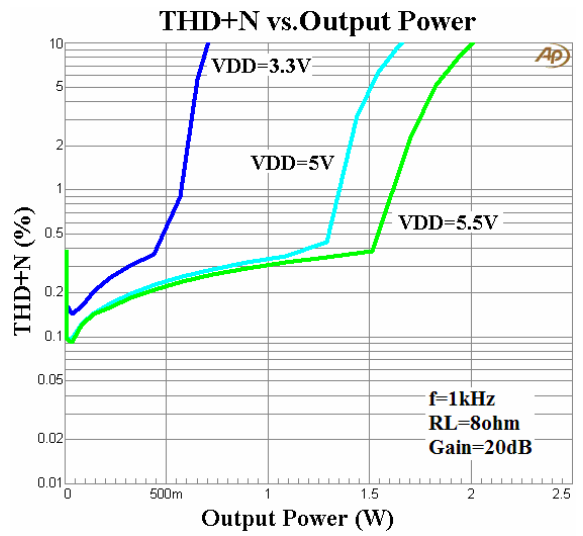


Figure4.

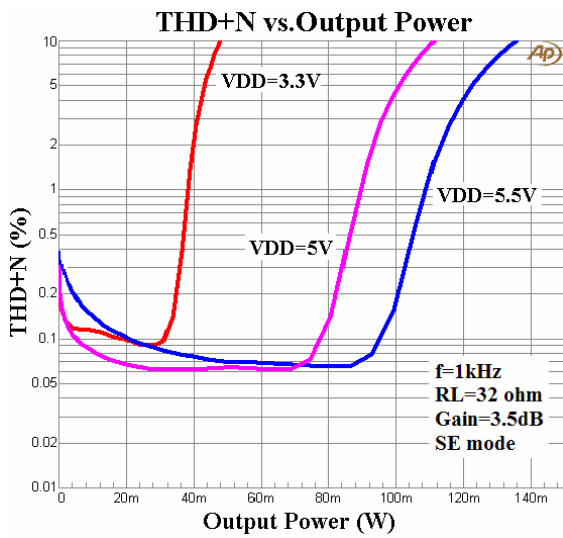


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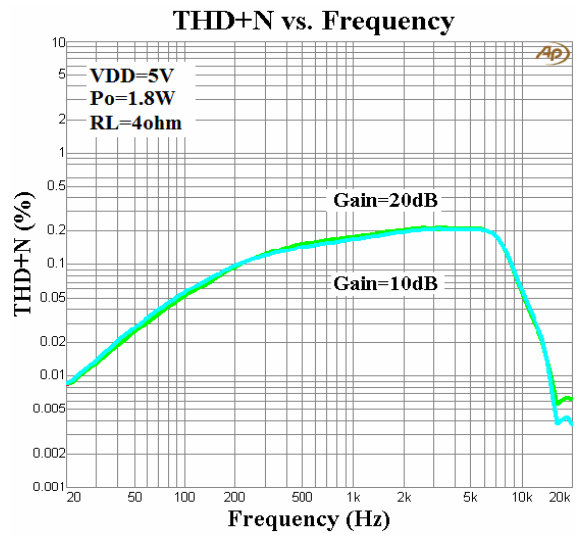


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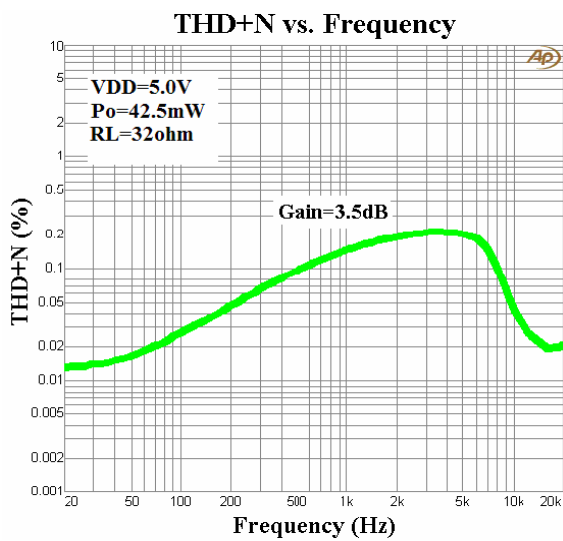


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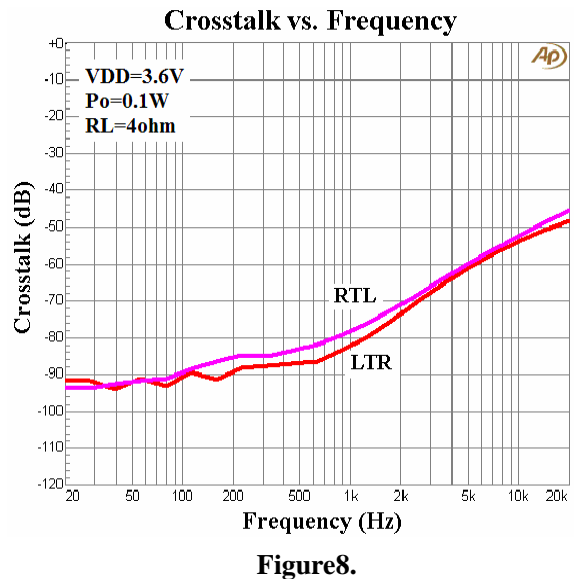
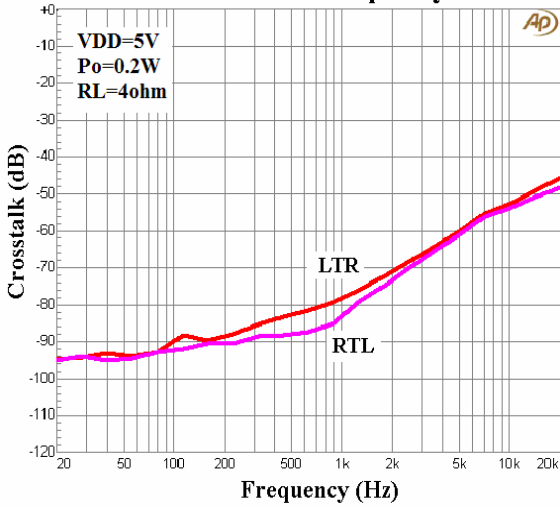


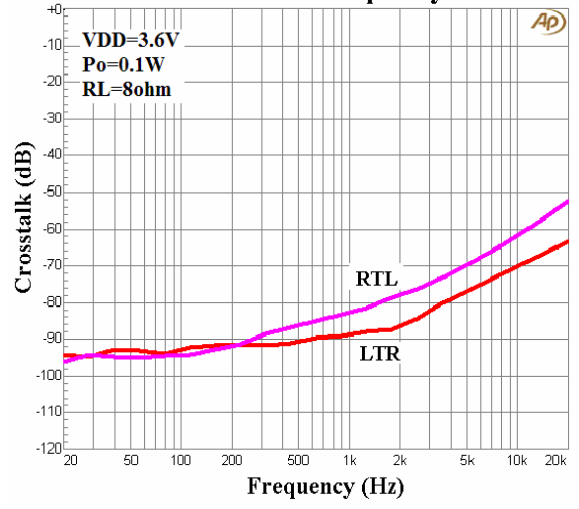
Figure8.

Typical Characteristics (continued)

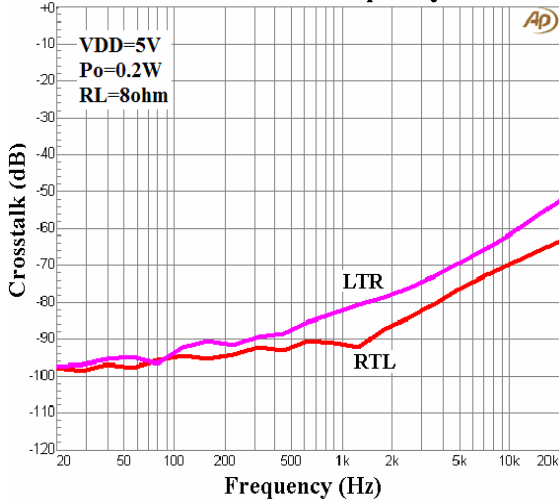
Crosstalk vs. Frequency



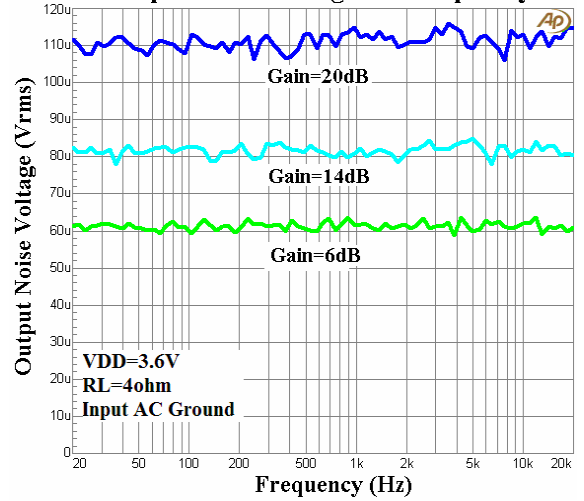
Crosstalk vs. Frequency



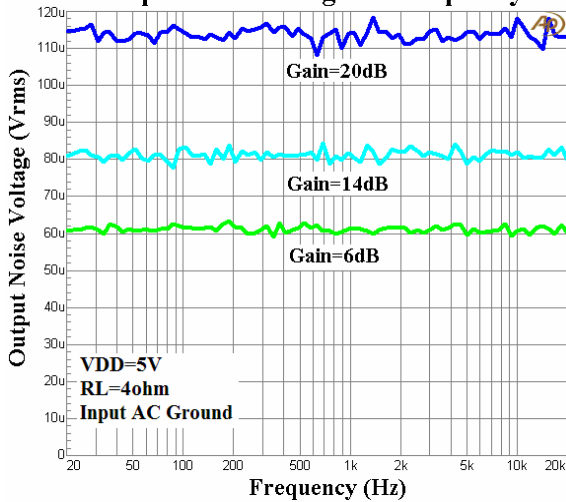
Crosstalk vs. Frequency



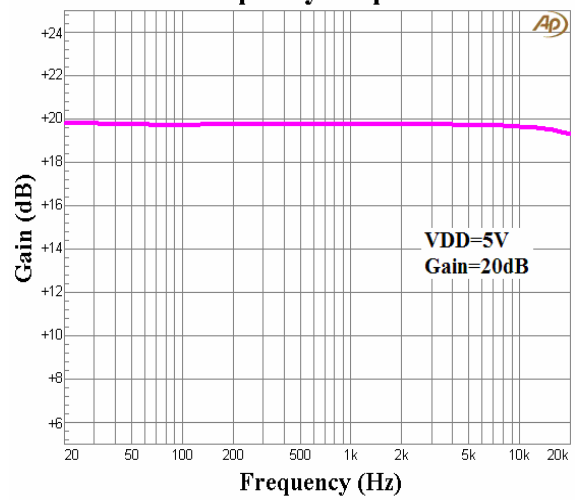
Output Noise voltage vs. Frequency



Output Noise voltage vs. Frequency



Frequency Response



Typical Characteristics (continued)

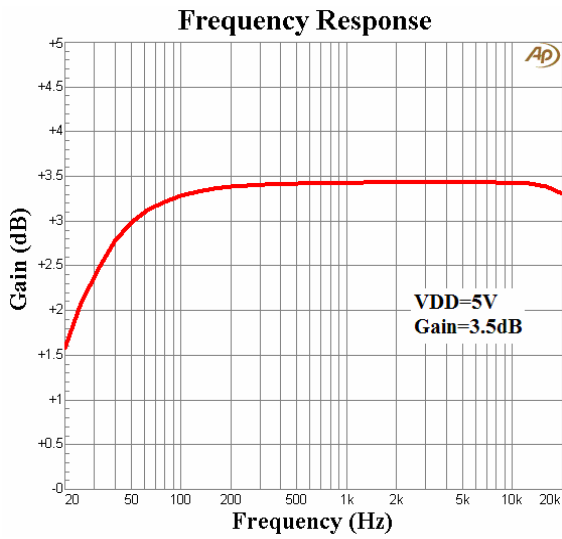


Figure15.

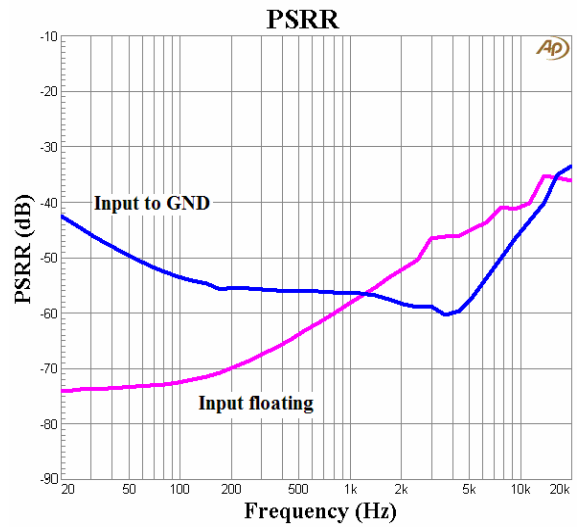


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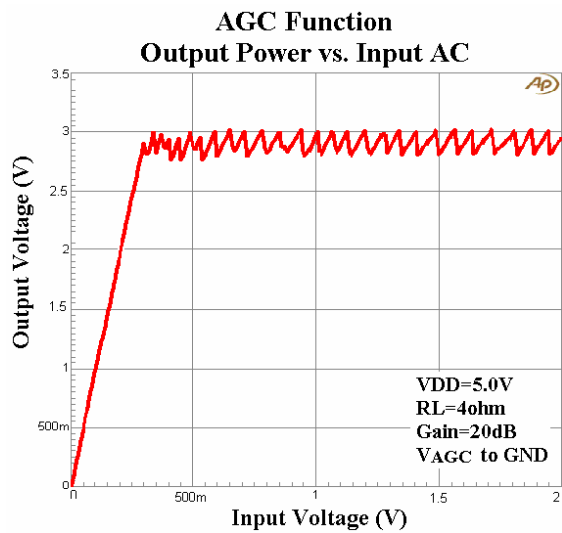


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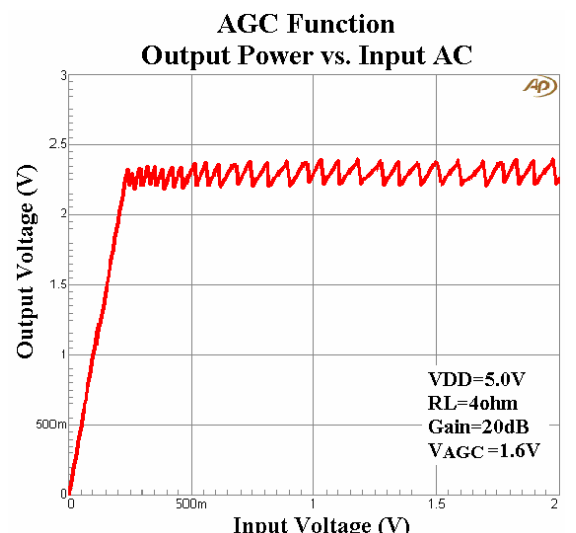


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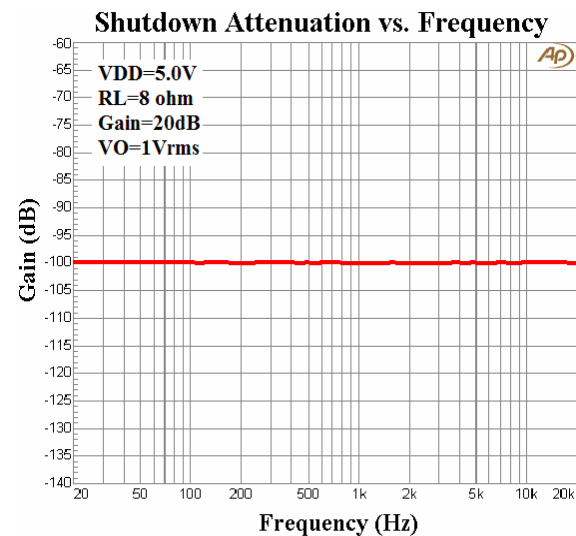


Figure19.

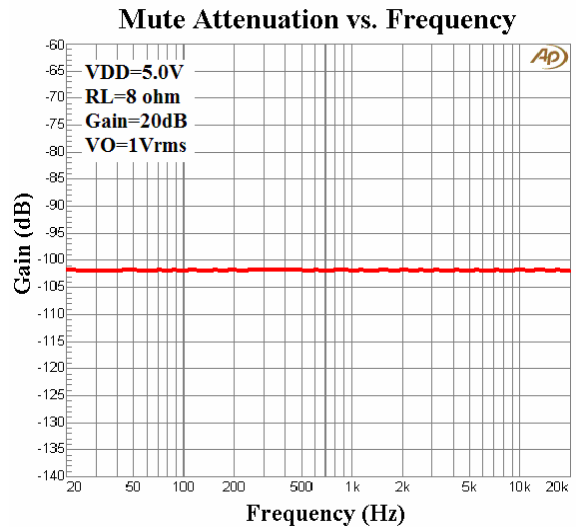


Figure20.

Typical Characteristics (continued)

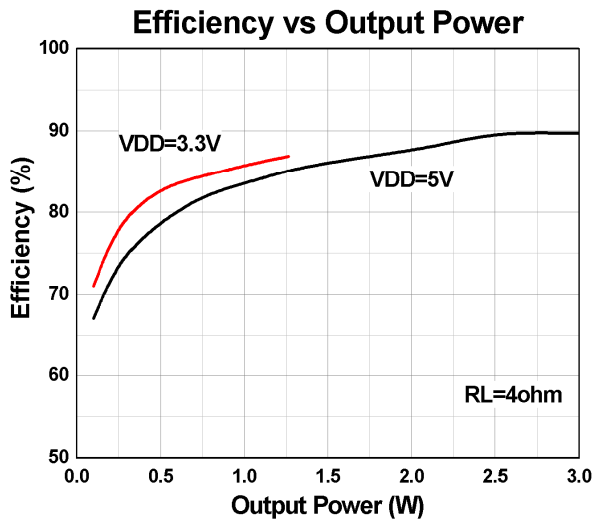


Figure21.

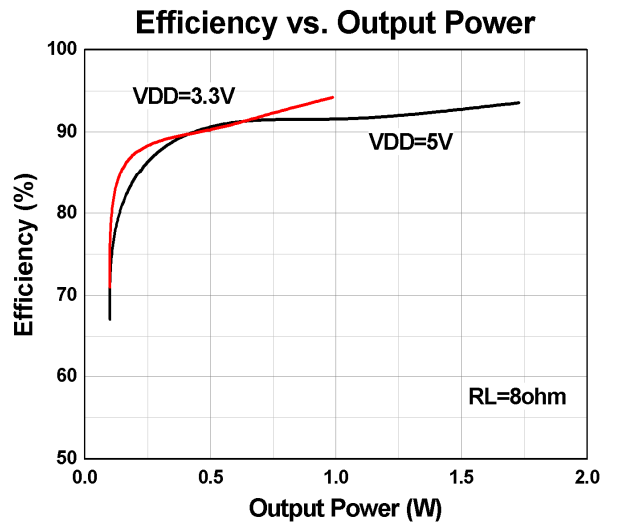


Figure22.

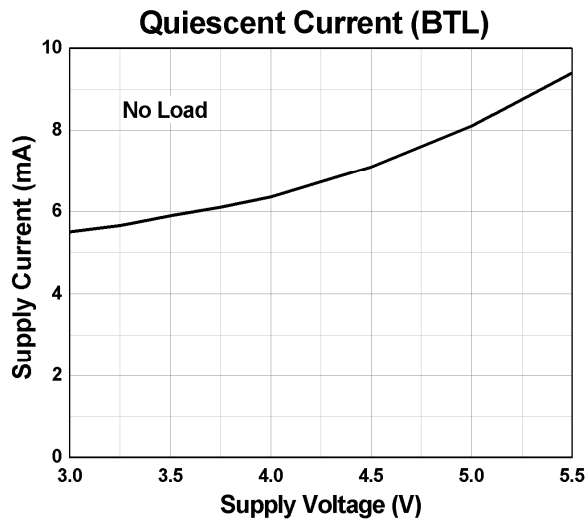


Figure23.

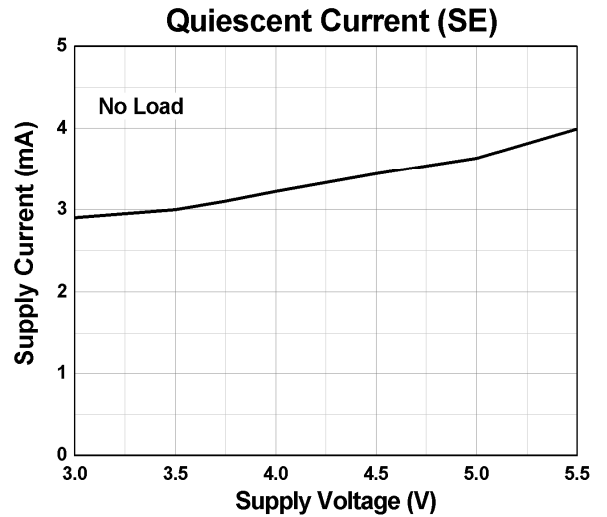


Figure24.

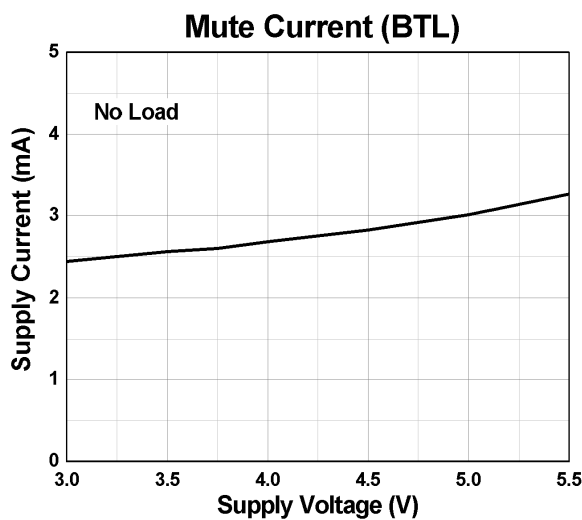


Figure25.

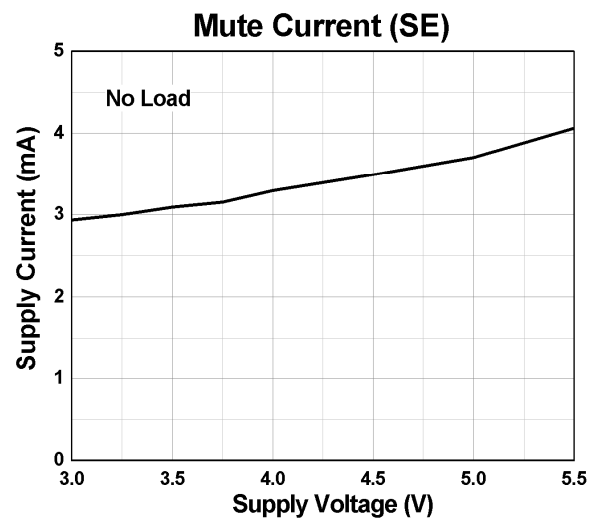


Figure26.

Typical Characteristics (continued)

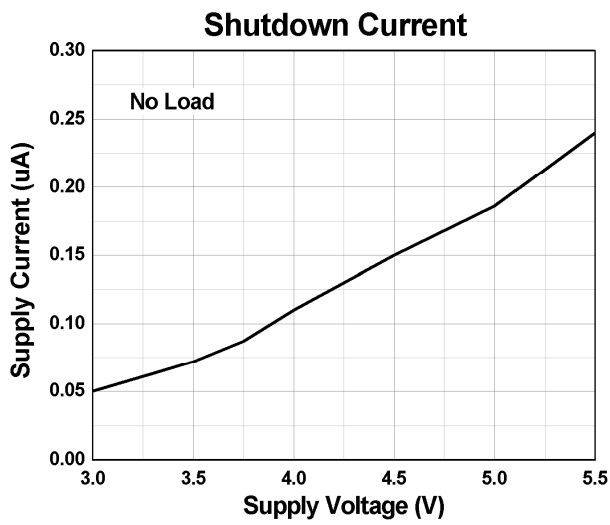


Figure27.

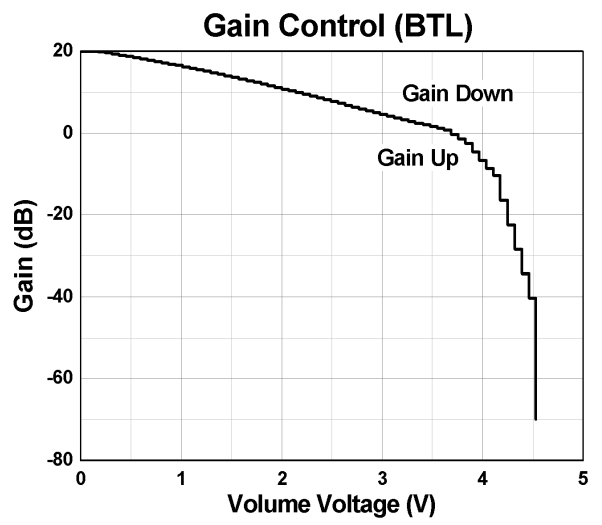


Figure28.

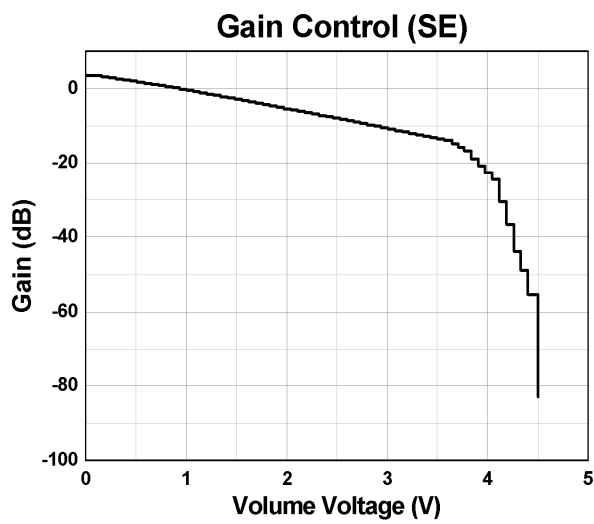


Figure29.

Application Information

Volume Control Operation

The VOLUME terminal controls the internal amplifier gain. This pin is controlled with a dc voltage, which should not exceed VDD. Table 1 lists the gain as determined by the voltage on the VOLUME pin in reference to the voltage on VDD.

A resistor divider can be connected across VDD and AGND. For fixed gain, calculate the resistor divider values necessary to center the voltage between the two percentage points given in the first column of Table 1.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another.

The timing of the volume control circuitry is controlled by an internal 30-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every clock cycle (nominally 32 ms) to the next step until the final desired gain is reached. For example, if the EUA2075 is currently in the 0 dB gain step and the VOLUME pin is adjusted for maximum gain at +20 dB, the time required for the gain to reach +20 dB is 50 steps \times 32ms/step = 1.6 seconds.

FADE Operation

During power-up or recovery from the shutdown state (a logic high is applied to the SDB terminal), the volume is smoothly ramped up from the mute state, -70dB, to the desired volume setting determined by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the SDB terminal.

Auto Gain Control Function

The EUA2075 provides the 64 steps AGC (Auto Gain Control) function, and the range is from 20dB to -70dB. The AGC works when the output reaches the maximum power setting value. The gain will be decreased to prevent the output waveform clipping. The gain changes constantly as the audio signal increases and/or decreases to suppress the clipped output signal.

Table 2. AGC Function

AGC Voltage	Output Power
VDD ~ 0.45VDD or AGC Floating	Disable AGC Function
0.45VDD~0.27VDD	$8 \times (VDD \times 0.5 - V_{AGC})^2 \times 0.95 / R_L$
0.27VDD ~ GND	$P_{OMAX}=2.45W @ 4\Omega$ $P_{OMAX}=1.225W @ 8\Omega$

MUTE Operation

The MUTE pin is an input for controlling the output state of the EUA2075. A logic high on this pin disables the outputs, and a logic low on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade. Quiescent current is listed in the electrical characteristic table. The MUTE pin can't be left floating.

Shutdown Operation

In order to reduce power consumption while not in use, the EUA2075 contains shutdown circuitry to turn off the amplifier's bias circuitry. The amplifier is turned off when logic low is placed on the SDB pin. By switching the SDB pin connected to GND, the EUA2075 supply current draw will be minimized in idle mode. The SDB pin can't be left floating.

For the best power on/off pop performance, the amplifier should be placed in the Mute mode prior to turning on/off the power supply.

Power Supply Decoupling

The EUA2075 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μ F, placed as close as possible to the device VDD terminal works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10 μ F or greater placed near the audio power amplifier is recommended.

Input Capacitor (Ci)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. In this case, input capacitor (Ci) and input resistance (Ri) of the amplifier form a high-pass filter with the corner frequency determined equation below,

$$f_c = \frac{1}{2\pi R_i C_i}$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable.

Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Analog Reference Bypass Capacitor (C_{BYP})

The Analog Reference Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N. A ceramic bypass capacitor (C_{BYP}) of 1μF to 2.2μF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Under Voltage Protection

External under voltage detection can be used to shutdown the EUA2075 before an input device can generate a pop. The shutdown threshold at the UVP pin is 1.2V. A resistor divider can be used to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as below:

With the condition: $R3 \gg R1/R2$

$$V_{UVP} = [1.2 - (5.7\mu A \times R3)] \times (R1 + R2) / R2$$

$$\text{Hysteresis} = (4.6\mu A \times R3) \times (R1 + R2) / R2$$

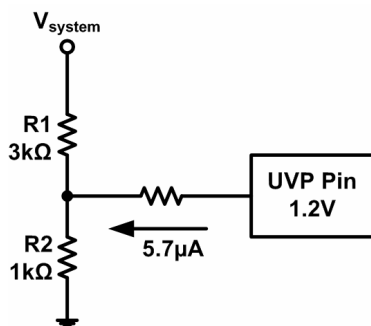


Figure 30. Under Voltage Protection

Short Circuit Protection (SCP)

The EUA2075 has short circuit protection circuitry on the outputs that prevents the device from damage when output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disabled immediately. The IC will turn on the output after about 200ms. But if the short circuit condition is still remain, the output will be disabled again. The situation will circulate until the short circuit condition is removed.

Over Temperature Protection

Thermal protection on the EUA2075 prevents the device from damage when the internal die temperature exceeds 165°C. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. This large hysteresis will prevent motor boating sound well. The device begins normal operation at this point without external system interaction.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000μF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (<20CM). Most applications require a ferrite bead filter as shown at Figure 31. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at low frequency.

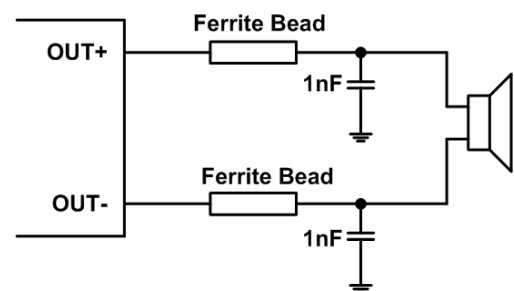
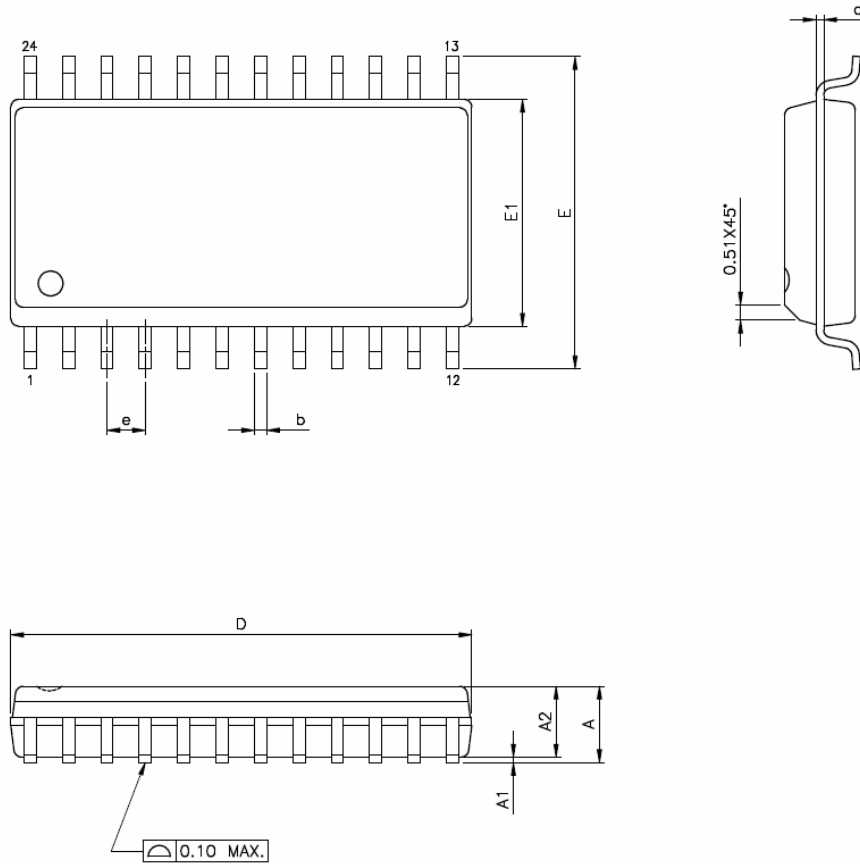


Figure 31. Ferrite Bead output filter

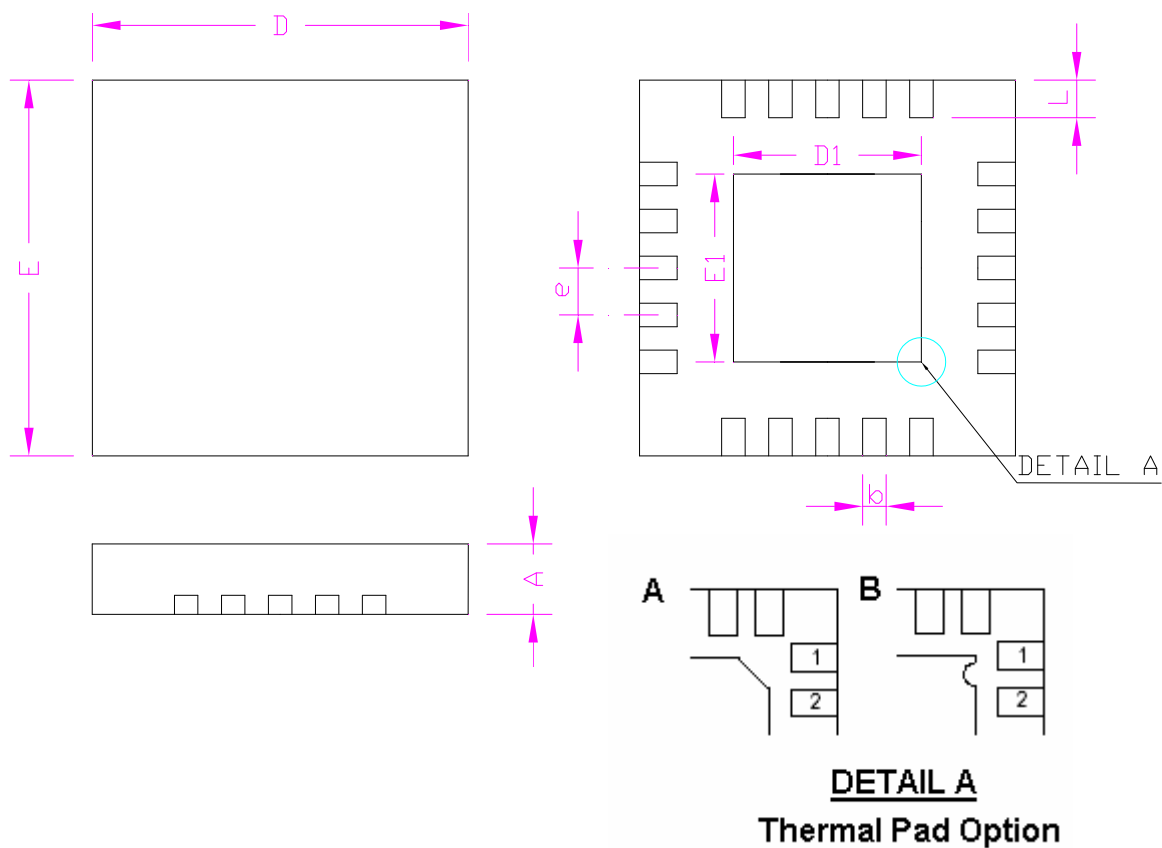
Packaging Information

SOP-24



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.35	2.60	2.80	0.093	0.102	0.110
A1	0.05	-	0.30	0.002	-	0.012
A2	2.00	-	2.65	0.079	-	0.104
b	0.31	0.41	0.51	0.012	0.016	0.020
c	0.20	-	0.35	0.008	-	0.014
D	15.20	15.34	15.75	0.598	0.604	0.620
E	9.75	10.20	10.65	0.384	0.402	0.419
E1	7.35	7.50	7.65	0.289	0.295	0.301
e	1.27 BSC			0.050 BSC		
L	0.38	-	1.27	0.015	-	0.050
Θ	0°	-	8°	0°	-	8°

TQFN-20



SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
b	0.18	0.25	0.32	0.007	0.010	0.013
D	3.90	4.00	4.10	0.154	0.157	0.161
E	3.90	4.00	4.10	0.154	0.157	0.161
D1	1.90	2.00	2.55	0.075	0.079	0.100
E1	1.90	2.00	2.55	0.075	0.079	0.100
e	0.50			0.020		
L	0.30	0.40	0.55	0.012	0.016	0.022