TFT LCD DC-DC Converter with Integrated Charge Pumps, OP-AMP and HV-Switch

DESCRIPTION

The EUP2681 generates power supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in monitors and notebooks operated from 2.5V to 5.5V input supply. The device integrates a step-up converter, positive and negative charge pumps, a high speed V_{COM} buffer and a HV-Switch.

The external compensated step-up converter features an internal power MOSFET and high frequency operation allowing to use small inductors and capacitors. The step up converter uses fixed-frequency peak current mode control architecture which provides fast load-transient response and easy compensation. A 3.5A peak current limit for the internal switch protects power supply fault condition.

The regulated positive and negative charge pump regulators generate the positive and negative supply rails for the TFT LCD gate resistive voltage-divider ICs.

The high speed V_{COM} buffer features 500mA short circuit current, 20MHz bandwidth, fast slew rate 45V/μs, and rail-to-rail inputs and outputs.

The HV-Switch circuit control provides the ability to control the slope for the gate drive voltage. It shapes the TFT gate high voltage to improve image quality.

The EUP2681 is available in a small (4mm× 4mm) 24 pin TQFN package and operates over the -40ºC to +85ºC temperature range.

FEATURES

- 2.5V to 5.5V Input Supply Range
- 1.2MHz Current Mode Step Up Converter
  - Built-In 20V, 3.5A, 0.16Ω N-MOSFET
  - High Efficiency Up to 90%
  - Internal digital Soft-Start
  - Fast Transient Response to Pulsed Load
  - Over-Temperature Protection
- Regulated Charge pump for TFT gate-on Supply
- Regulated Charge pump for TFT gate-off Supply
- High Speed High Current 18V V_{COM} Buffer
  - 20MHz BW
  - 45V/μS Slew Rate
  - More than 500mA Peak Output Current
- HV-Switch Circuit
  - Adjustable Falling rate
  - Reduction of Coupling Effect between Gate Line and Pixel
  - Flicker Compensation Circuit
- Input Under Voltage Lockout and Thermal Protection
- 24 pin 4mm×4mm TQFN Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATIONS

- LCD Monitors
- Notebook Display
- LCD TVs

Typical Application Circuit

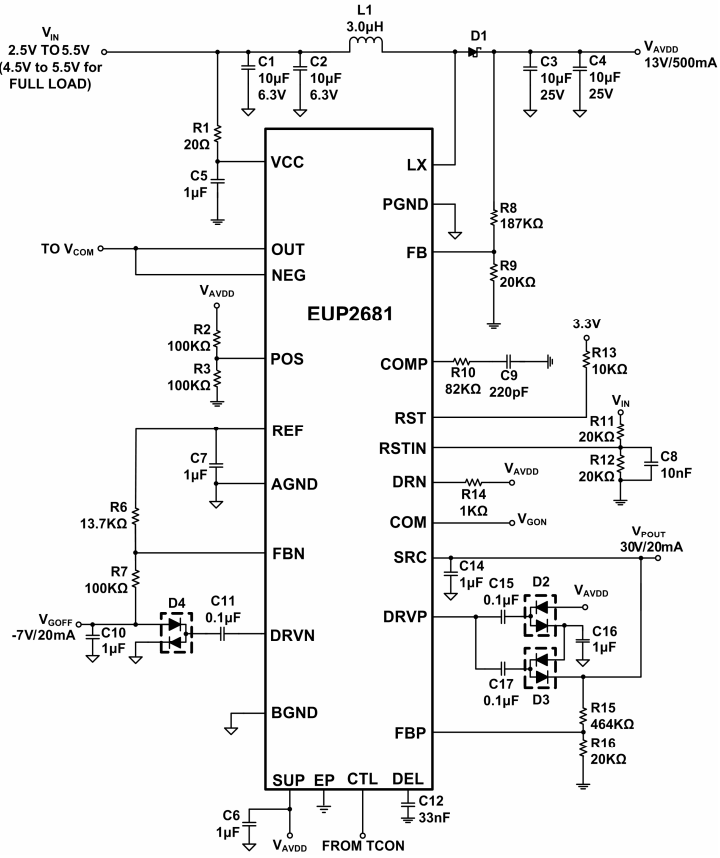


Figure 1. EUP2681 Typical Operating Circuit

Functional Block Diagram

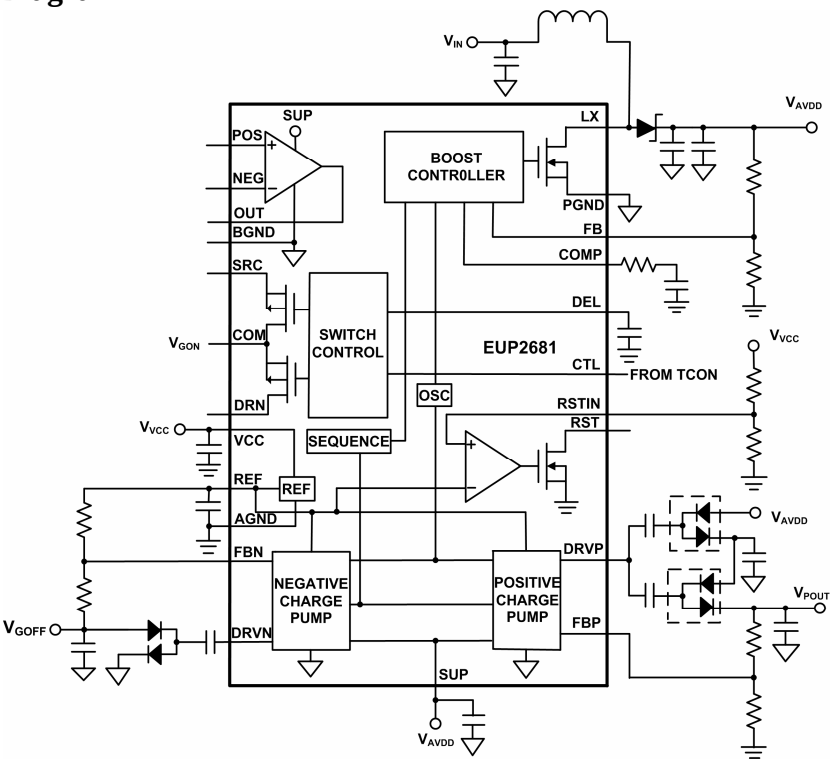
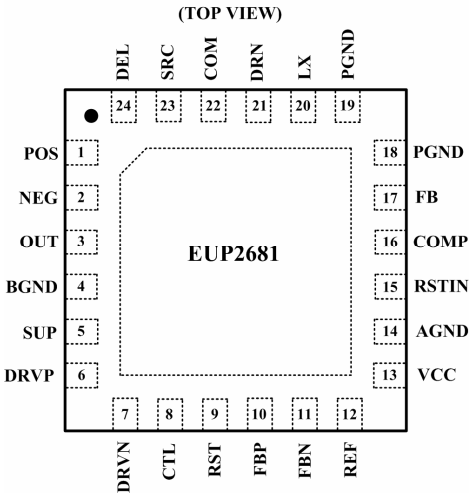


Figure 2. EUP2681 Functional Block Diagram

Pin Configurations

Package Type	Pin Configurations
TQFN-24	

Pin Description

PIN	PIN	DESCRIPTION
1	POS	Operational Amplifier Noninverting Input.
2	NEG	Operational Amplifier Inverting Input.
3	OUT	Operational Amplifier Output.
4	BGND	Analog Ground for Operational Amplifier and Charge Pump. Connect to AGND underneath the IC.
5	SUP	Operational Amplifier and Charge-Pump Supply Input. Connect this pin to the output of the boost Regulator AVDD and bypass to BGND with a minimum 1μF capacitor.
6	DRVP	Positive Charge-Pump Driver Output.
7	DRVN	Negative Charge-Pump Driver Output.
8	CTL	High-Voltage Switch Control Input. When CTL is high, the switch between GON and SRC is on and the switch between GON and DRN is off. When CTL is low, the switch between GON and DRN is on and the switch between GON and SRC is off. CTL is inhibited by VCC UVLO and when DEL is less than 1.25V.
9	RST	Reset Output. RST is an open-drain output.
10	FBP	Positive Charge-Pump Regulator Feedback Input. Connect FBP to the center of a resistive voltage- divider between the positive charge-pump regulator output and AGND to set the positive charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBP.
11	FBN	Negative Charge-Pump Regulator Feedback Input. Connect FBN to the center of a resistive voltage- divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.
12	REF	Reference Output. Connect a 1μF capacitor from REF to AGND. All power outputs are disabled until REF exceeds its UVLO threshold.
13	VCC	Supplies the Internal Reference and Other Internal Circuitry. Connect VCC to the input supply voltage and bypass to AGND with a minimum 1μFceramic capacitor.

Pin Description (continued)

PIN	PIN	DESCRIPTION
14	AGND	Analog Ground for Step-Up Regulator and Linear Regulators.
15	RSTIN	VIN Reset Comparator Input. Connect to the center of a resistor-divider from VIN.
16	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to AGND.
17	FB	Step-Up Regulator Feedback Input. Connect FB to the center of a resistive voltage-divider between the step-up regulator output and AGND to set the regulator's output voltage. Place the resistive voltage- divider within 5mm of FB.
18,19	PGND	Power Ground.
20	LX	Step-Up Regulator Switching Node. Connect inductor and catch diode here and minimize trace area for lowest EMI power ground.
21	DRN	Switch Input. Drain of the internal high-voltage back-to-back p-channel FET connects to COM.
22	COM	Internal High-Voltage MOSFET switch Common Terminal.
23	SRC	Switch Input. Source of the internal high-voltage pFET. Bypass SRC to PGND with a minimum 0.1µF capacitor closed to the cap.
24	DEL	High-Voltage Switch Delay Input. Connect a capacitor from DEL to AGND to set delay.
-	EP	Exposed Pad. Connect EP to AGND.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP2681JIR1	TQFN-24	xxxxx P2681	-40 °C to 85°C

EUP2681 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TQFN

Absolute Maximum Ratings (1)

- VCC, CTL, RSTIN, RST to AGND ---------- -0.3V to +6V
- DEL, REF, COMP, FB, FBN,FBP to AGND ---------- -0.3V to (VCC+0.3V)
- PGND, BGND to AGND ---------- -0.3V to +0.3V
- LX to PGND ---------- -0.3V to +20V
- SUP to PGND ---------- -0.3V to +20V
- DRVN, DRVP to PGND ---------- -0.3V to (VSUP + 0.3V)
- SRC, COM, DRN to AGND ---------- -0.3V to + 36V
- DRN to COM ---------- -30V to +30V
- SRC to SUP ---------- 23V
- REF Short Circuit to AGND ---------- Continuous
- POS, NEG, OUT to AGND ---------- -0.3V to (VSUP + 0.3V)
- DRVN, DRVP RMS Current ---------- 200mA
- LX, PGND RMS Current Rating ---------- 2.4A
- Continuous Power Dissipation (T_A= +70°C)
  24-Pin TQFN (derate 27.8mW/°C above +70°C) ---------- 2222mW
- Junction Temperature ---------- +150°C
- Storage Temperature Range ---------- -65°C to +160°C
- Lead Temp (Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} (TQFN-24) ---------- 45°C/W
- ESD Rating
  Human Body Model ---------- 2kV

Recommend Operating Conditions (2)

- Supply Voltage (V_{IN}) ---------- 2.5V to 5.5V
- Operating Temperature Range ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(V_{VCC} = 5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = 13V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C)

PARAMETER	CONDITIONS	EUP2681			UNIT
		MIN	TYP	MAX	
V_{CC} Input Supply Range		2.5		5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising, hysteresis(typ)=200mV	2.05	2.25	2.45	V
V_{CC} Shutdown Current	V_{CC} = 2V		100	200	µA
V_{CC} Quiescent Current	V_{FB} = 1.3V, Not switching		1	1.5	mA
	V_{FB} = 1.0V, Switching		4	5	
REFERENCE					
REF Output Voltage	No external load	1.238	1.250	1.262	V
REF Load Regulation	0< I_{LOAD} <50µA			6	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage Lockout Threshold	Rising edge. Hysteresis(typ)=200mV		1	1.15	V
OSCILLATOR and TIMING					
Frequency		1000	1200	1400	kHz
Oscillator Maximum Duty Cycle		87	90	93	%
Duration to Trigger Fault Condition	FB or FBP or FBN below threshold	47	55	65	msec

Electrical Characteristics (continued)

(V_{VCC} = 5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = 13V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C)

PARAMETER	CONDITIONS	EUP2681			UNIT
		MIN	TYP	MAX	
OSCILLATOR and TIMING					
DEL Capacitor Charge Current	During startup, V_{DEL} = 1.0V	4	5	6	µA
DEL Turn-On Threshold		1.19	1.25	1.31	V
DEL Discharge Switch on resistance			20		Ω
STEP-UP REGULATOR					
Output Voltage Range		V_{VCC}		18	V
FB Regulation Voltage	FB = COMP, C_{COMP} = 1nF	1.238	1.250	1.262	V
FB Fault Trip Level	Falling Edge	0.96	1	1.04	V
FB Load Regulation	0 < I_{LOAD} < Full, transient only		-1		%
FB Line Regulation	V_{CC} = 2.5V to 5.5V		0.08	0.15	%/V
FB Input Bias Current	V_{FB} = 1.25V	50	125	200	nA
FB Transconductance	ΔI = ±2.5µA at COMP, FB = COMP	75	160	280	µS
FB Voltage Gain	FB to COMP		2600		V/V
LX Current Limit	FB=1.1V, Duty cycle = 75%	2.5	3	3.5	A
LX On-Resistance	I_{LX} = 200mA		0.16	0.25	Ω
LX Leakage Current	V_{LX} = 19V		10	20	µA
Current Sense Transresistance		0.1	0.2	0.3	V/A
Soft-Start period	7 bit current ramp		14		ms
POSITIVE CHARGE PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
V_{SUP} Over Voltage Threshold	V_{SUP} = Rising, Hystersis = 200mV	19	20	21	V
Operating Frequency			0.5×fosc		Hz
FBP Regulation Voltage		1.225	1.25	1.275	V
FBP Line Regulation Error	V_{SUP}=8V to 18V, V_{GON}=30V,			0.2	%/V
FBP Input Bias Current	V_{FBP}=1.5V	-50		+50	nA
DRVP Current Limit	Not in dropout		400		mA
DRVP PCH ON Resistance			4	6	Ω
DRVP NCH ON Resistance			1.5	3	Ω
FBP fault trip level	Falling edge	0.96	1	1.04	V
Positive Charge Pump Soft-Start Period	7 bit voltage ramp with filtering to prevent high peak currents		3	5	ms
NEGATIVE CHARGE PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
Operating Frequency			0.5×fosc		Hz
FBN regulation voltage(V_{REF}-V_{FBN})	V_{REF} -V_{FBN}=1V	0.98	1	1.02	V
FBN Input Bias Current	V_{FBN}=0mV	-50		+50	nA
FBN Line Regulation Error	V_{SUP}=9V to 18V, V_{GOFF}=-7V			0.2	%/V
DRVN PCH On-resistance			4	6	Ω
DRVN NCH On-resistance			1.5	3	Ω
DRVN Current Limit	Not in dropout		400		mA
FBN fault trip level	Rising edge		450		mV
Negative Charge Pump Soft-Start Period	7 bit voltage ramp with filtering to prevent high peak currents		3	5	ms

Electrical Characteristics (continued)

(V_{VCC} = 5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = 13V, T_A = 0°C to +85°C, unless otherwise noted.
Typical values are at TA = +25°C)

PARAMETER	CONDITIONS	EUP2681			UNIT
		MIN	TYP	MAX	
POSITIVE GATE DRIVER TIMING AND CONTROL SWITCHES					
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		2			V
CTL Input Current	CTL=0V or V_{VCC}	-1		1	µA
CTL to COM Rising Propagation Delay	C_{LOAD}= 100pF		250		ns
SRC Input Voltage Range				36	V
SRC-to-COM Switch On-Resistance	DEL = 1.5V, CTL = VCC		5	10	Ω
DRN-to-COM Switch ON-Resistance	DEL = 1.5V, CTL = AGND		30	60	Ω
COM-to-GND Pull Down	DEL= 0V		1.5	2.5	KΩ
SRC Input Current	DEL = 1.5V, CTL = VCC		300	600	µA
	DEL = 1.5V, CTL = AGND		200	360	µA
OPERATIONAL AMPLIFIERS					
SUP Supply Range		6		18	V
V_{SUP} Undervoltage Threshold		3.8	4	4.2	V
SUP Supply Current	Buffer configuration, V_{POS}= V_{SUP}/2, no load		4	6.5	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{SUP}/2, T_A = 25°C			8	mV
Input Bias Current	V_{NEG}, V_{POS} = V_{SUP}/2	-1		+1	µA
Input Common Mode Voltage Range		0		V_{SUP}	V
Input Common Mode Rejection Ratio			80		dB
Output Voltage Swing High	I_{OUT} = 1mA	V_{SUP} -50			mV
	I_{OUT} = 50mA	V_{SUP}-300			
Output Voltage Swing Low	I_{OUT} = -1mA			50	mV
	I_{OUT} = -50mA			300	
Large Signal Voltage Gain	V_{OUT} = 1V to (V_{SUP} -1)V		80		dB
Slew Rate			45		V/µs
-3dB Bandwidth			20		MHz
Short Circuit Current	Sourcing	500			mA
	Sinking	500			
XAO CONTROL					
RSTIN Threshold	Falling Edge @ VCC=5V	1.225	1.25	1.275	V
	Falling Edge @ VCC=1.8V	1.213	1.25	1.287	V
RSTIN Input Current		-1		1	µA
RSTIN Hysteresis		30	50	80	mV
RST Output Voltage	I_{SINK}=1mA			0.4	V
RST Blanking Time	Counting from V_{VCC} crossing 2.25V	160	220	280	msec
XAO UVLO	V_{VCC} rising with hysteresis of 50mV		1.5	1.7	V

Electrical Characteristics (continued)

(V_{CC} = 5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = 13V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	EUP2681			UNIT
		MIN	TYP	MAX	
V_{CC} Input Supply Range		2.5		5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising, hysteresis(typ)=200mV	2.05		2.45	V
V_{CC} Shutdown Current				200	μA
V_{CC} Quiescent Current	V_{FB} = 1.3V, Not switching			1.5	mA
	V_{FB} = 1.0V, Switching			5	
REFERENCE					
REF Output Voltage	No external load	1.230		1.267	V
REF Load Regulation	0< I_{LOAD} <50μA			6	mV
REF Sink Current	In regulation	10			μA
REF Undervoltage Lockout	Rising edge. Hysteresis(typ)=200mV			1.15	V
OSCILLATOR and TIMING					
Frequency		1000		1400	kHz
Oscillator Maximum Duty Cycle		87		93	%
Duration to Trigger Fault Condition	FB or FBP or FBN below threshold	47		65	msec
DEL Capacitor Charge Current	During startup, V_{DEL} = 1.0V	4		6	μA
DEL Turn-On Threshold		1.19		1.31	V
STEP-UP REGULATOR					
Output Voltage Range		V_{IN}		18	V
FB Regulation Voltage	FB = COMP, C_{COMP} = 1nF	1.230		1.267	V
FB Fault Trip Level	Falling Edge	0.96		1.04	V
FB Line Regulation	V_{CC} = 2.5V to 5.5V			0.25	%/V
FB Input Bias Current	V_{FB} = 1.25V	50		200	nA
FB Transconductance	ΔI = ±2.5μA at COMP, FB = COMP	75		280	μS
LX Current Limit	FB=1.1V, Duty cycle = 75%	2.5		3.5	A
LX On-Resistance	I_{LX} = 200mA			0.25	Ω
Current Sense Transresistance		0.10		0.30	V/A
POSITIVE CHARGE PUMP REGULATOR					
V_{SUP} Input Supply Range		6		18	V
V_{SUP} Over Voltage Threshold	V_{SUP} = Rising, Hystersis = 200mV	19		21	V
FBP Regulation Voltage		1.225		1.275	V
FBP Line Regulation Error	V_{SUP}=8V to 18V, V_{GON}=30V,			0.2	%/V
FBP Input Bias Current	V_{FBP}=1.5V	-50		+50	nA
DRVP PCH ON Resistance				6	Ω
DRVP NCH ON Resistance				3	Ω
FBP fault trip level	Falling edge	0.96		1.04	V
Positive Charge Pump Soft-Start Period	7 bit voltage ramp with filtering to prevent high peak currents			5	ms
NEGATIVE CHARGE PUMP REGULATOR					
VSUP Input Supply Range		6		18	V
FBN regulation voltage(V_{REF} -V_{FBN})	V_{REF} - V_{FBN}=1V	0.96		1.04	V
FBN Input Bias Current	V_{FBN}=0mV	-50		+50	nA
FBN Line Regulation Error	V_{SUP}=9V to 18V, V_{GOFF}=-7V			0.2	%/V

Electrical Characteristics (continued)

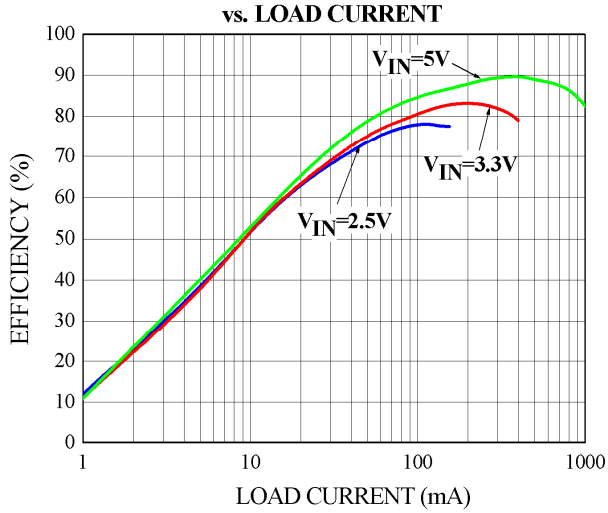
(V_{CC} = 5V, Circuit of Figure 1, V_{AVDD} = V_{SUP} = 13V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	EUP2681			UNIT
		MIN	TYP	MAX	
NEGATIVE CHARGE PUMP REGULATOR					
DRVN PCH On-resistance				6	Ω
DRVN NCH On-resistance				3	Ω
Negative Charge Pump Soft-Start Period	7 bit voltage ramp with filtering to prevent high peak currents			5	ms
POSITIVE GATE DRIVER TIMING AND CONTROL SWITCHES					
CTL Input Low Voltage				0.6	V
CTL Input High Voltage		2			V
CTL Input Current	CTL=0V or V_{VCC}	-1		1	µA
SRC Input Voltage Range				36	V
SRC-to-COM Switch On-Resistance	DEL = 1.5V, CTL = VCC			10	Ω
DRN-to-COM Switch ON-Resistance	DEL = 1.5V, CTL = AGND			60	Ω
COM-to-GND Pull Down	DEL= 0V		1.5	2.5	KΩ
SRC Input Current	DEL = 1.5V, CTL = VCC			600	µA
	DEL = 1.5V, CTL = AGND			360	µA
OPERATIONAL AMPLIFIERS					
SUP Supply Range		6		18	V
V_{SUP} Undervoltage Threshold		3.8	4	4.2	V
SUP Supply Current	Buffer configuration, V_{POS}=V_{SUP}/2, no load			6.5	mA
Input Offset Voltage	V_{NEG}, V_{POS} = V_{SUP}/2, T_A = 25°C			8	mV
Input Bias Current	V_{NEG}, V_{POS} = V_{SUP}/2	-1		+1	µA
Input Common Mode Voltage Range		0		V_{SUP}	V
Output Voltage Swing High	I_{OUT} = 1mA	V_{SUP} -50			mV
	I_{OUT} = 50mA	V_{SUP}-300			
Output Voltage Swing Low	I_{OUT} = -1mA			50	mV
	I_{OUT} = -50mA			300	
Short Circuit Current	Sourcing	500			mA
	Sinking	500			
XAO CONTROL					
RSTIN Threshold	Falling Edge	1.225		1.275	V
RSTIN Input Current		-1		1	µA
RSTIN Hysteresis	Falling Edge	30		80	mV
RST Output Voltage	I_{SINK}=1mA			0.4	V
RST Blanking Time	Counting from V_{VCC} crossing 2.25V	160		280	msec
XAO UVLO	V_{CC} rising with typical hysteresis of 50mV			1.7	V

Note (3): -40°C specs are guaranteed by design, not production tested.

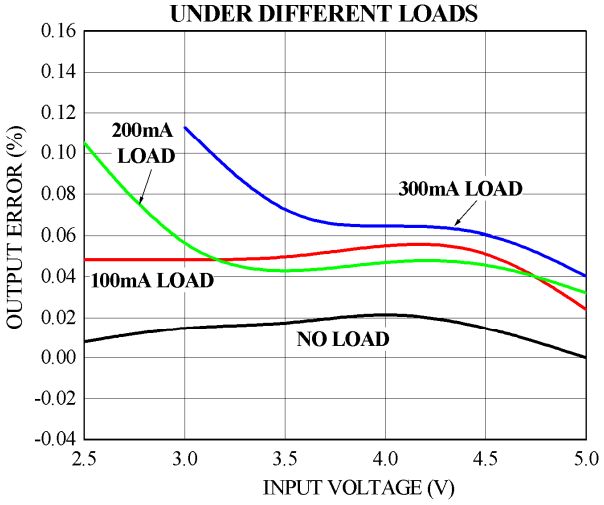
Typical Operating Characteristics

STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT

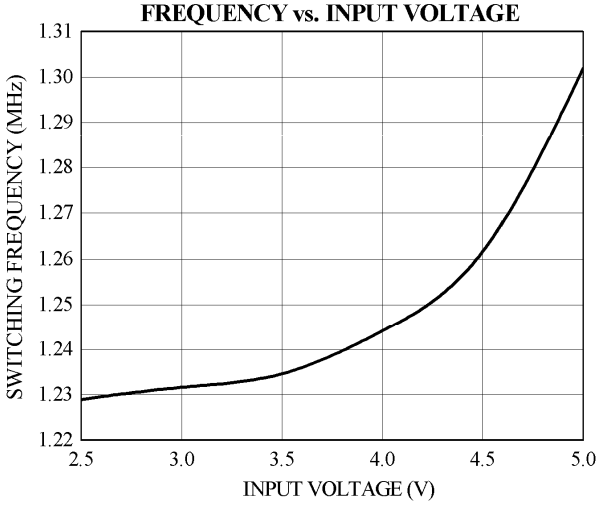


STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT

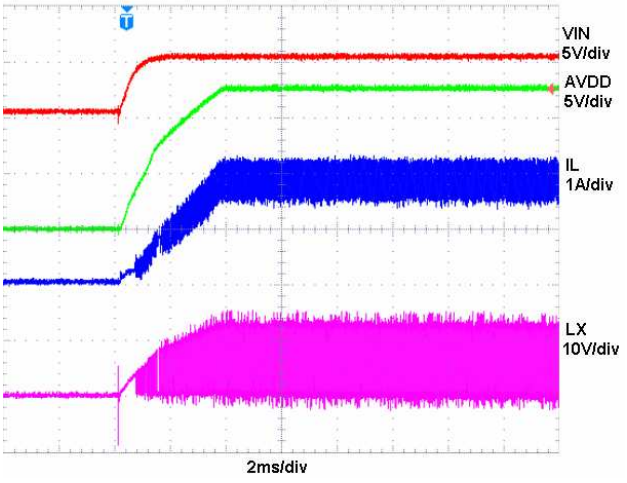
STEP-UP REGULATOR LINE REGULATION UNDER DIFFERENT LOADS



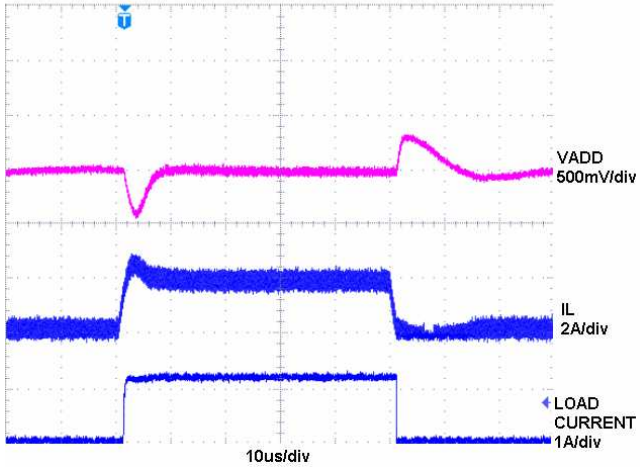
STEP-UP REGULATOR SWITCHING FREQUENCY vs. INPUT VOLTAGE



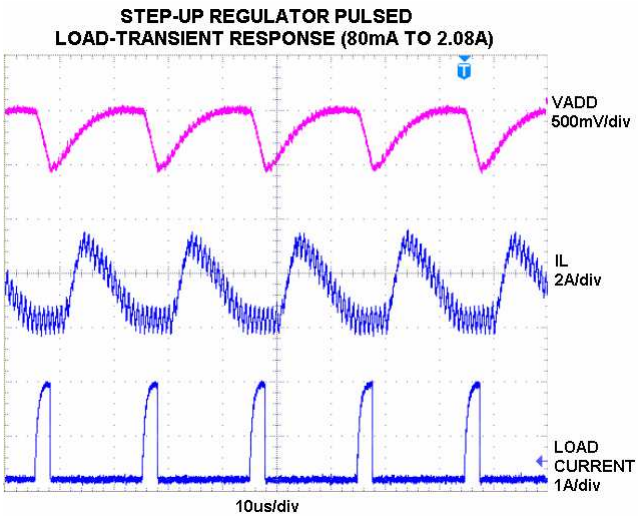
STEP-UP REGULATOR STARTUP WITH HEAVY LOAD (600mA)

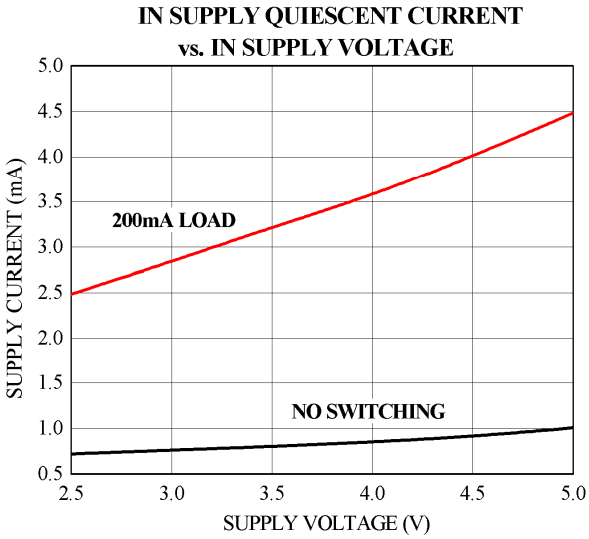


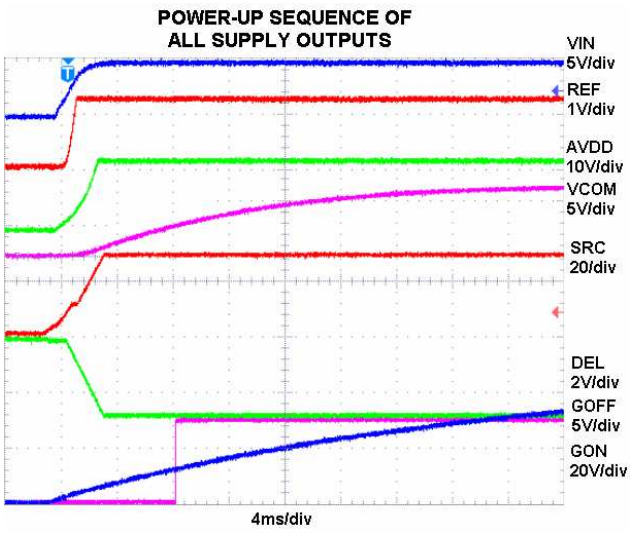
STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (100mA TO 800mA)

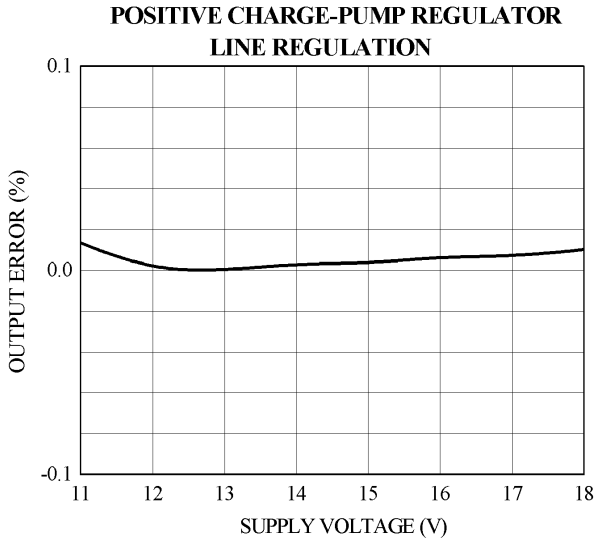


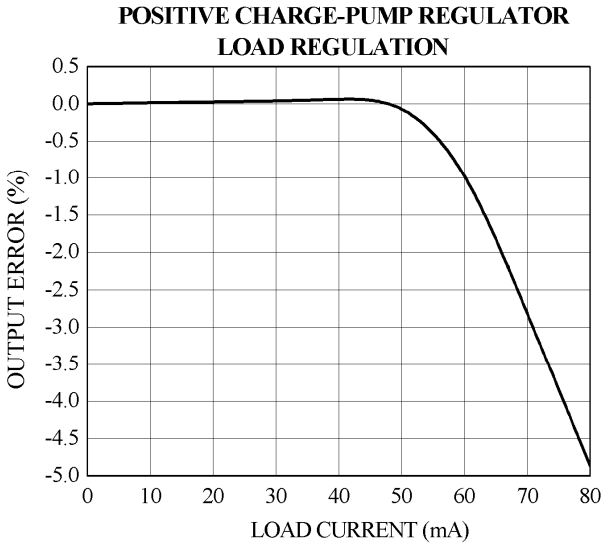
Typical Operating Characteristics (continued)

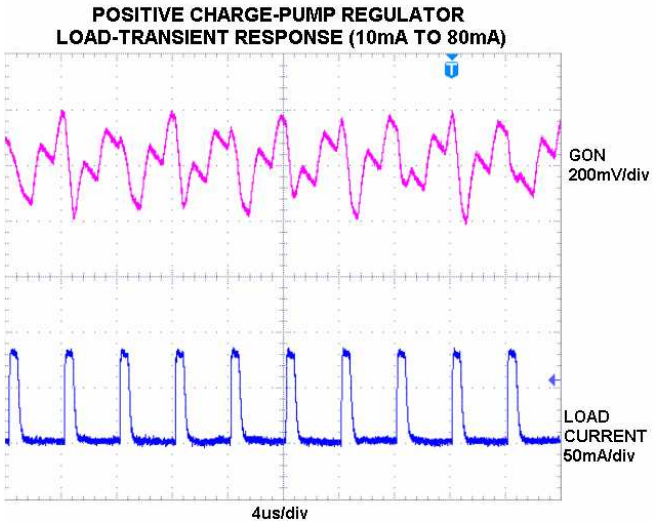






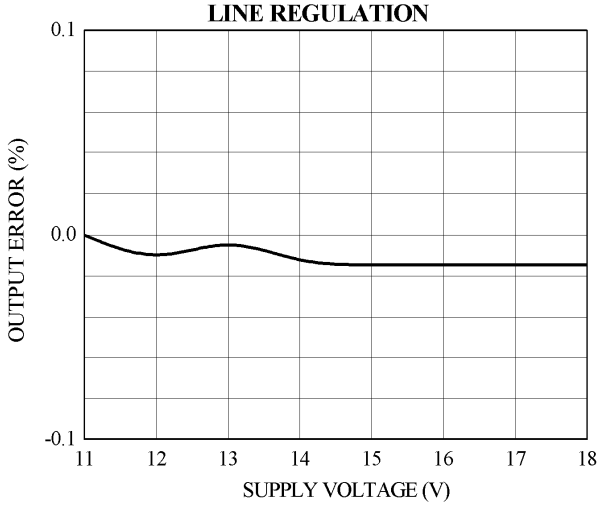




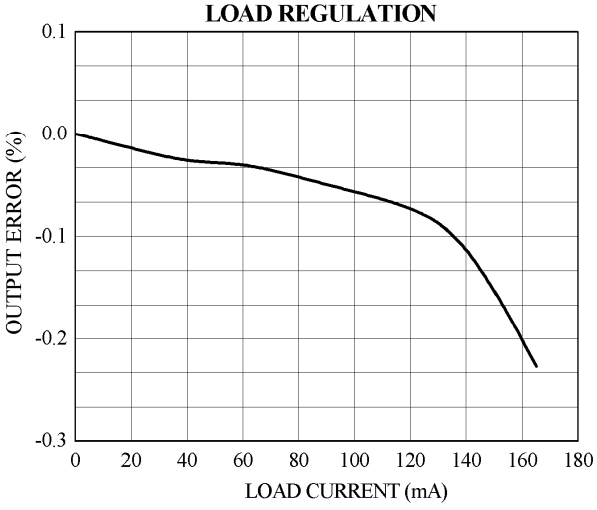


Typical Operating Characteristics (continued)

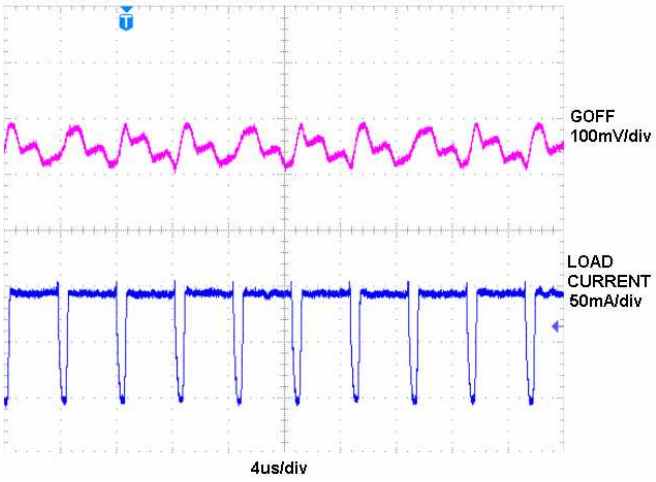
NEGTIVE CHARGE-PUMP REGULATOR
LINE REGULATION



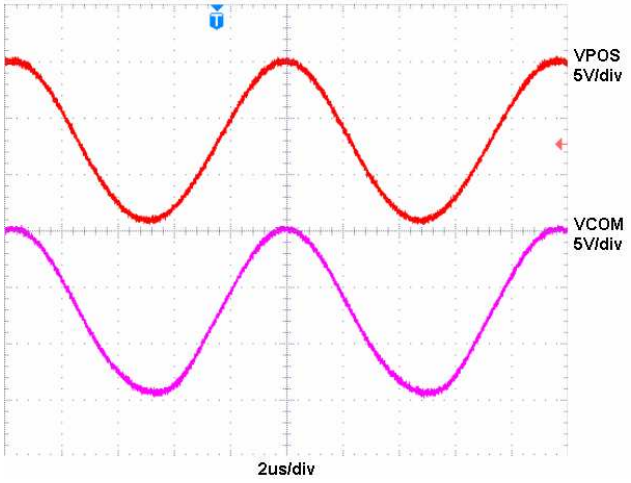
NEGTIVE CHARGE-PUMP REGULATOR
LOAD REGULATION



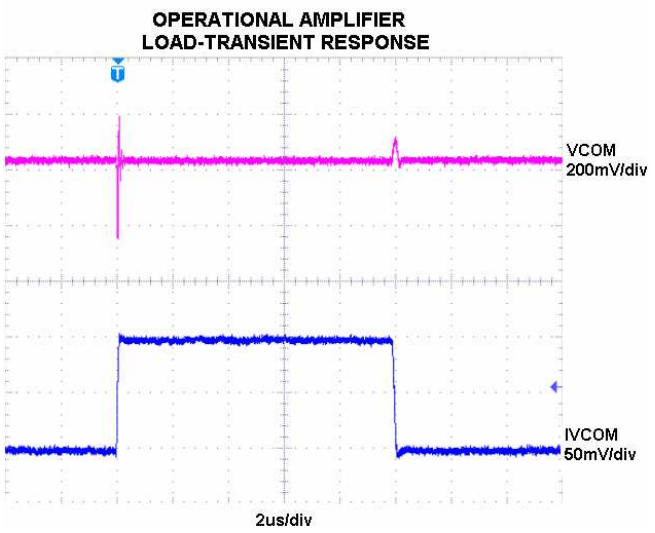
NEGATIVE CHARGE-PUMP REGULATOR
LOAD-TRANSIENT RESPONSE (10mA TO 100mA)



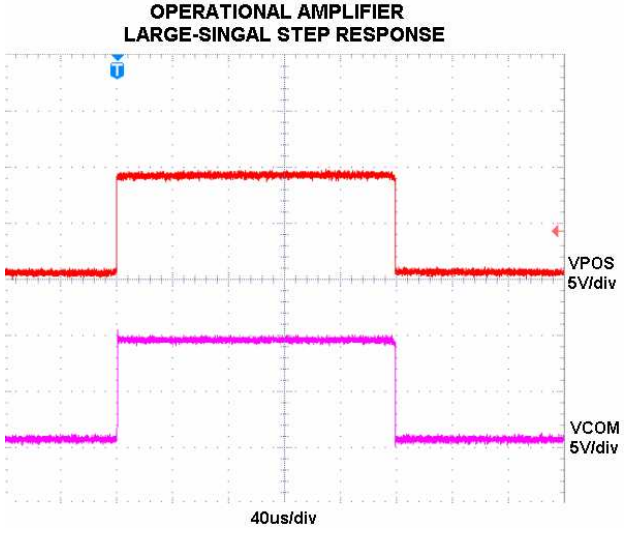
OPERATIONAL AMPLIFIER RAIL-TO-RAIL
INPUT/OUTPUT WAVEFORMS



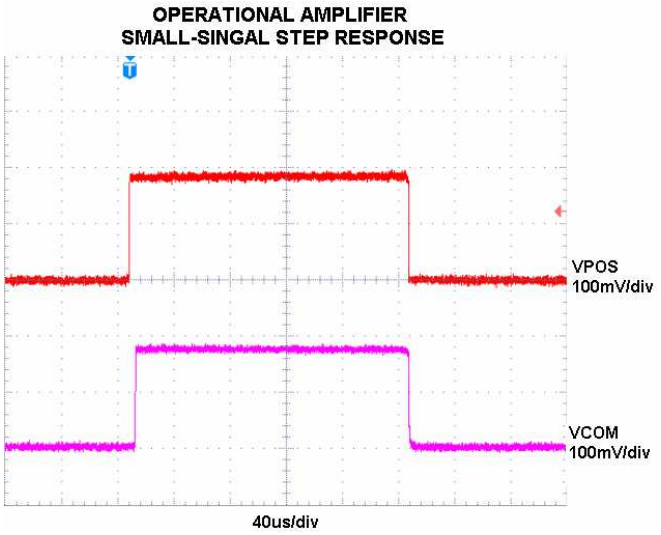
OPERATIONAL AMPLIFIER
LOAD-TRANSIENT RESPONSE

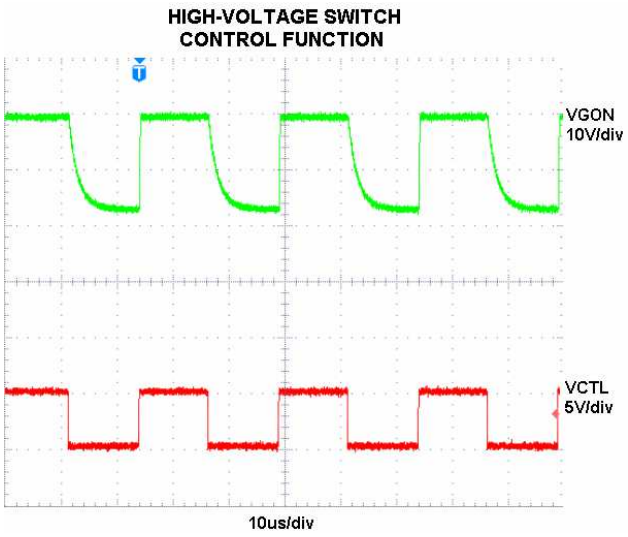


OPERATIONAL AMPLIFIER
LARGE-SINGAL STEP RESPONSE



Typical Operating Characteristics (continued)





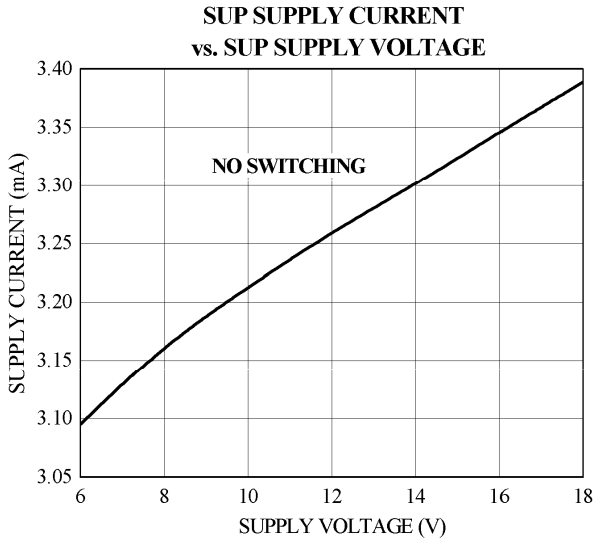


Table 1. Component List (Figure 1)

Designation	Description
C1, C2	10µF, 6.3V, X5R ceramic capacitors
C3, C4	10µF, 25V, X5R ceramic capacitors
C5, C7	1µF, 6.3V, X7R ceramic capacitors
C6	1µF, 25V, X7R ceramic capacitor
C8	10nF, 50V, X7R ceramic capacitor
C9	220pF, 50V, X7R ceramic capacitor
C10, C14, C16	1µF, 50V, X7R ceramic capacitors
C11, C15, C17	0.1µF, 50V, X7R ceramic capacitors
C12	33nF, 50V, X7R ceramic capacitor
D1	Schottky diode 30V, 3A Toshiba CMS02 (TE12L,Q)
D2, D3, D4	Dual diodes 30V, 200mA(3 SOT23) Zetex BAT54S Fairchild BAT54S
L1	Inductor, 3µH, 3A Sumida CDRH6D28-3R0

Function Description

Step Up Converter

Step up Converter can operate in continuous conduction mode and steady state operation, where the inductor current is continuously. In the first half cycle, the power MOSFET is on and Schottky diodes are reverse biased, the output current is provided by output capacitor, inductor voltage is V_{IN} , and its current increase at the rate of V_{IN}/L; during the other half cycle, MOSFET is off and Schottky diodes are forward biased, the energy stored in the inductor is released. The inductor current ripple is:

$$\Delta I_L = \Delta T_2 \times \frac{V_{IN} - V_{OUT}}{L}$$

$$\Delta T_2 = \frac{1-D}{F_{SW}}$$

Where L is self-inductance, the energy of inductor is stored by electromagnetic induction.

In the steady state operation, the energy stored in inductor must be converted equally, so the inductor current ripples in two half cycle are identical.

$$\Delta I_{L1} + \Delta I_{L2} = 0$$

$$\frac{D}{F_{SW}} \times \frac{V_{IN}}{L} + \frac{1-D}{F_{SW}} \times \frac{V_{IN} - V_{OUT}}{L} = 0$$

$$\frac{V_{STEP-UP}}{V_{IN}} = \frac{1}{1-D}$$

Output Voltage

The output voltage is reduced to a reference voltage 1.25V by external feedback resistor divider. The resistors maximum value is limited by feedback output biased current and potential coupling noise of feedback pin. Output voltage of Step up Converter can be set according to the following equations:

$$V_{STEP-UP} = V_{FB} \times \left[1 + \frac{R_8}{R_9} \right]$$

Where the range of R_2 is from 10KΩ to 50KΩ, typical value of V_{FB} is 1.25V.

Inductor Selection

The output voltage ripple, transient response, capacity and efficiency of output current supply are decided by inductor selection and the inductor value is influenced by input and output voltage, switching frequency and the maximum output current. For most application, 3µH inductor fits the application of 1.2MHz.

Moreover, it is noteworthy that the maximum direct current of inductor must exceed the peak inductor current expected by power MOSFET, the peak current value can be calculated as：

$$I_{L(PEAK)} = \frac{I_{OUT} \times V_{STEP-UP}}{V_{IN}} + 1/2 \times \frac{V_{IN} \times (V_{STEP-UP} - V_{IN})}{L \times V_{STEP-UP} \times F_S}$$

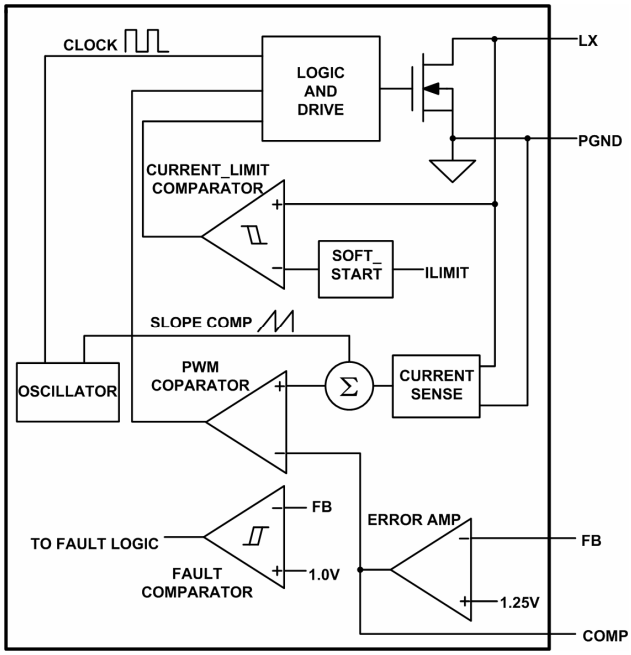


Figure 3. Step-Up Regulator Functional Diagram

Output Capacitor:

Small value of ESR capacitor can minimum the output voltage ripple. So it is recommended that multi-layer ceramic capacitors（X5R or X7R）are used to be output capacitor because of its low ESR characteristics and small size in package. Higher ESR tantalum capacitor is also preferred. ESR determines the output voltage ripple according to the equation:

$$\Delta V_O = \frac{I_{OUT} \times D}{F_S \times C_O} + I_{OUT} \times ESR$$

To meet the requirements of output ripple and load transient response, 10µF~47µF ceramic capacitor is often selected. In the noise sensitive operation, a 0.1µF parallel bypass capacitor could be connected to output capacitor for reducing the high frequency noise of the LX switching.

Schottky Diode

The Schottky diode for a high performance converter must be chosen correctly depending on some parameters such as reverse breakdown voltage, forward current and forward voltage drop. Schottky diodes of EUP2681 must follow these rules: 3A maximum output current; reverse breakdown voltage must be greater than the peak output voltage; low forward voltage drop, low dropout current and fast reverse recovery.

Input Capacitor

Input capacitors, which are decided by input and output voltage, maximum output current, inductor and supply noise, are important in restraining input voltage ripple and enhancing chip performance. In most application, a 20µF capacitor is suitable, but if the output current is close to 3A, output capacitor must be set from 22µF to 47µF. Care must be taken to make sure that chip is normal operated, a 20Ω resistor and a 1µF bypass capacitor should be taken next to the VCC pin to decrease the high frequency noise of power wire.

Loop Compensation

The feedback loop of EUP2681 contains a trans-conductance amplifier, which makes the chip achieve better transient response and regulation. The EUP2681 employs current mode control architecture, which features rapid current sense loop and slow voltage feedback loop. Compensation is not required for rapid current sense loop but is necessary for slow voltage feedback loop to insure that the device is in the steady state. RC network connected between the COMP pin and GND is a compensation network. In the network, resistors play a decisive role in achieving a high gain of high-frequency and obtain fast transient response. Capacitor sets the zero of the integrator. Assuring about loop stabilization, capacitor must be chosen between 220pF~10nF and resistor must be chosen accurately in the range of 2kΩ ~100kΩ.

Maximum Output Current

The output current capacity of EUP2681 is influenced by current limitation, input voltage, working frequency and inductance value, and described as follows：

$$I_L = I_{L-AVG} + (1/2 \times \Delta I_L)$$

where:

I_L = current limitation of MOSFET

$I_{L\text{-}AVG}$ = average inductor current

ΔI_L = inductor current ripple

$$\Delta I_L = \frac{V_{IN} \times (V_O + V_{DIODE} - V_{IN})}{L \times (V_O + V_{DIODE}) \times F_S}$$

V_{DIODE} ：forward voltage of Schottky diode (typical value is 0.3 V)；

F_S ：switching frequency，1.2MHz；

$$I_{L\text{-}AVG} = \frac{I_{OUT}}{1 - D}$$

D：conductive rate of MOSFET，

$$D = 1 - \frac{V_{IN}}{V_{STEP\text{-}UP} + V_{DIODE}}$$

Dual Charge-Pump Regulator

The EUP2681 contain two individual low-power charge pumps. One charge pump inverts the supply voltage (SUP) and provides a regulated negative output voltage. The second charge pump triples the supply voltage (SUP) and provides a regulated positive output voltage. The EUP2681 contain internal p-channel and n-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant 600 kHz (0.5 x f_{OSC}).

Negative Charge Pump

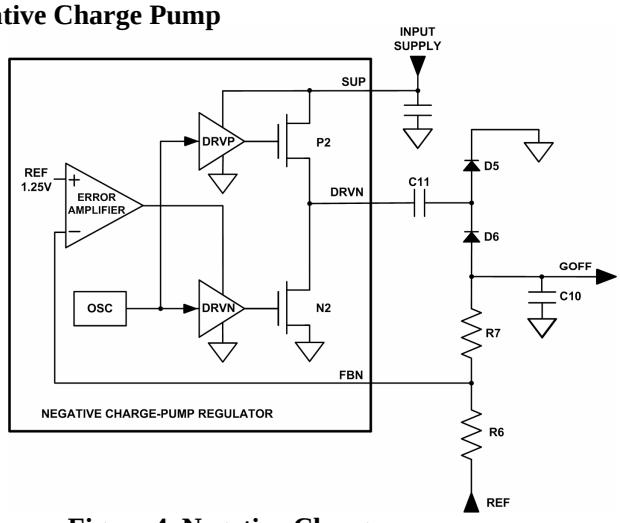


Figure 4. Negative Charge-pump

During the first half-cycle, the p-channel MOSFET turns on and the flying capacitor C11 charges to V_{SUP} minus a diode drop. During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting C11. This connects C11 in parallel with the reservoir capacitor C10. If the voltage across C10 minus a diode drop is higher lower than the voltage across C11, charge flows from C10 to C11 until the diode (D6) turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance.

Positive Charge Pump

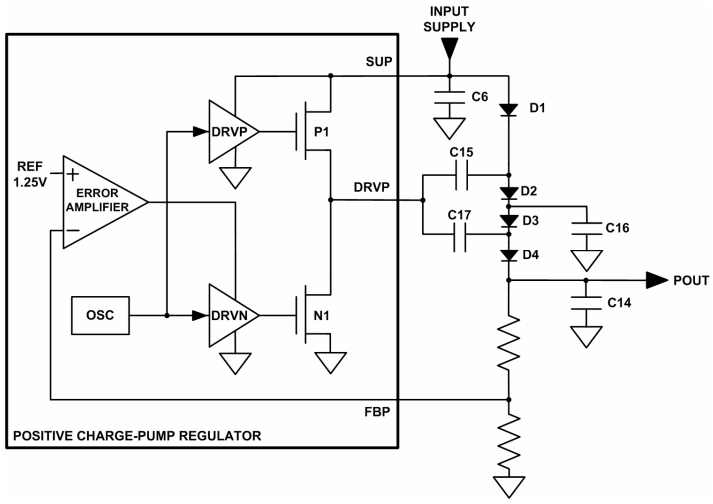


Figure 5. Positive Charge-pump

During the first half-cycle, the n-channel MOSFET turns on and charges the flying capacitor C15 and C17. This initial charge is controlled by the variable n-channel on resistance. During the second half-cycle, the n-channel MOSFET turns off and the p-channel MOSFET turns on, level shifting C15 and C17 by V_{SUP} volts. If the voltage across C14 plus a diode drop (V_{POS} +V_{DIODE}) is smaller than the level-shifted flying capacitor voltage (V_{C17} +V_{SUP}) charge flows from C17 to C14 until the diode (D4) turns off.

Efficiency Considerations

The efficiency characteristics of the EUP2681 regulated charge pumps are similar to a linear regulator. They are dominated by quiescent current at low output currents and by the input voltage at higher output currents. So the maximum efficiency can be approximated by:

$$Efficiency \cong V_{NEG}/[V_{SUP} \times N]$$

For the negative charge pump

$$Efficiency \cong V_{POS}/[V_{SUP} \times (N+1)]$$

For the positive charge pump, where N is the number of charge-pump stages.

Output Voltage Selection

Adjust the positive output voltage by connecting a voltage-divider from the output (V_{POS}) to FBP to GND Typical Operating Circuit. Adjust the negative output voltage by connecting a voltage-divider from the output to FBN to REF. Higher resistor values improve efficiency at low output current but increase output-voltage error due to the feedback input bias current. Calculate the remaining resistors with the following equations:

$$R15 \cong R16[(V_{POS}/V_{REF})-1]$$

$$R6 \cong R7[(V_{REF}-V_{FBN})/(V_{FBN}-V_{GOFF})]$$

Where V_{REF}=1.25V.V_{POS} can range from V_{SUP} to 36V and V_{NEG} can range from 0 to AVDD.

Flying Capacitor

Increasing the flying capacitor's value reduces the output current capability. Above a certain point, increasing the capacitance has a negligible effect because the output current capability becomes dominated by the internal switch resistance and the diode impedance. Start with 0.1uF ceramic capacitors. Smaller values can be used for low-current applications.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq [I_{OUT}/(600KHz \times V_{RIPPLE})]$$

Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect directly to GND.

Charge-Pump Input Capacitor

Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the SUP pin as possible. Connect directly to GND.

Rectifier Diode

Use Schottky diodes with a current rating equal to or greater than 4 times the average output current, and a for the positive voltage rating at least 1.5 times V_{SUP} for the negative charge pump.

V_{COM} Amplifier

V_{COM} amplifier provides V_{COM} voltage for LCD monitor. Its main features are listed as follows: the V_{COM} amplifier is capable of ±100mA continuous output current, 45V/μs slew rate, 20 MHz -3dB bandwidth and rail to rail input/output voltage.

Limitation and Protection of Short-circuit Current

V_{COM} amplifier in EUP2681 has a more than 500mA short-circuit current limitation. The output current of OUT would be limited to around ±500mA to avoid chip damage caused by too large current by connecting OUT to power supply or ground.

Power Dissipation

The power dissipation of VCOM amplifier is mainly decided by the output current, output voltage and the power voltage; it can be calculated by following equation:

$$PD_{SOURCE} = I_{OUT(SOURCE)} \times (VDD\text{-}V_{OUT})$$

$$PD_{SINK} = I_{OUT(SINK)} \times V_{OUT}$$

Where the $I_{OUT(SOURCE)}$ is output current of the amplifier, the $I_{OUT(SINK)}$ is sink current of amplifier. Typically, the V_{COM} amplifier's power supply voltage (SUP) is 13V, output voltage is 3V, output current is 20mA and power dissipation is 200mW.

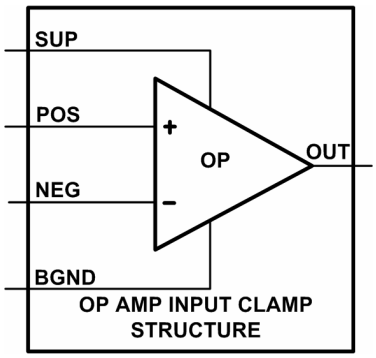


Figure 6. Op Amp Input Clamp Structure

The operational amplifier is typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

Reference Voltage (REF)

The reference voltage is nominally 1.25V, and can source at least 50μA (see the Typical Operating Characteristics).VCC is the input of the internal reference block. Bypass REF with a 1μF ceramic capacitor connected between REF and AGND. The greater bypass capacitor is, more stable REF is.

HV-Switch Circuit

The HV-Switch is used for LCD applications in which shaping of the gate high voltage signal improves image quality.

The HV-Switch circuit functions as three ways multiplexer, switching COM between ground, AVDD and SRC. Voltage selection is provided by inputs DEL (enable) and CTL (control). High to low slew control is provided by external components on pins DRN. A block diagram of the HV-Switch circuit is shown in following figure, the block is disabled and COM is grounded. When DEL is HIGH, the output is determined by CTL. When CTL goes high, COM is pulled to SRC by a 5Ω switch. When CTL goes low, COM is driven to AVDD, with a slew rate controlled by resistor on DRN pin. Note that AVDD is used only as a reference voltage for HV-Switch.

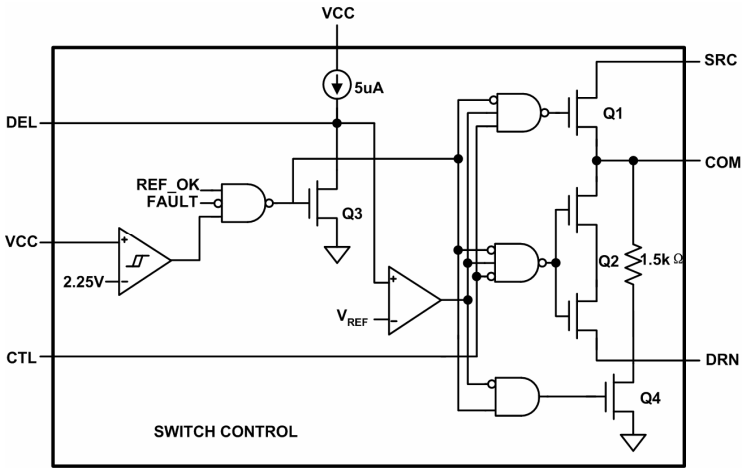


Figure 7. Switch Control

XAO Voltage Detector

Based upon the input at the RSTIN and VCC pins, the XAO controller either pulls the reset pin RST low or sets it to high impedance. RST is an open-drain output. Pull it high to system 3.3V through a 10kΩ resistor. Connect through resistor-dividers R11 and R12 RSTIN to VIN (Figure 1) to set the proper XAO threshold. Once VCC voltage exceeds approximately 2.25V, the controller initiates a 220ms blanking period during which the drop on VCC is ignored and RST is set to high impedance. After this blanking period and if RSTIN goes below approximately 1.25V, RST is pulled low indicating low RSTIN input. RST stays low until VCC falls below approximately 1V. Then RST cannot be held low any more. The controller gives up and RST is pulled up by the external resister. A 50mV hysteresis is implemented for XAO threshold.

Start Up Sequence

The soft-start is motivated by internal digital soft-start, which is generated by 7 byte DAC circuit. The MOSFET peak current is limited by the soft-start circuit. Once the VCC pin exceeds approximately 2.25V, the soft-start initiates.

Once the voltage on VCC exceeds the XAO UVLO threshold of approximately 1.5V, the reference turns on with a 1μF REF bypass capacitor, the reference reaches its regulation voltage of 1.25V in approximately 1ms. When the reference voltage exceeds 1V and VCC exceeds its UVLO threshold of approximately 2.25V, the IC enables the main step-up regulator, the gate-on linear-regulator

controller, and the gate-of linear-regulator controller simultaneously.

The IC employs soft-start for each regulator to minimize inrush current and voltage overshoot and to ensure a well-defined startup behavior. Each output uses a 7-bit soft-start DAC. For the step-up and the gate-on linear regulator, the DAC output is stepped in 128 steps from zero up to the reference voltage. For the gate-off linear regulator, the DAC output steps from the reference down to 250mV in 128 steps. The soft-start duration is 10ms (typ) for step-up regulator and 3ms (typ) for gate-on and gate-off regulators.

A capacitor (C_{DEL}) switch control blocks startup delay. After the input voltage exceeds the UVLO threshold (2.25V typ) and the soft-start routine for each regulator is complete and there is no fault detected, a 5μA current source starts. Once the capacitor voltage exceeds DEL charging CDEL 1.25V (typ), the switch-control block is enabled as shown in Figure 8. After the switch-control block is enabled, COM can be connected to SRC or DRN through the internal p-channel switches, depending upon the state of CTL. Before startup and when VCC is less than UVLO, DEL is internally connected to AGND. Select C_{DEL} to set the delay time using the following equation:

$$C_{DEL} = DELAY\_TIME \times \frac{5\mu A}{1.25V}$$

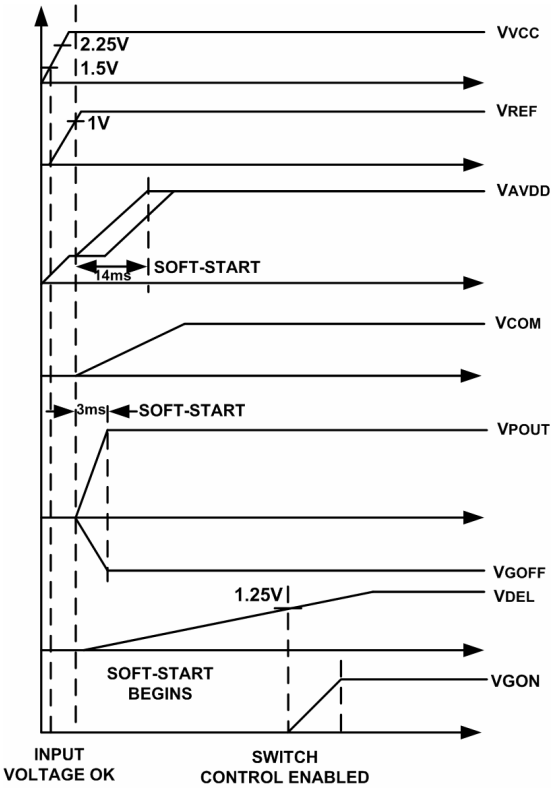


Figure 8. Start Up Sequence

Under-Voltage Lockout (UVLO)

The UVLO circuit compares the input voltage at VCC with the VULO threshold (2.25V rising , 2.05V falling, typ) to insure the input voltage is high enough for reliable operation . The 200 mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins.

When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and disable the switch-control block, the operational amplifier output is high impedance.

Fault Protection

EUP2681 has over-current protection and over-temperature protection. When the chip working, integrated over-temperature protection circuit continuous detects the chip temperature, and the chip would be turn off if the chip temperature exceed the over-temperature protection threshold. (the over-temperature protection's high and low threshold are 160°C and 140°C respectively).

During steady-state operation, if the output of the main regulator or any of the outputs exceeds their respective fault-detection thresholds, the EUP2681 activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault-timer duration (50ms typ), the EUP2681 sets the fault latch to shut down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

PCB Layout

To obtain high performance including good regulation, high efficiency and stability, high power switching supply, a good PCB layout is expected. The PCB layout must be evaluated strictly. Power element should be placed as close as possible ensuring the traces are short, straight and wide. Put power element together enough, and connect them by using asteroid in the element layer, then connect the asteroid to external Ground using some vias. Do not connect the GND pin of power element to external Ground. There are some general guidelines for layout:

- Put inductors, output diodes and output capacitances beside input capacitor，LX and PGND to minimize the circle area of high-current. The input loop of high-current begins with positive of input capacitor, sequentially through an inductor, the LX pin and PGND, finally reaches the negative of capacitor. And the output loop of high-current is consisted with the positive of input capacitor, through the inductor and the output terminal of diode and the positive of output capacitor for reconnecting the GND of output capacitor with the GND of input capacitor .Keep these traces shot and wide. Meanwhile, avoid using

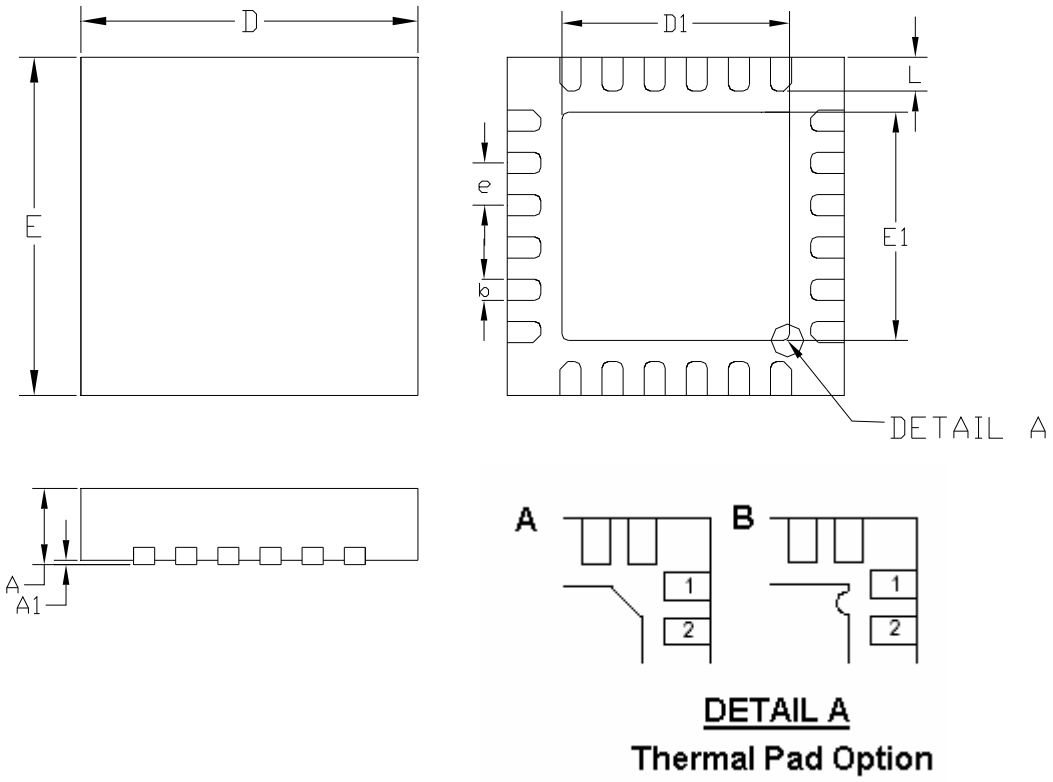
via in the circle area of high-current, otherwise, put via parallel to reduce resistance and inductance.

- Put all the feedback resistances within the 5mm scope of the corresponding feedback pin of them and keep the traces short enough to avoid switching noise. Keep feedback traces as close as possible to LX prevent a shield come into being.
- Put the bypass capacitances as close as possible to VIN and LVIN, the GND pin of bypass capacitances should be connected to the AGND pin using wide trace.
- Keep the traces between output capacitance and load as short and wide as possible to get a best transient response.

Keep the node area of LX least in the condition of insuring it is as short and wide as possible. Insure the node of LX far away from feedback node (FB) and AGND. Shield LX with DC traces if needed.

Packaging Information

TQFN-24



Note: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
E	3.90	4.00	4.10	0.154	0.157	0.161
D	3.90	4.00	4.10	0.154	0.157	0.161
D1	2.50	2.70	2.85	0.098	0.110	0.112
E1	2.50	2.70	2.85	0.098	0.110	0.112
e	0.50 REF			0.020 REF		
L	0.30	0.40	0.50	0.012	0.016	0.020