Multi-Output Power Supplies for TV TFT LCD Panels

DESCRIPTION

The EUP2683 generates all the four supply rails for thin-film transistor liquid-crystal display (TFT LCD) TV panels operating from a regulated 12V input. They include a step-down and a step-up regulator, a positive and a negative charge pump.

The step-up and step-down switching regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. The step-up regulator provides TFT source driver supply voltage, while the step-down regulator provides the system with logic supply voltage. Both regulators use fixed-frequency current-mode control architectures, providing fast load-transient response and easy compensation. The positive and negative charge-pump regulators provide TFT gate-driver supply voltages. Both output voltages can be adjusted with external resistive voltage-dividers. Both switching regulators and both charge pumps operate from a central clock that can be set to either 750 kHz or 500 kHz by tying the FREQ pin high or low.

The EUP2683 features adjustable power-up sequencing, step-up regulator over voltage protection, step-down regulator short-circuit protection, and over temperature protection to ensure in safe operating. The device also incorporates a gate drive signal to control an external MOSFET isolation switch connected in series with V_S or V_{GH}.

FEATURES

- 8V to 14.7V In Input Voltage Range
- Selectable Frequency (500kHz/750kHz)
- Current-Mode Step-Up Regulator
  - Built-In 20V, 3.7A, 100mΩ MOSFET
- Current-Mode Step-Down Regulator
  - Built-In 20V, 2.3A, 175mΩ MOSFET
- 100mA Charge Pump Output Current
- Negative Charge Pump Driver for V_{GL}
- Positive Charge Pump Driver for V_{GH}
- Adjustable Sequencing for V_{GL} and V_{GH}
- Gate Drive Signal to Drive External MOSFET
- Internal and Adjustable Soft Start
- Short-Circuit Protection
- Over voltage Protection
- Thermal Shutdown
- Available in TSSOP-28 (EP) Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATIONS

- TFT LCD Displays for Monitor and LCD TV

Typical Application Circuit

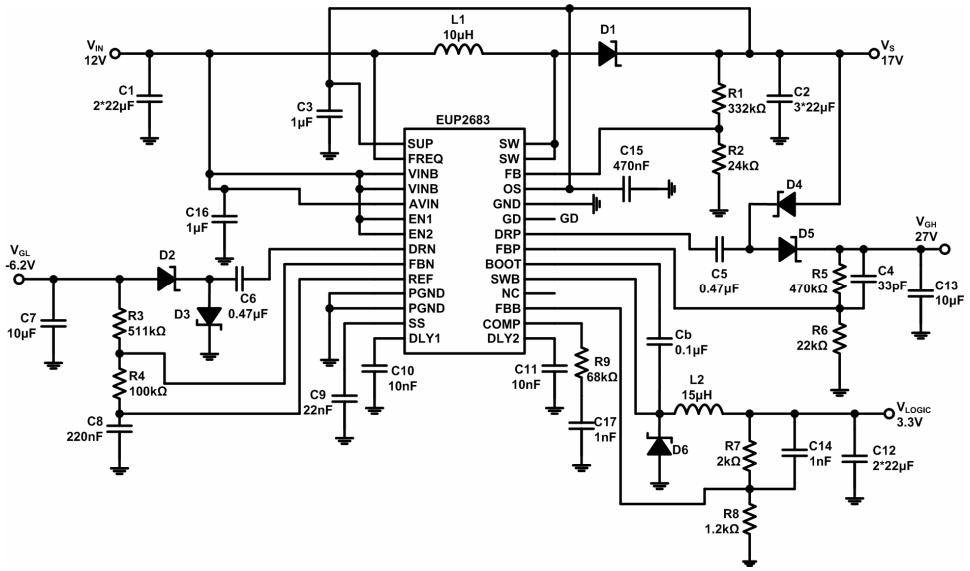
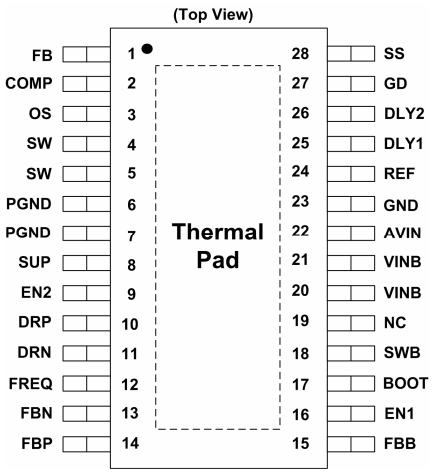


Figure 1. Typical Application Circuit

Pin Configurations

Package Type	Pin Configurations
TSSOP-28 (EP)	

Note: Recommend connecting the Thermal Pad to the PGND for excellent power dissipation.

Pin Description

PIN	TSSOP-28 (EP)	DESCRIPTION
1	FB	Feedback of the main step-up regulator generating Vsource (V_S).
2	COMP	This is the compensation pin for the Step-up regulator.
3	OS	Output sense pin. The OS pin is connected to the internal rectifier switch and overvoltage protection comparator. This pin needs to be connected to the output of the step-up regulator and cannot be connected to any other voltage rail. Connect a 470nF capacitor from OS pin to GND to avoid noise coupling into this pin.
4,5	SW	Switch pin of the Step-up regulator generating Vsource (V_S).
6,7	PGND	Power ground.
8	SUP	This is the supply pin of the positive charge pump driver and can be connected to the input supply V_{IN} or the output of the main step-up regulator V_S. This depends mainly on the desired output voltage V_{GH} and numbers of charge pump stages.
9	EN2	The step-up regulator starts only with EN1 = high, after the step-down regulator is enabled. EN2 is the enable pin of the step-up regulator and positive charge pump. When this pin is pulled high, the step-up regulator and positive charge pump starts up after the step-down regulator is within regulation and a delay time set by DLY2 has passed by. This pin must be terminated and not be left floating.
10	DRP	Drive pin of the positive charge pump.
11	DRN	Drive pin of the negative charge pump.
12	FREQ	Frequency adjust pin. This pin allows setting the switching frequency with a logic level to 500 kHz = low and 750 kHz = high.
13	FBN	Feedback pin of negative charge pump.
14	FBP	Feedback pin of positive charge pump.
15	FBB	Feedback pin of the step-down regulator.
16	EN1	This is the enable pin of the step-down regulator and negative charge pump. When this pin is pulled high, the step-down regulator starts up, and after a delay time set by DLY1, the negative charge pump comes up. This pin must be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device.

Pin Description (continued)

PIN	TSSOP-28 (EP)	DESCRIPTION
17	BOOT	N-channel MOSFET gate drive voltage for the step-down regulator. Connect a capacitor from the switch node SWB to this pin.
18	SWB	Switch pin of the step-down regulator.
19	NC	Not connected.
20,21	VINB	Power input voltage pin for the step-down regulator. A 22µF capacitor needs to be connected to this pin within 5mm.
22	AVIN	Analog input voltage of the device. This is the input for the analog circuits of the device and should be bypassed with a 1µF ceramic capacitor for good filtering.
23	GND	Analog ground.
24	REF	Internal reference output typically 1.213V. A 220-nF capacitor needs to be connected to this pin.
25	DLY1	Connecting a capacitor from this pin to GND allows the setting of the delay time between $V_{(LOGIC)}$ (step-down regulator output high) to V_{GL} during start-up.
26	DLY2	Connecting a capacitor from this pin to GND allows the setting of the delay time between $V_{(LOGIC)}$ (step-down regulator output high) to V_S step-up regulator and positive charge-pump V_{GH} during start-up.
27	GD	This is the gate drive pin which can be used to control an external MOSFET switch to provide input to output isolation of V_S or V_{GH}. GD is an open-drain output and is latched low as soon as the step-up regulator is within 8% of its nominal regulated output voltage. GD goes high impedance when the EN2 input voltage is cycled low.
28	SS	This pin allows setting the soft-start time for the main step-up regulator V_S. Typically a 22nF capacitor needs to be connected to this pin to set the soft-start time.
Thermal Pad		The thermal Pad needs to be connected and soldered to power ground (PGND).

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP2683XIR1	TSSOP-28 (EP)	xxxxx EUP2683	-40 °C to 85°C

EUP2683 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  X: TSSOP-28 (EP)

Functional Block Diagram

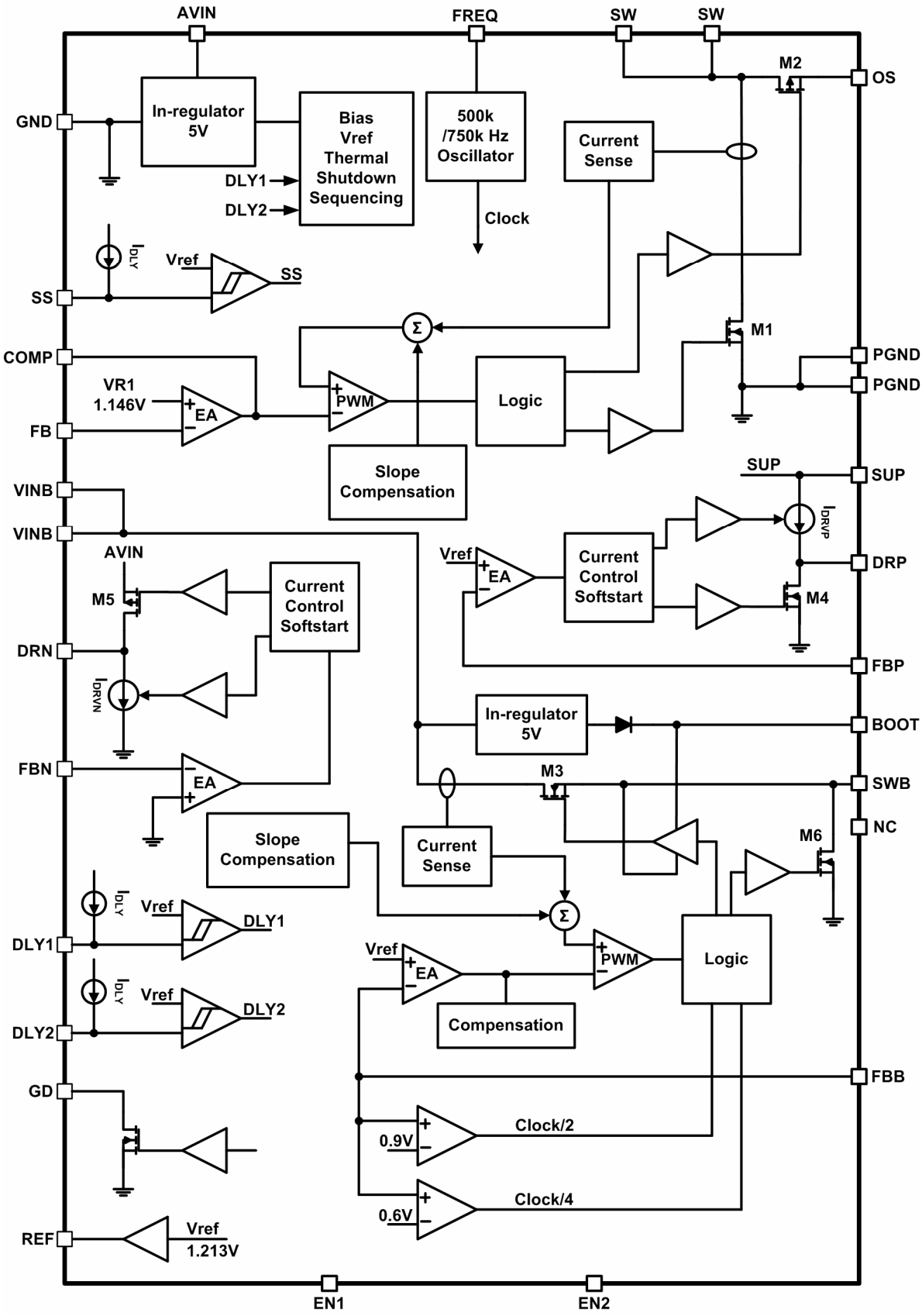


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (1)

- AVIN, VINB, EN1, EN2, FREQ ---------- -0.3V to 16.5V
- SW, OS, SWB, SUP, GD ---------- 20V
- BOOT ---------- SWB-0.3V to SWB+6V
- DRN ---------- -0.3V to AVIN+0.3V
- DRP ---------- -0.3V to SUP+0.3V
- All Other Pins ---------- -0.3V to 6V
- Continuous Power Dissipation (T_A= +70°C)
  28-Pin TSSOP (derate 29.4mW/°C above +70°C) ---------- 2353mW
- Junction Temperature ---------- +150°C
- Storage Temperature Range ---------- -65°C to +160°C
- Lead Temp (Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} (TSSOP-28_EP) ---------- 34°C/W

Recommend Operating Conditions (2)

- AVIN, VINB ---------- 8V to 14.7V
- Operating Temperature Range ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

V_{IN}=12V, SUP=V_{IN}, EN1=EN2=V_{IN}, V_S =15V, V_{LOGIC}=3.3V, T_A = –40 ºC to 85 ºC, typical values are at T_A=25 ºC (unless otherwise noted)

Symbol	Parameter	Conditions	EUP2683			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
V_{IN}	Input voltage range		8		14.7	V
I_Q	Quiescent current into AVIN	V_{GH} = 2 × V_S, Step-up regulator not switching		1	2	mA
	Quiescent current into VINB	V_{GH} = 2 × V_S, Step-down regulator not switching		0.4	1	mA
I_{SD}	Shutdown current into AVIN	EN1 = EN2 = GND		1	5	µA
	Shutdown current into VINB	EN1 = EN2 = GND		0.1	2	µA
I_{SUP}	Shutdown current into SUP	EN1 = EN2 = GND		0.1	4	µA
	Quiescent current into SUP	V_{GH} = 2 × V_S		0.2	2	mA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		8	8.8	V
V_{ref}	Reference voltage		1.195	1.213	1.231	V
	Thermal shutdown	Temperature rising		155		ºC
	Thermal Shutdown Hysteresis			20		ºC
LOGIC SIGNALS EN1, EN2, FREQ						
V_{IH}	High-level input voltage EN1, EN2		2.0			V
V_{IL}	Low-level input voltage EN1, EN2				0.8	V
V_{IH}	High-level input voltage FREQ		1.7			V
V_{IL}	Low-level input voltage FREQ				0.4	V
I_{leak}	Input leakage current	EN1 = EN2 = FREQ = GND or V_{IN}		0.5	1	µA

Electrical Characteristics (continued)

V_{IN}=12V, SUP=V_{IN}, EN1=EN2=V_{IN}, V_S =15V, V_{LOGIC}=3.3V, T_A = –40 ℃ to 85 ℃, typical values are at T_A=25 ℃ (unless otherwise noted)

Symbol	Parameter	Conditions	EUP2683			Unit
			Min.	Typ.	Max.	
CONTROL AND SOFT START DLY1, DLY2, SS						
I_{DLY1}	Delay1 charge current	$V_{THRESHOLD}$ = 1.213V	3.3	4.8	6.2	μA
I_{DLY2}	Delay2 charge current		3.3	4.8	6.2	μA
I_{SS}	SS charge current		6	9	12	μA
f_{OSC}	Oscillator frequency	FREQ = high	600	750	900	kHZ
		FREQ = low	400	500	600	kHZ
STEP-UP REGULATOR (V_S)						
V_S	Output voltage range(3)				19	V
V_{FB}	Feedback regulation voltage		1.123	1.146	1.169	V
I_{FB}	Feedback input bias current			10	100	nA
R_{DSON}	N-MOSFET on-resistance (M1)	I_{SW} = 500mA		100	185	mΩ
	P-MOSFET on-resistance (M2)	I_{SW} = 200mA		10	16	Ω
I_{MAX}	Maximum P-MOSFET peak switch current				1	A
I_{LIM}	N-MOSFET switch current limit (M1)		3.7	4.6	5.5	A
I_{leak}	Switch leakage current	V_{SW} = 15V		1	10	μA
OVP	Overvoltage protection	V_{OUT} rising	19.5	20	21	V
	Line regulation	10.6V≤V_{IN}≤11.6V at 1mA		0.0008		%/V
	Load regulation			0.03		%/A
GATE DRIVE (GD)						
V_{GD}	Gate drive threshold(4)	V_{FB} rising	V_S-12%	V_S-8%	V_S-4%	V
V_{OL}	GD output low voltage	I_{sink} = 500μA			0.3	V
	GD output leakage current	V_{GD} = 20V		0.05	1	μA
STEP-DOWN REGULATOR (V_{LOGIC})						
V_{LOGIC}	Output voltage range		1.8		5	V
V_{FBB}	Feedback regulation voltage		1.189	1.213	1.237	V
I_{FBB}	Feedback input bias current			10	100	nA
R_{DSON}	High side N-MOSFET on-resistance (M3)	I_{SW} = 500mA		175	300	mΩ
	Low side N-MOSFET on-resistance (M6)	I_{SW} = 200mA		10	16	Ω
I_{LIM}	N-MOSFET switch current limit (M3)		2.5	3.2	3.9	A
I_{leak}	Switch leakage current	EN1=0,V_{SW} = 0V		1	10	μA
	Line regulation	10.6V≤V_{IN}≤11.6V at 1mA		0.0018		%/V
	Load regulation			0.037		%/A

Electrical Characteristics (continued)

V_{IN}=12V, SUP=V_{IN}, EN1=EN2=V_{IN}, V_S =15V, V_{LOGIC}=3.3V, T_A = –40 ºC to 85 ºC, typical values are at T_A=25 ºC (unless otherwise noted)

Symbol	Parameter	Conditions	EUP2683			Unit
			Min.	Typ.	Max.	
NEGATIVE CHARGE-PUMP V_{GL}						
V_O	Output voltage range				-2	V
V_{FBN}	Feedback regulation voltage		-36	0	36	mV
I_{FBN}	Feedback input bias current			10	100	nA
R_{DSON}	M5 P-Channel switch R_{DSON}	I_{OUT} = 20mA		3.7		Ω
V_{DropN}	Current sink voltage drop (5)	I_{DRN} = 100mA, V_{FBN}=V_{FBN} nominal -5%		0.24	0.42	V
		I_{DRN} =200mA, V_{FBN}=V_{FBN} nominal -5%		0.52	0.90	V
POSITIVE CHARGE-PUMP OUTPUT V_{GH}						
V_{FBP}	Feedback regulation voltage		1.189	1.213	1.237	V
I_{FBP}	Feedback input bias current			10	100	nA
R_{DSON}	M4 N-Channel switch R_{DSON}	I_{OUT} = 20mA		1.1		Ω
V_{DropP}	Current source voltage drop (V_{SUP} – V_{DRP}) (6)	I_{DRP} = 100mA, V_{FBP}=V_{FBP} nominal -5%		0.63	1.60	V
		I_{DRP} = 200mA, V_{FBP}= V_{FBP} nominal -5%		1.40	3.20	V

Note (3): The maximum output voltage is limited by the overvoltage protection threshold and not be the maximum switch voltage rating.

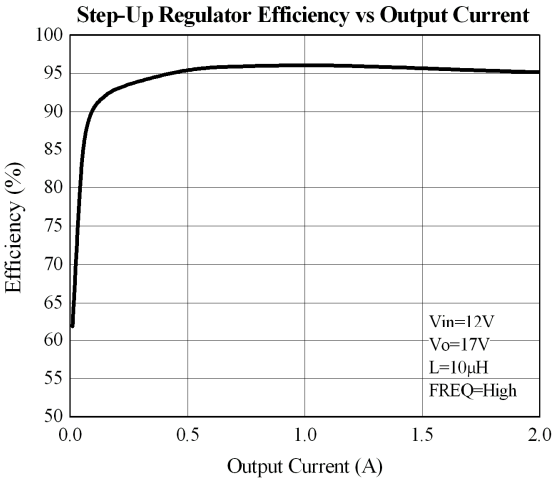
Note (4): The GD signal is latched low when the main step-up regulator output V_S is within regulation. The GD signal is reset when the input voltage or enable of the step-up regulator is cycled low.

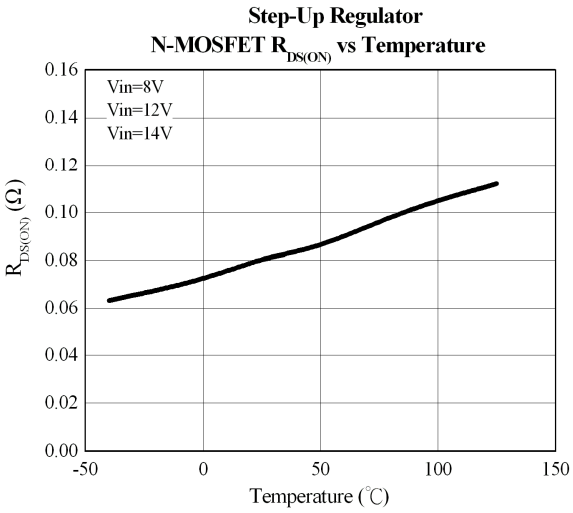
Note (5): The maximum charge-pump output current is typically half the drive current of the internal current source or current sink.

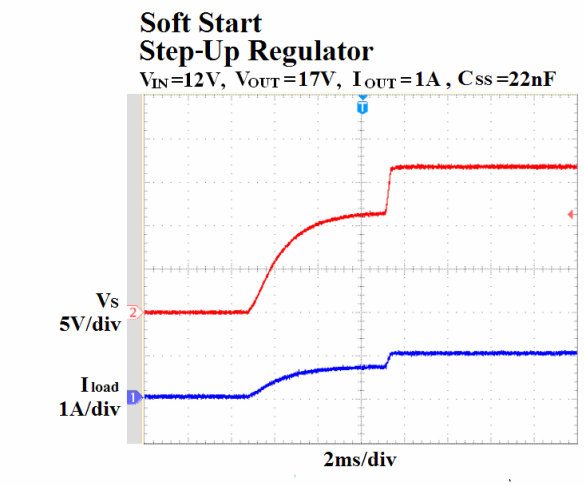
Note (6): The maximum charge-pump output current is typically half the drive current of the internal current source or current sink.

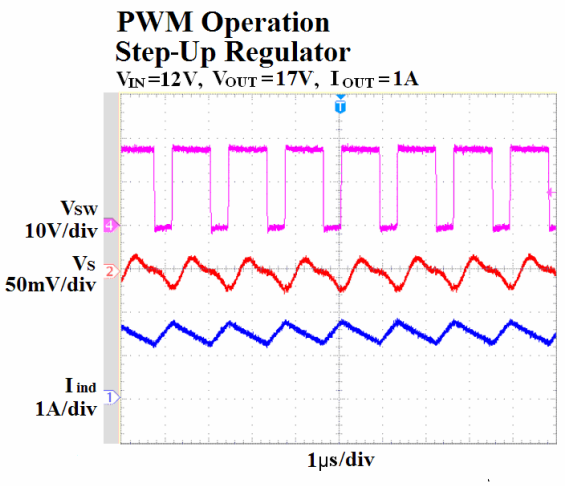
Typical Operating Characteristics

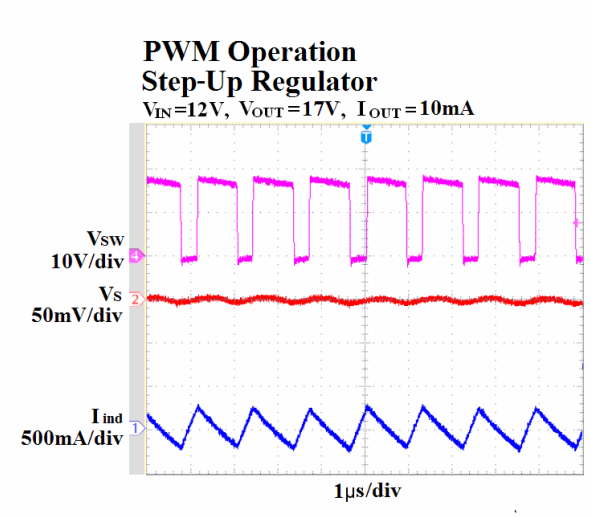
V_{IN}=12V, V_S=17V, V_{LOGIC}=3.3V, V_{GL}=-6.2V, V_{GH}=27V, FREQ=High, L1=10µH, L2=15µH, T_A=25 °C, unless otherwise noted.

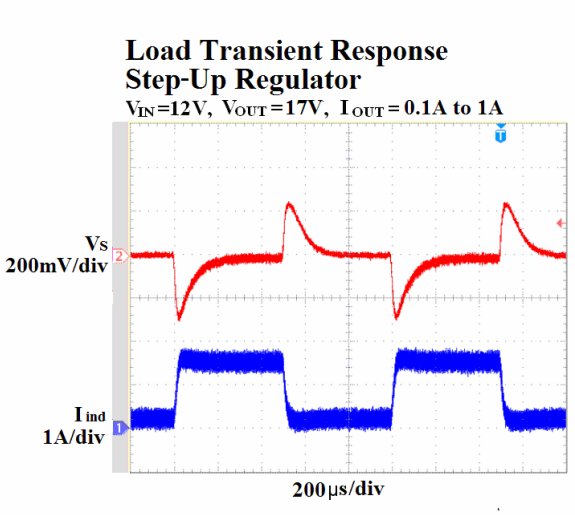






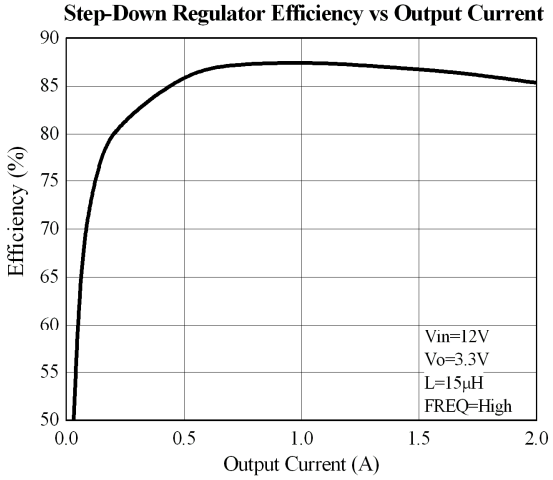




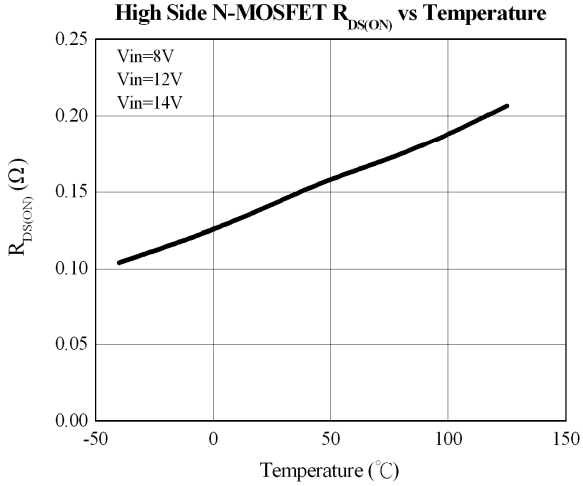


Typical Operating Characteristics (continued)

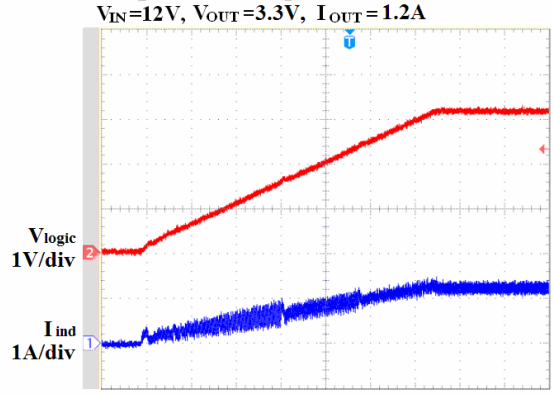
Step-Down Regulator Efficiency vs Output Current



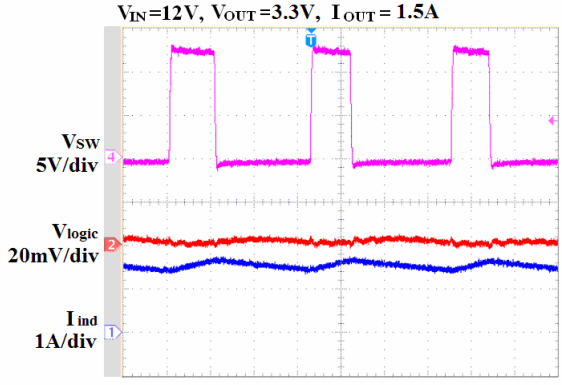
Step-Down Regulator
High Side N-MOSFET $R_{DS(ON)}$ vs Temperature



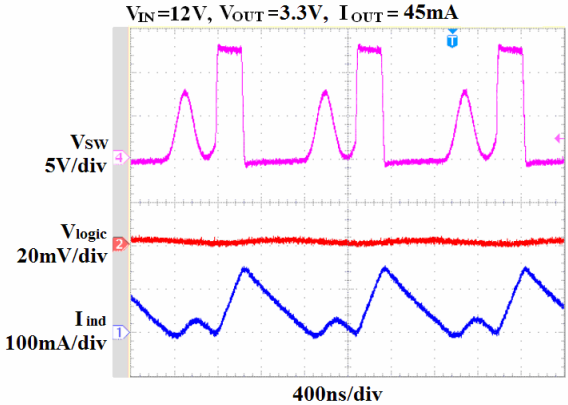
Soft Start
Step-Down Regulator
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=1.2A



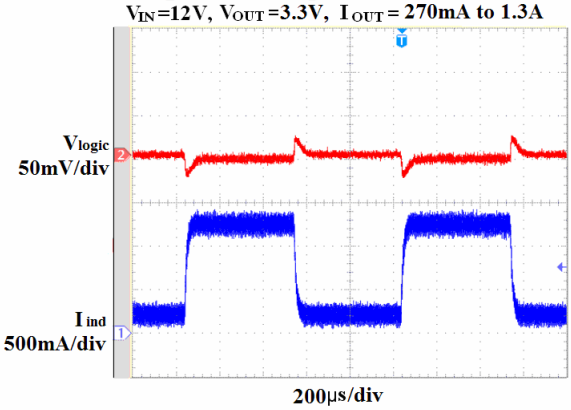
PWM Operation CCM
Step-Down Regulator
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=1.5A



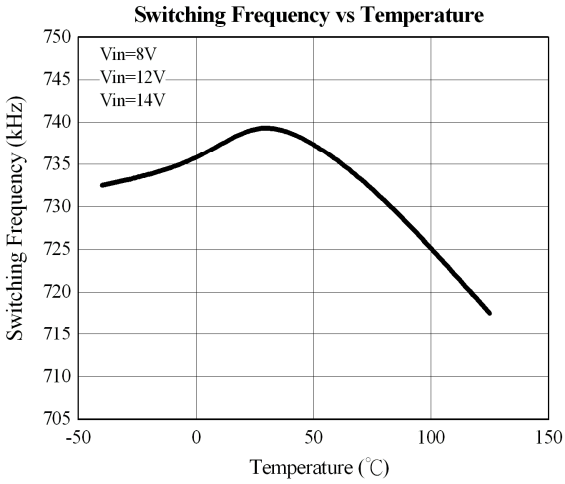
PWM Operation DCM
Step-Down Regulator
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=45mA

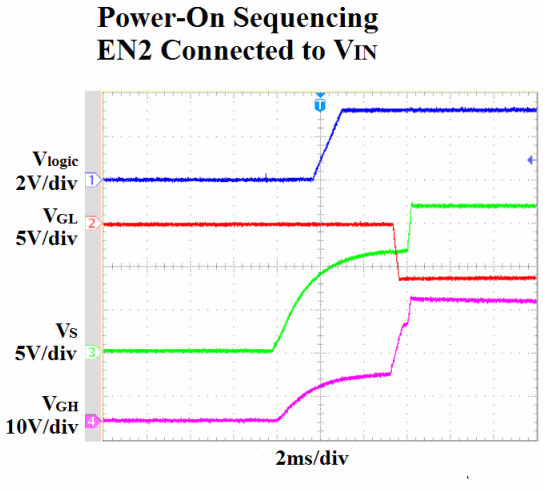


Load Transient Response
Step-Down Regulator
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=270mA to 1.3A



Typical Operating Characteristics (continued)





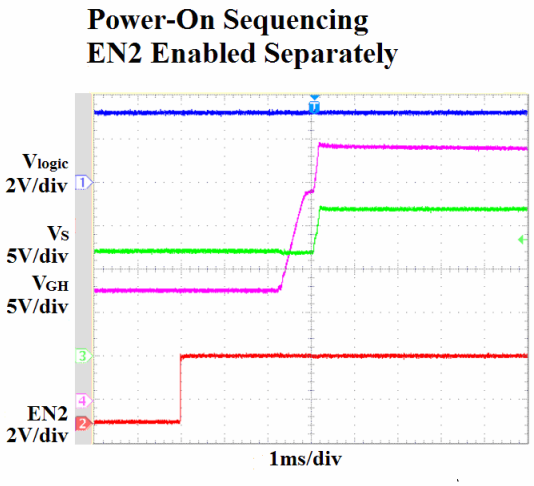


Table 1. Component List (Figure 1)

Designation	Description
C1	2×22μF, 16V, X5R ceramic capacitors
C2	3×22μF, 25V, X5R ceramic capacitors
C3, C16	1μF, 25V, X7R ceramic capacitors
C4	33pF, 50V, X7R ceramic capacitor
C5, C6, C15	0.47μF, 50V, X7R ceramic capacitors
C7, C13	10μF, 35V, X5R ceramic capacitors
C8	220nF, 6.3V, X7R ceramic capacitor
C9	22nF, 50V, X7R ceramic capacitor
C10, C11	10nF, 50V, X7R ceramic capacitors
C12	2×22μF, 6.3V, X5R ceramic capacitor
C14	1nF, 50V, X7R ceramic capacitor
D1, D6	Schottky diodes 30V, 3A DIODES B330A
D2-D3, D4-D5	Dual diodes 30V, 200mA(3 SOT23) Zetex BAT54S Fairchild BAT54S
L1	Inductor, 10μH, 3A/50mΩ
L2	Inductor, 15μH, 3A/50mΩ

Function Description

The EUP2683 contains a high performance current mode step-up regulator, a step-down regulator, a gate-on charge pump driver, and a gate-off charge pump driver. The following content contains the detailed description and the information of the component selection.

Step-Up Regulator

The step-up regulator is a high efficiency current-mode PWM architecture with operation frequency of 500KHz or 750KHz set by the FREQ pin. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components to minimize the thickness of LCD panel. The Step-up regulator can operate in continuous conduction mode even at light load current, which is achieved with a novel architecture using an external Schottky diode with an integrated MOSFET in parallel connected between SW and OS. In the first half cycle, the power MOSFET is on and Schottky diode are reverse biased, the output current is provided by output capacitor, inductor voltage is V_{IN}, and its current increase at the rate of V_{IN}/L; during the other half cycle, MOSFET is off and Schottky diodes are forward biased, the energy stored in the inductor is released. The inductor current ripple is:

$$\Delta I_L = \Delta T_2 \times \frac{V_{IN} - V_{OUT}}{L}$$

$$\Delta T_2 = \frac{1-D}{F_{SW}}$$

Where L is self-inductance, the energy of inductor is stored by electromagnetic induction.

In the steady state operation, the energy stored in inductor must be converted equally, so the inductor current ripples in two half cycle are identical.

$$\frac{D}{F_{SW}} \times \frac{V_{IN}}{L} + \frac{1-D}{F_{SW}} \times \frac{V_{IN} - V_{OUT}}{L} = 0$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

Soft start

The step-up regulator has an adjustable soft start to prevent high inrush current during start-up. The soft start time is set by the external capacitor connected to the SS pin. The capacitor is charged with a constant current that increases the SS pin voltage. The larger the soft start capacitor value, the longer the soft start time.

Overvoltage Protection

The step-up regulator has an overvoltage protection to protect the main switch M1 at pin SW in case the feedback pin FB is floating or shorted to GND. The output voltage is monitored with the overvoltage protection comparator over the OS pin. As soon as the comparator trips at typically 20V, the step-up regulator turns the N-Channel MOSFET switch off. The output voltage falls below the overvoltage threshold and the regulator continues to operate.

Output Voltage

The output voltage is reduced to a reference voltage 1.146V by external feedback resistor divider. The resistors maximum value is limited by feedback output biased current and potential coupling noise of feedback pin.

Output voltage of Step-up Regulator can be set according to the following equations:

$$V_S = 1.146V \times \left(1 + \frac{R1}{R2}\right)$$

Place the resistor divider as close as possible to the chip can reduce noise sensitivity.

Inductor Selection

The output voltage ripple, transient response, capacity and efficiency of output current supply are decided by inductor selection and the inductor value is influenced by input and output voltage, switching frequency and the maximum output current. The EUP2683 operates typically with a 10uH inductor. Other possible inductor values are 6.8μH or 22μH. The saturation current of the selected inductor should be higher than the peak switch current.

Output Capacitor Selection

Small value of ESR capacitor can minimum the output voltage ripple. So it is recommended that multi-layer ceramic capacitors（X5R or X7R）are used to be output

capacitor because of its low ESR characteristics and small size in package. ESR determines the output voltage ripple according to the equation:

$$\Delta V_O = \frac{I_O \times D}{F_{SW} \times C_O} + I_O \times ESR$$

Diode Selection

Schottky diodes, with their low forward voltage drop and fast reverse recovery, are the ideal choices for EUP2683 applications. It must be chosen correctly depending on some parameters such as reverse breakdown voltage, forward current and forward voltage drop. A Schottky diode rated at 3A is sufficient for most EUP2683 applications.

Input Capacitor Selection

Input capacitors, which are decided by input and output voltage, maximum output current, inductor and supply noise, are important in restraining input voltage ripple and enhancing chip performance. In most application, a 22μF capacitor is suitable. Care must be taken to make sure that chip is normal operated, a 10Ω resistor and a 1μF bypass capacitor should be taken next to the V_{IN} pin to decrease the high frequency noise of power wire.

Loop Compensation

The feedback loop of EUP2683 contains a trans-conductance amplifier, which makes the chip achieve better transient response and regulation. The EUP2683 employs current mode control architecture, which features rapid current sense loop and slow voltage feedback loop. Compensation is not required for rapid current sense loop but is necessary for slow voltage feedback loop to insure that the device is in the steady state. RC network connected between the COMP pin and AGND is a compensation network. In the network, resistors play a decisive role in achieving a high gain of high-frequency and obtain fast transient response. Capacitor sets the zero of the integrator. Assuring about loop stabilization, capacitor must be chosen between 220pF~10nF and resistor must be chosen accurately in the range of 2kΩ ~100kΩ.

Step-Down Regulator

The nonsynchronous step-down regulator operates at a fixed switching frequency of 500kHz or 750kHz set by the FREQ pin. The step-down regulator uses peak current mode architecture to control the regulator loop. The regulator uses an internal N-Channel MOSFET to step-down the voltage. Since the N-Channel switch requires gate driver voltage higher than SW, a bootstrap BOOT capacitor is connected between SW and BOOT to drive the N-Channel MOSFET.

Soft Start

An internal soft start is implemented in the step-down regulator to avoid high inrush current during start up. To further limit the inrush current during soft start, the feedback voltage is monitored by the comparator to control the switching frequency. The frequency is set to 1/4 of the normal switching frequency when feedback voltage FBB bellows 0.6V. The frequency is set to 1/2 of the normal switching frequency when feedback voltage FBB between 0.6V and 0.9V.

Short Circuit Protection

The device has a cycle-by-cycle current limit. To avoid the short-circuit current rising above the internal current limit when the output is shorted to GND, the switching frequency is reduced. The step-down regulator switching frequency is reduced to 1/2 of normal switching frequency when the feedback is below 0.9V and to 1/4 of the switching frequency when the feedback is below 0.6V.

Setting the Output Voltage

The output voltage is set through a resistor voltage divider. The output voltage is calculated as:

$$V_{LOGIC} = 1.213V \times (1 + \frac{R7}{R8})$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current and lower output ripple voltage. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions. A good rule for determining the inductance is to allow the peak-to- peak ripple current in the inductor to be approximately 30% of the maximum load current. Also, make sure that the peak inductor current (the load current plus half the peak-to-peak inductor ripple current) is below the 2A minimum peak current limit.

The inductance value can be calculated by the equation:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Input Capacitor

The input current to the step-down regulator is discontinuous, and therefore an input capacitor is required to supply the AC current to the step-down regulator while maintaining the DC input voltage. A low ESR capacitor is required to keep the noise minimum at the IC. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. The input capacitor value should be greater than 10μF, and the RMS current rating should be greater than approximately 1/2 of the DC load current. In Figure 1, all ceramic capacitors should be placed close to EUP2683.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. The characteristics of the output capacitor also affect the stability of the regulator control loop. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. For most application, two 22μF ceramic capacitors will be sufficient.

Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the switch is off. A schottky diode is recommended to reduce losses due to the diode forward voltage and recovery times. The reverse voltage rating of the diode should be greater than the maximum input voltage, and current rating should be greater than the maximum load current.

Dual Charge-Pump Regulator

The EUP2683 contain two individual low-power charge pumps. One charge pump inverts the supply voltage (SUP) and provides a regulated negative output voltage. The second charge pump doubles the supply voltage (SUP) and provides a regulated positive output voltage. The EUP2683 contain internal p-channel and n-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant 500 kHz/750 kHz.

Negative Charge Pump

During the first half-cycle, the p-channel MOSFET turns on and the flying capacitor C6 charges to AVIN minus a diode drop. During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting C7. This connects C6 in parallel with the reservoir capacitor C7. If the voltage across C7 minus a diode drop is higher lower than the voltage across C6, charge flows from C7 to C6 until the diode turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance. The output voltage of negative charge pump is set by:

$$V_{GL} = -1.213V \times \frac{R3}{R4}$$

Positive Charge Pump

During the first half-cycle, the n-channel MOSFET turns on and charges the flying capacitor C5 to the V_{OUT} voltage. During the second half-cycle, the n-channel MOSFET turns off and the p-channel MOSFET turns on to charge the DRVP pin up to the SUP voltage. At this cycle, C5 is connected in parallel with C13 and pumps the maximum output voltage to (VSUP+VOUT). The output voltage of positive charge pump is set by:

$$V_{GH} = 1.213V \times \left(1 + \frac{R5}{R6}\right)$$

Power-On Sequencing

The EUP2683 has an adjustable power on sequence set by the capacitor connected to DLY1 and DLY2 and controlled by EN1 and EN2. Pulling EN1 high enables the step-down regulator and then the negative charge-pump driver. The delay time between the step-down regulator and negative charge-pump driver is set by DLY1. EN2 enables the step-up regulator and positive charge-pump driver at the same time. The delay time between the step-down regulator and the step-up regulator is set by DLY2. This is especially useful to adjust the delay when EN2 is always connected to VIN. If EN2 goes high after the step-down regulator is already enabled, the delay DLY2 starts when EN2 goes high. See Figure 3 and Figure 4.

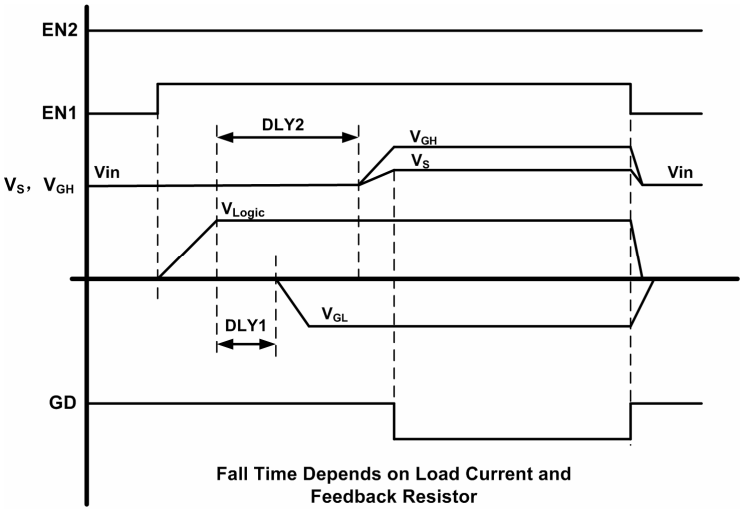


Figure 3. Power On Sequencing with EN2=Vin

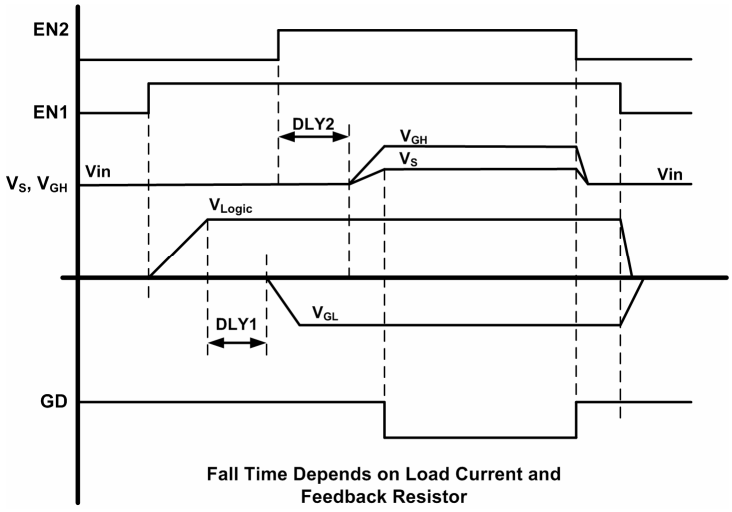


Figure 4. Power On Sequencing Using EN1 and EN2

Setting the Delay Times DLY1, DLY2

Connecting an external capacitor to the DLY1 and DLY2 pins sets the delay time. If no delay time is required, these pins can be left open. To set the delay time, the external capacitor connected to DLY1 and DLY2 is charged with a constant current source of typically 4.8μA. The delay time is terminated when the capacitor voltage has reached the internal reference voltage of V_{REF}=1.213V. The external delay capacitor is calculated:

$$C_{DLY} = \frac{4.8\mu A \times T_D}{1.213V}$$

Where T_D is desired delay time.

Frequency Selection

The frequency select pin (FREQ) allows setting the switching frequency of the entire device to 500 kHz (FREQ=low) or 750 kHz (FREQ=high). A lower switching frequency gives a higher efficiency with a slightly reduced load transient regulation.

Gate Drive Pin (GD)

This is an open-drain output that goes low when the step-up regulator, V_S, is within regulation. The gate drive pin GD remains low until the input voltage or enable EN2 is cycled to ground.

Undervoltage Lockout

To avoid incorrect operation of the device at low input voltages, an undervoltage lockout is included which shuts down the device at voltages lower than 8V.

Thermal Shutdown

A thermal shutdown is implemented to prevent damage caused by excessive heat and power dissipation. Typically, the thermal shutdown threshold is 155°C.

PCB Layout Consideration

To obtain high performance including good regulation, high efficiency and stability, high power switching supply, a good PCB layout is expected. Especially with a switching dc-dc regulator at high load currents, too-thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible, a common ground plane to minimize ground shifts between analog (GND) and power ground (PGND) is recommended. The PCB layout must be evaluated strictly. Power element should be placed as close as possible ensuring the traces short, straight and wide. Put power element together enough, and connect them by using asteroid in the element layer, then connect the asteroid to external Ground using some vias. Do not connect the GND pin of power element to external Ground. The following PCB layout guidelines are recommended:

1. Separate the power supply traces for AVIN and VINB, use separate bypass capacitors, and the bypass capacitors as close as possible to the device.
2. Keep the traces of the main current paths as short and wide as possible.
3. To minimize noise coupling into the OS pin, use a 470nF bypass capacitor to GND.
4. Use a short and wide trace to connect the OS pin to the output of the step-up regulator.
5. Place the rectifier diode of the step-down regulator as close as possible to the SWB pin.
6. Place a 1μF bypass capacitor from the SUP pin to GND.
7. Use short traces for the charge-pump drive pins (DRN, DRP) of V_{GH} and V_{GL} because these traces carry switching waveforms.
8. Place the flying capacitors as close as possible to the DRP and DRN pins, avoiding a high voltage spike at these pins.
9. Place the Schottky diodes as close as possible to the IC, respective to the flying capacitors connected to the DRP and DRN.
10. Route the feedback network of the negative charge pump away from the drive pin traces (DRN) of the negative charge pump. This avoids parasitic coupling into the feedback network of the negative charge pump giving good output voltage accuracy and load regulation. To do this, use the FREQ pin and trace to isolate DRN from FBN.

Application Information

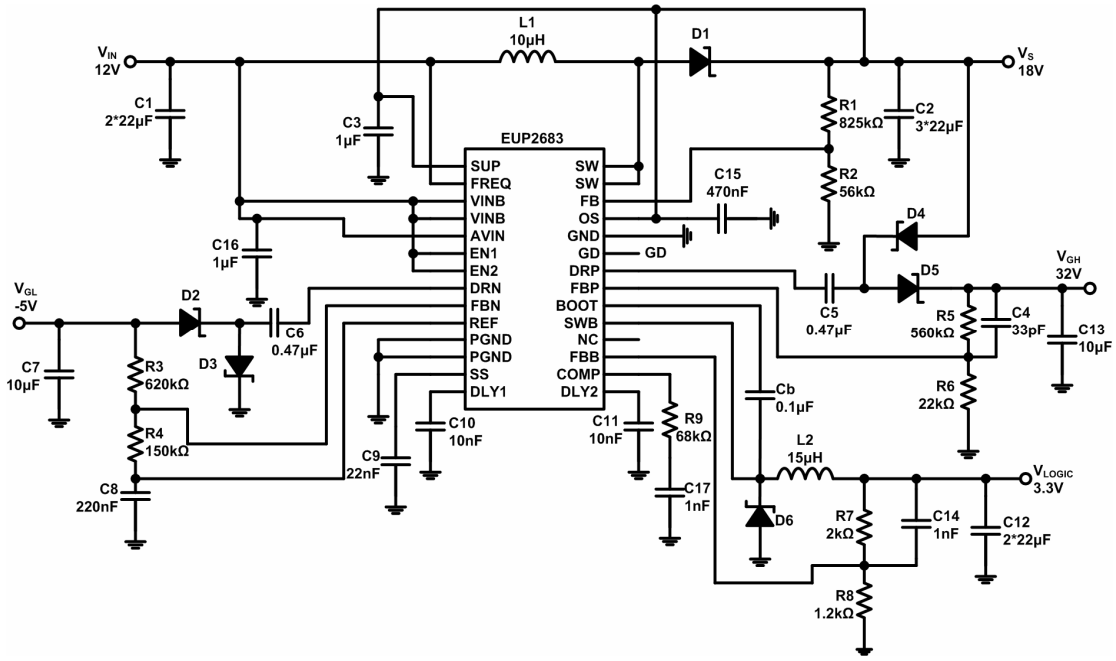


Figure 5. Standard 12V to 18V Conversion

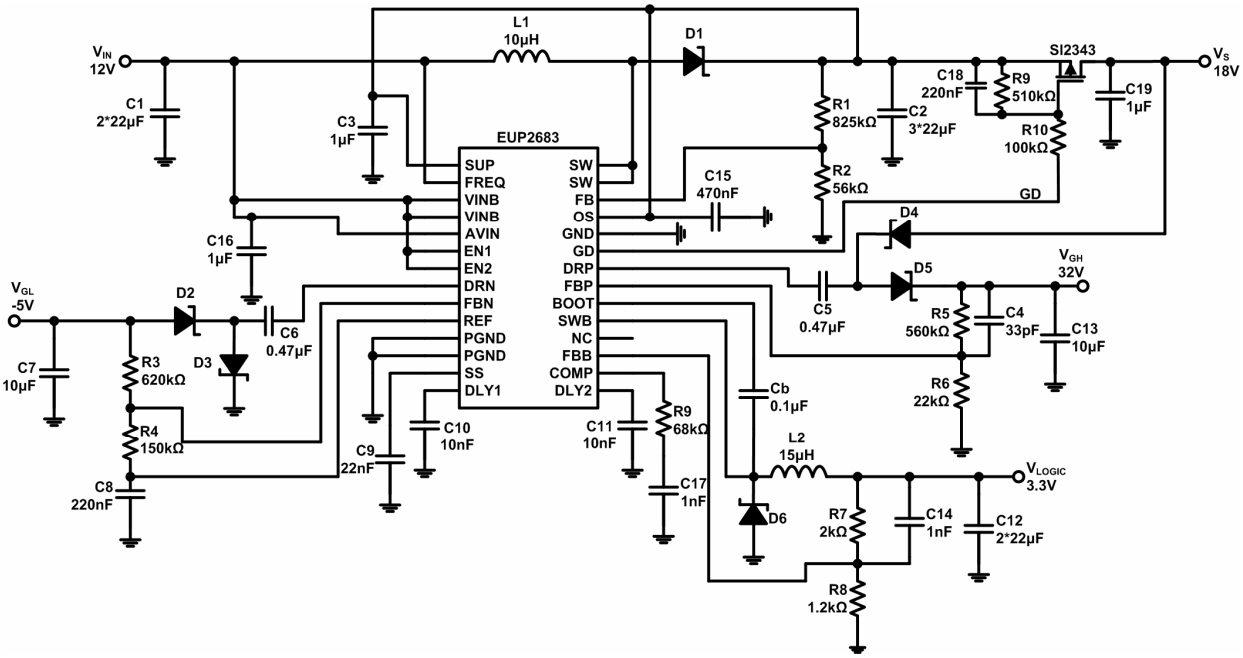


Figure 6. Standard 12V to 18V Conversion Using an External Isolation MOSFET to Isolate V_S as well as V_{GH}

Application Information (continued)

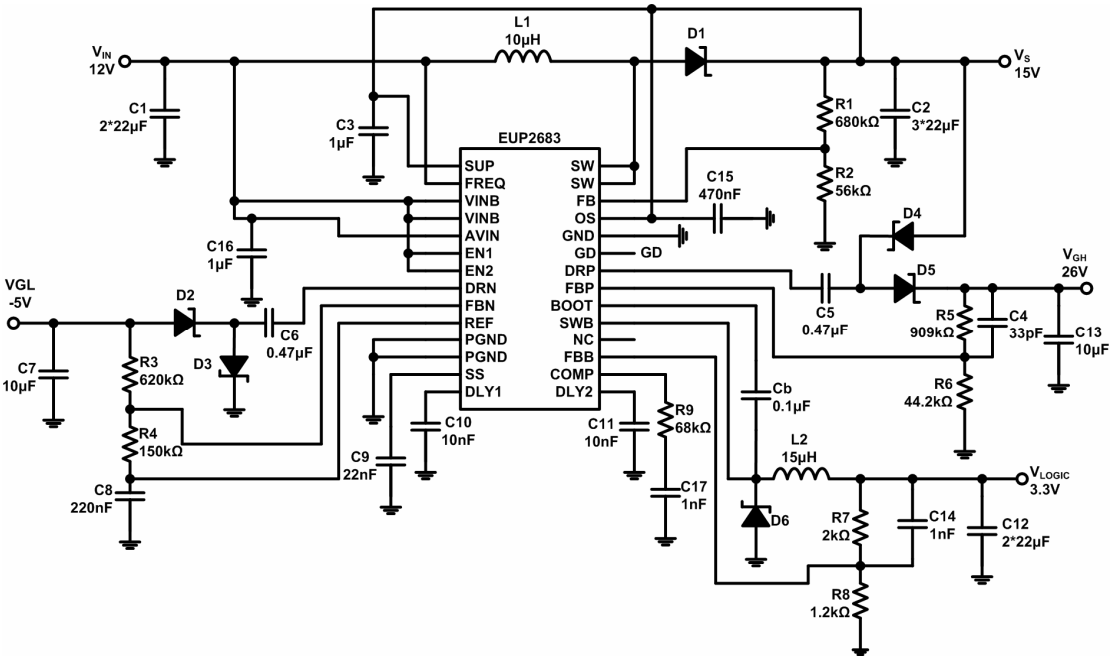


Figure 7. Standard 12V to 15V Conversion

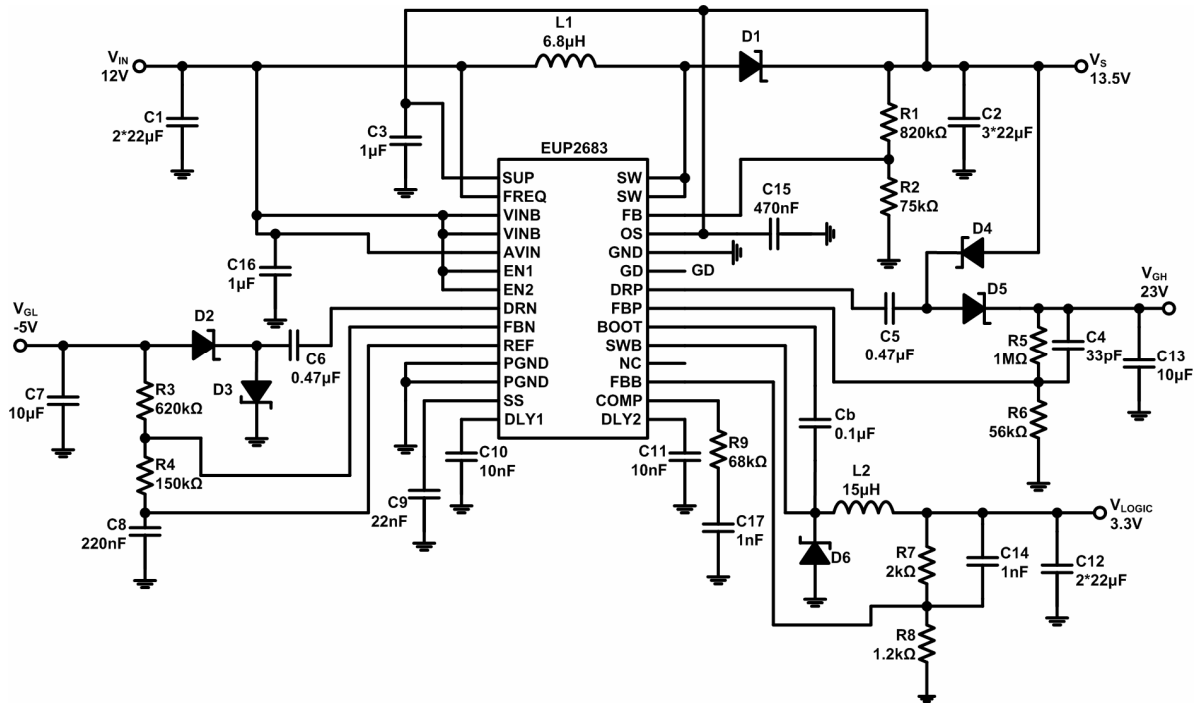


Figure 8. Standard 12V to 13.5V Conversion

Application Information (continued)

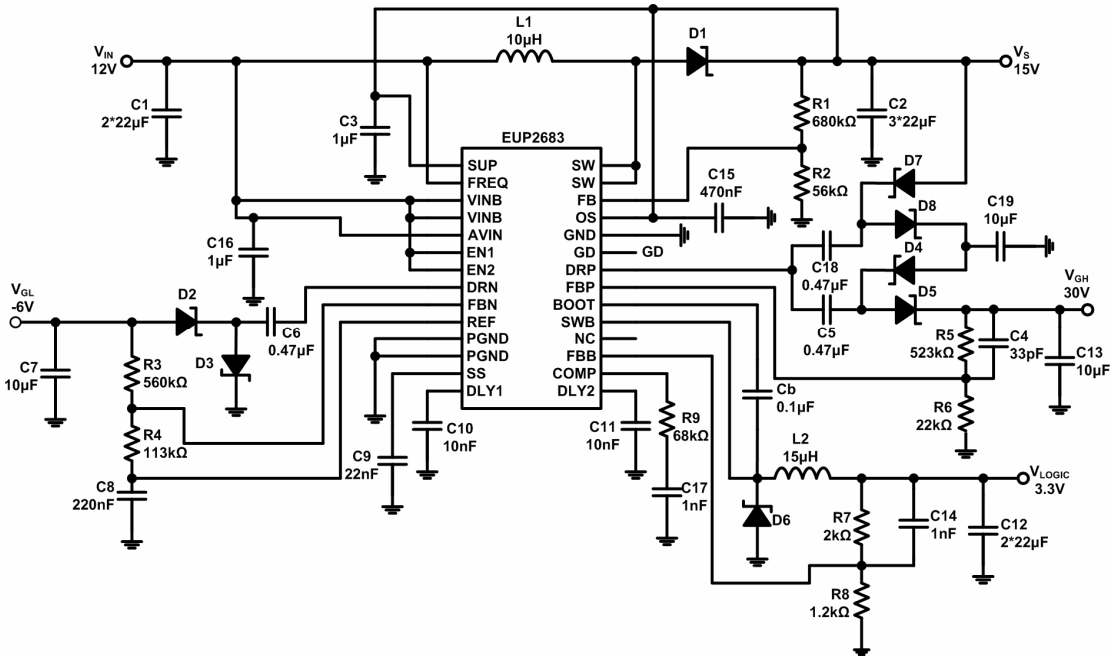
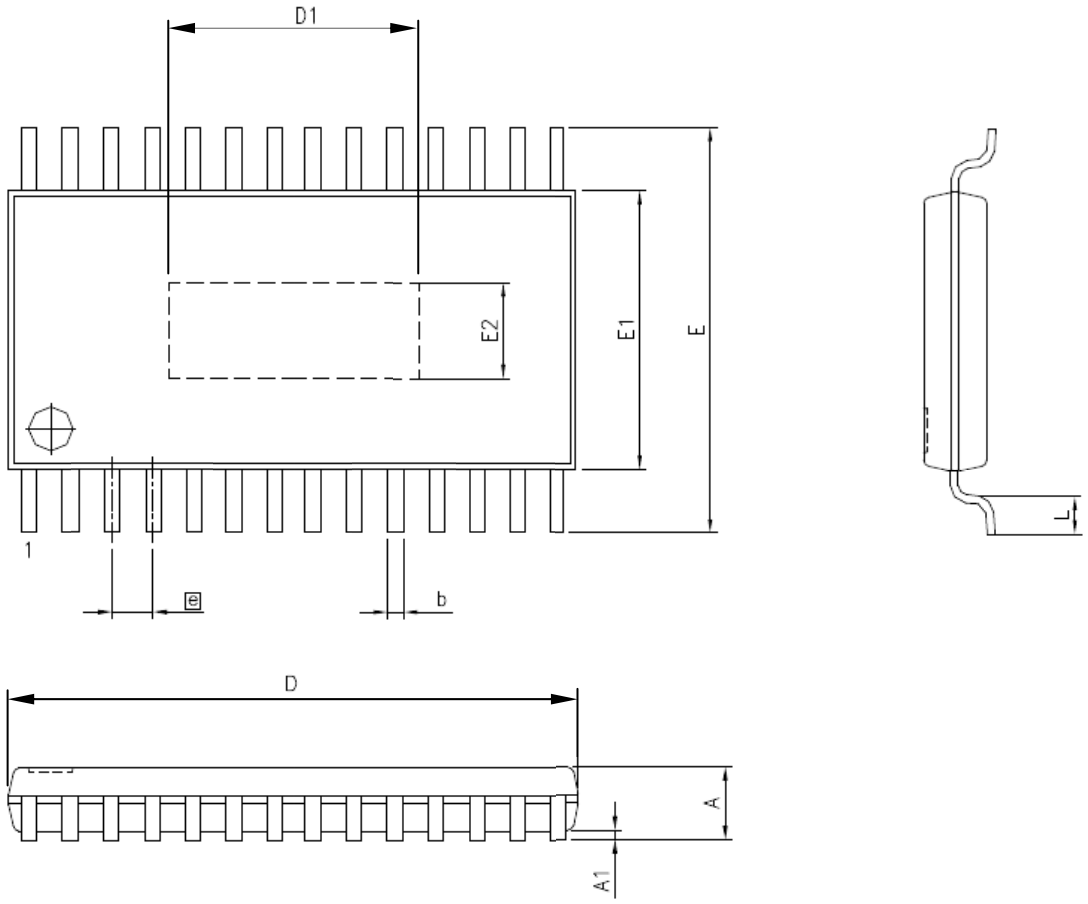


Figure 9. Standard 12V to 15V Conversion with 3x Positive Charge Pump

Packaging Information

TSSOP-28 (EP)



Note: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.20	-	0.047
A1	0.00	0.15	0.000	0.006
b	0.19	0.30	0.007	0.012
E1	4.40 REF		0.173 REF	
D	9.60	9.80	0.378	0.386
D1	2.80	6.30	0.110	0.248
E	6.20	6.60	0.244	0.260
E2	2.10	3.30	0.083	0.130
e	0.65 REF		0.026 REF	
L	0.45	0.75	0.018	0.030