2A Sink/Source Bus Termination Regulator

DESCRIPTION

The EUP7171 is a high performance linear regulator designed to provide power for termination of a DDR memory bus. It significantly reduces parts count, board space and overall system cost over previous switching solutions.

The EUP7171 contains a high-speed operational amplifier to provide excellent response to load transients. It also has an independent power source pin (VCNTL) for achieving better output driving capability. The regulator can both sink and source up to 2A current. The output termination voltage can be tightly regulated to track 1/2 V_{DDQ} by two external voltage divider resistors.

The EUP7171, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses. A typical DDR memory system is seen in Figure 1.

FEATURES

- Compatible with DDR-I (1.25VTT), DDR-II (0.9VTT) and DDR-III (0.75VTT) SDRAM Systems.
- Low Quiescent Current (1.1mA)
- Fast Transient Response Time
- Capable of Sourcing and Sinking 2A
- Adjustable VOUT by Two External Resistors
- Current Limiting Protection
- Over-Temperature Protection
- High Accuracy Output Voltage at Full-Load
- Low External Component Count
- Available in SOP-8 (EP) Package
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- DDR SDRAM Termination Voltage

Simplified System Diagram

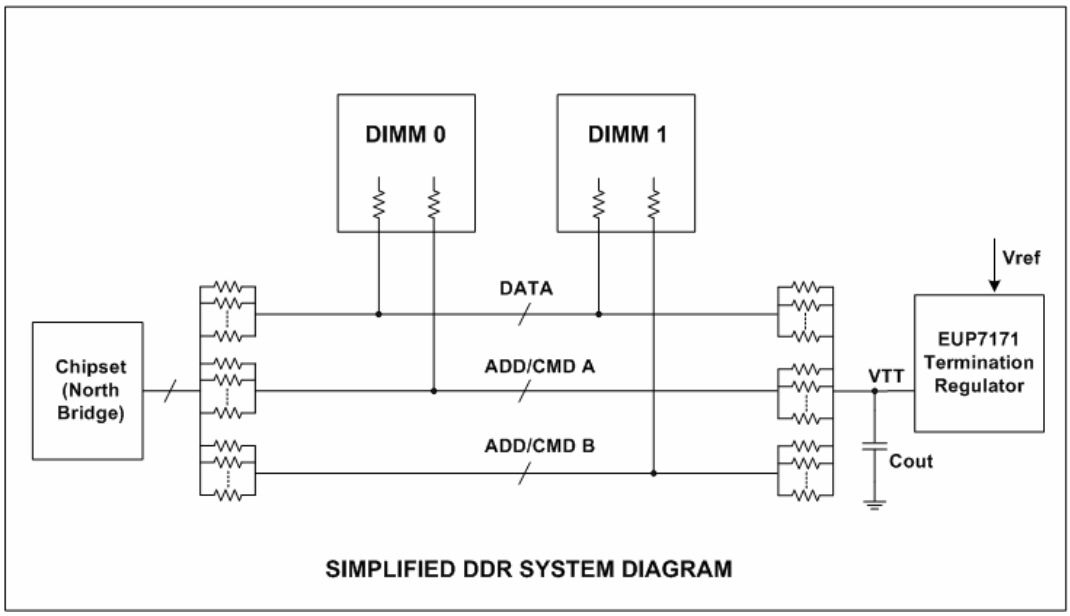
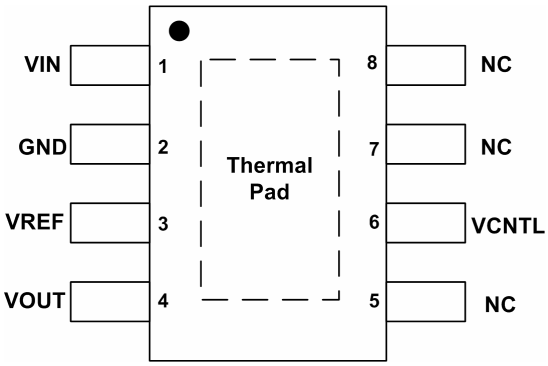


Figure1.

Pin Configurations

Package Type	Pin Configurations (TOP VIEW)
SOP-8 (EP)	

Pin Description

PIN	SYMBOL	DESCRIPTION
1	VIN	Power Input pin
2	GND	Ground
3	VREF	Reference voltage input and chip enable (Chip enable when VREF > 0.65V)
4	VOUT	Output voltage for regulation terminator voltage
6	VCNTL	Gate driver voltage
5 , 7 , 8	NC	NC

Typical Application Circuit

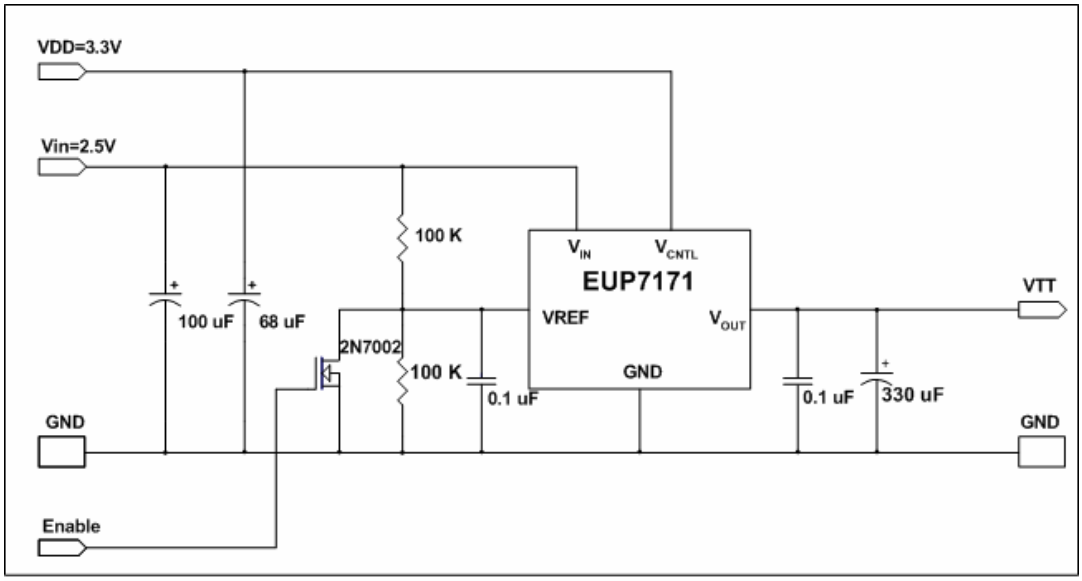


Figure2.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP7171DIR1	SOP-8 (EP)	xxxx EUP7171	-40°C to 125°C

EUP7171 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
D: SOP

Absolute Maximum Ratings

- Input voltage ---------- 6V
- Power dissipation ---------- Internal limiting
- ESD rating ---------- 2KV
- Maximum junction temperature ---------- 150 °C
- Storage temperature range ---------- -65°C to150°C
- Lead temperature (soldering , 5 sec) ---------- 260 °C
- Package thermal resistance SOP-8 (EP) θ_{JA} ---------- 42.3 °C/W

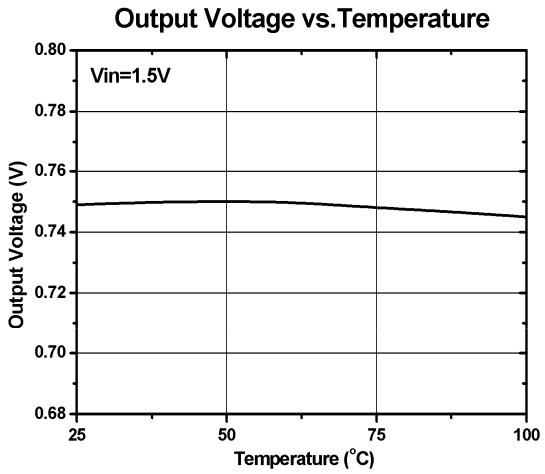
Electrical Characteristics

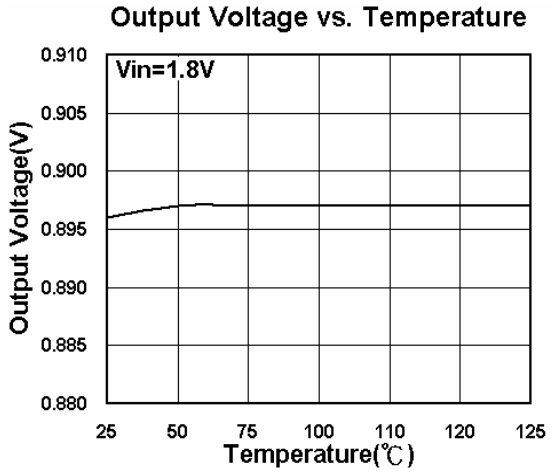
(Limits in standard typeface are for T_A=25 °C, unless otherwise specified:
VIN=2.5V/1.8V, VCNTL=3.3V, VREF=1.25V/0.9V, COUT=10μf (Ceramic)

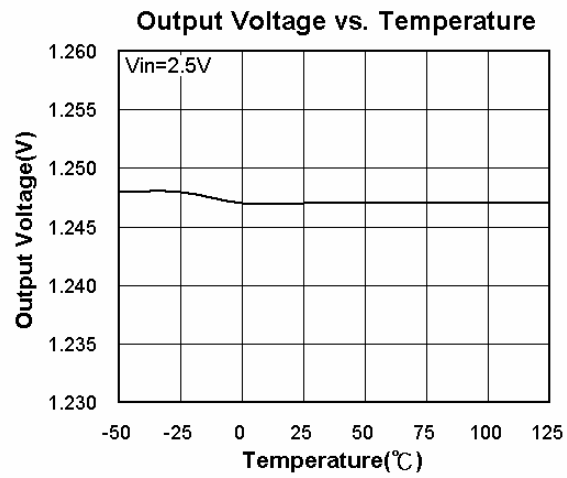
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Output Offset Voltage	I_{OUT} = 0A, (Note1)	-20	0	20	mV
ΔV_{LOAD}	Load Regulation	I_L : 0 →2A(DDRI)/1.5(DDRII) /1.5 (DDRIII)	-20	0	20	mV
		I_L : 0 → -2A(DDRI)/-1.5(DDRII) /-1.5 (DDRIII)				
VIN	Input Voltage Range (DDR I / DDR II /DDRIII)	Keep VCNTL ≥ VIN on operation power on and power off sequences	- -	2.5/1.8/1.5	- -	V
VCNTL			- -	3.3	5.5	
I_{VCNTL}	Operating Current of VCNTL	I_L = 0A	- -	1.4	2	mA
I_{SHDN}	Current in Shutdown mode	VREF ＜ 0.2V	- -	60	110	μA
Short Circuit Protection						
I_{LIMIT}	Current Limit		2.2	- -	- -	A
Over Temperature Protection						
T_{SD}	Thermal Shutdown Temperature		- -	157	- -	°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Guaranteed by design	- -	40	- -	°C
Shutdown function						
V_{IH}	Shutdown Threshold	Output = High	0.65	- -	- -	V
V_{IL}		Output = Low	- -	- -	0.2	

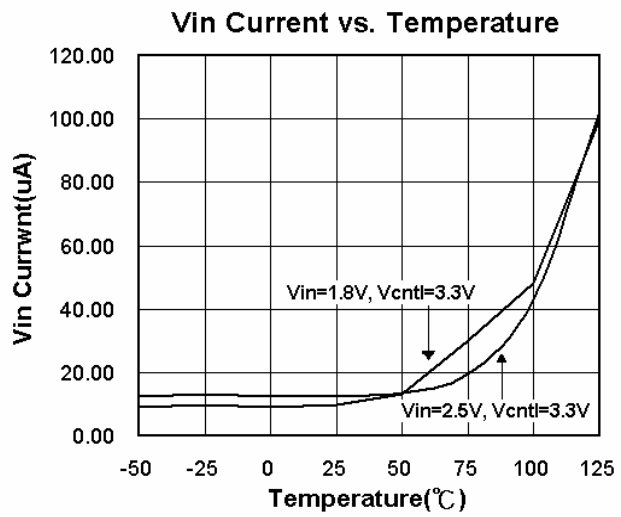
Note 1: V_{OS} offset is the voltage measurement defined as VOUT subtracted from VREF.

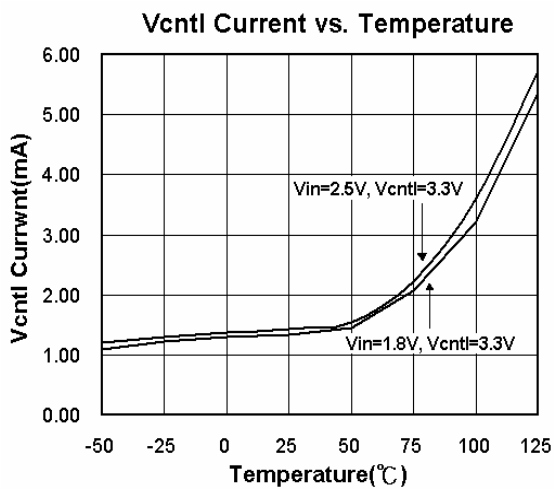
Typical Operating Characteristics

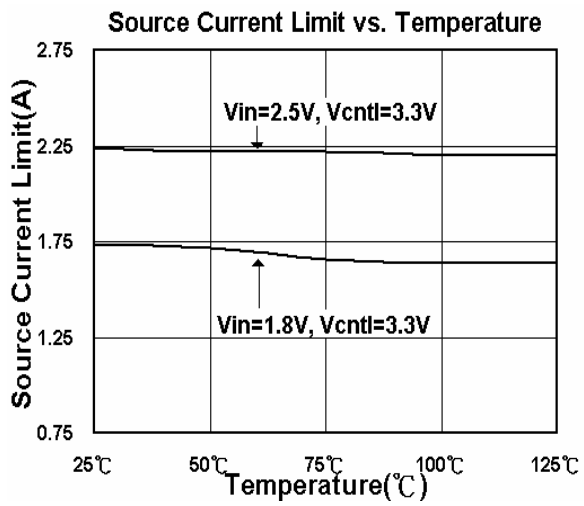






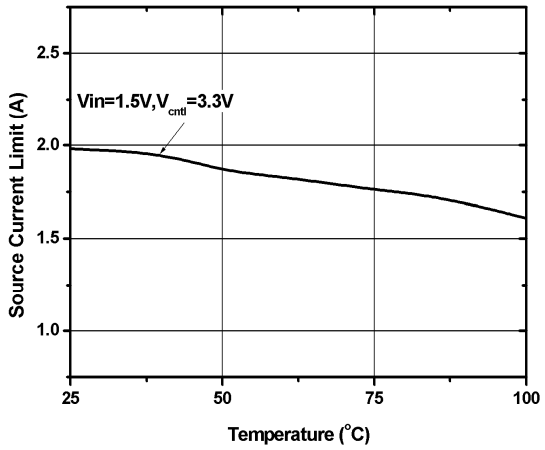




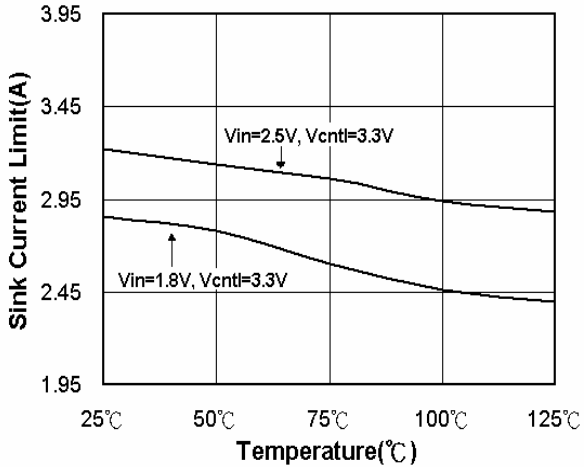


Typical Operating Characteristics (continued)

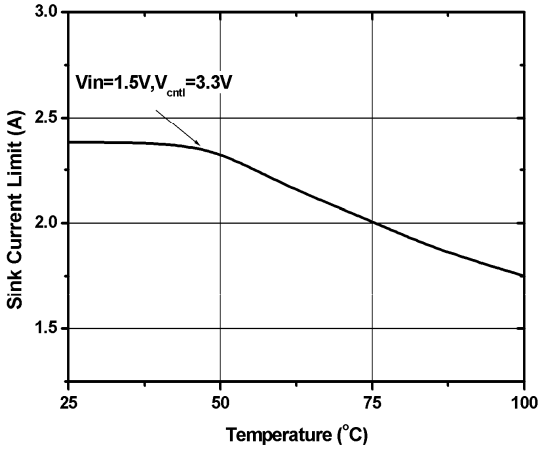
Source Current Limit vs. Temperature



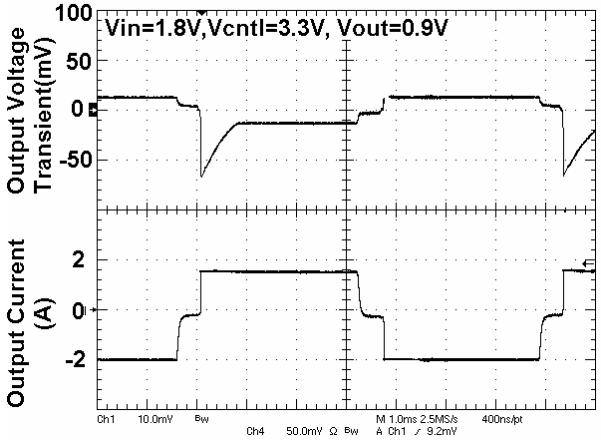
Sink Current limit vs. Temperature



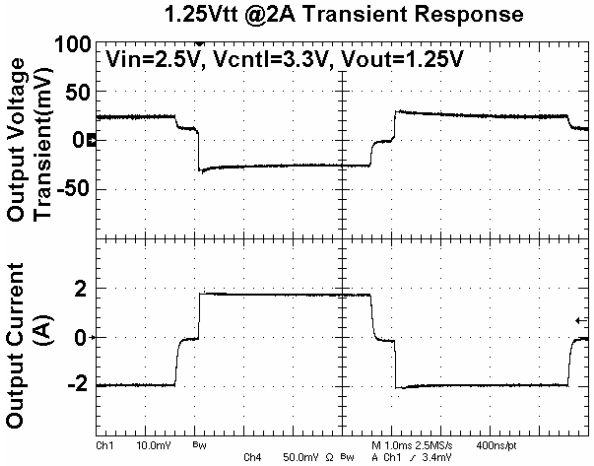
Sink Current Limit vs. Temperature



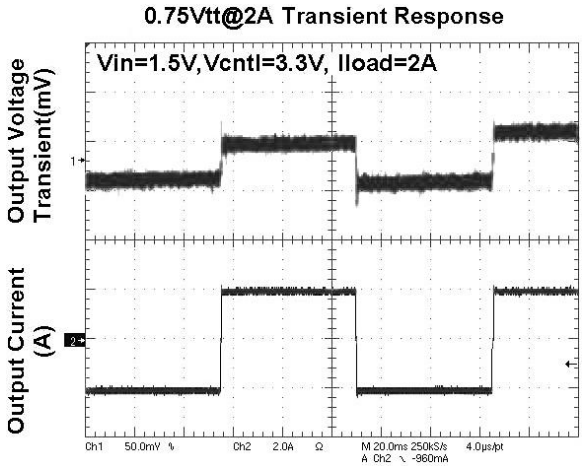
0.9Vtt @1.8A Transient Response



1.25Vtt @2A Transient Response

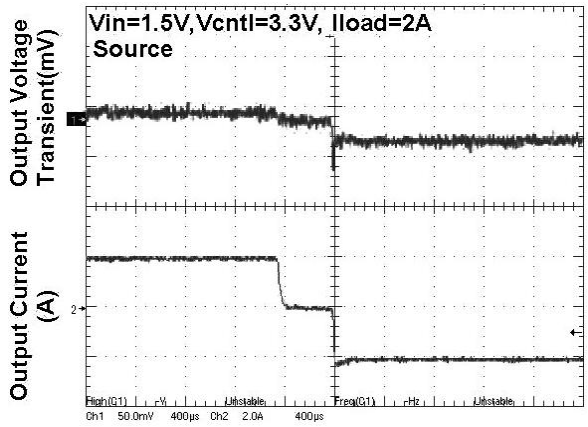


0.75Vtt@2A Transient Response

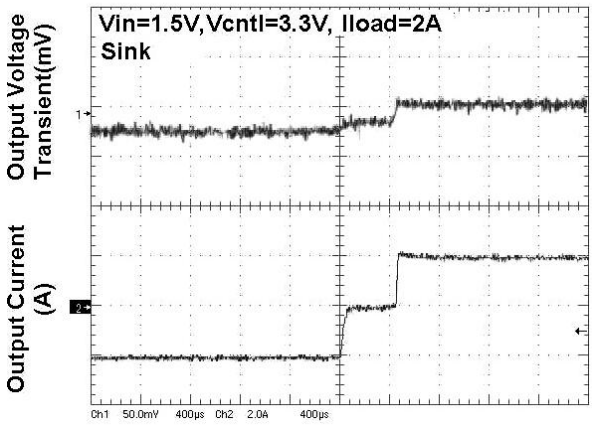


Typical Operating Characteristics (continued)

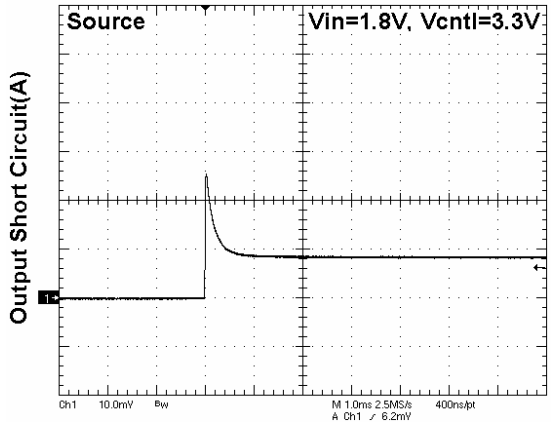
0.75Vtt@2A Transient Response



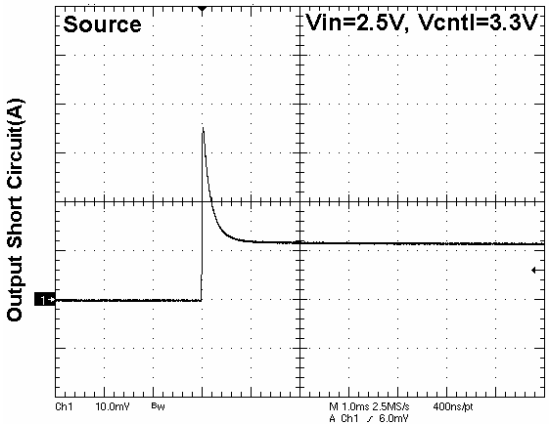
0.75Vtt@2A Transient Response



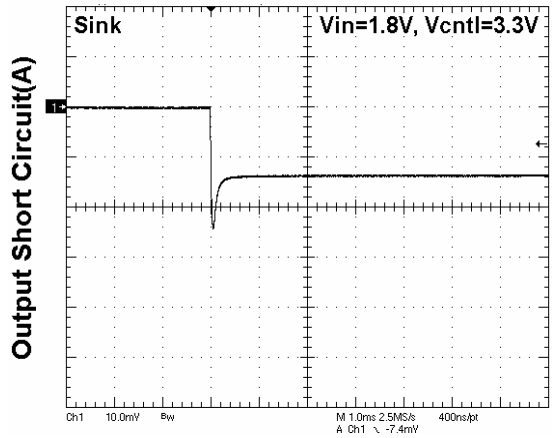
Output Short-Circuit Protection



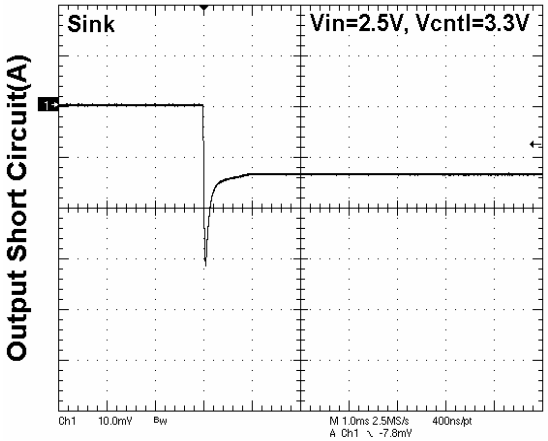
Output Short-Circuit Protection



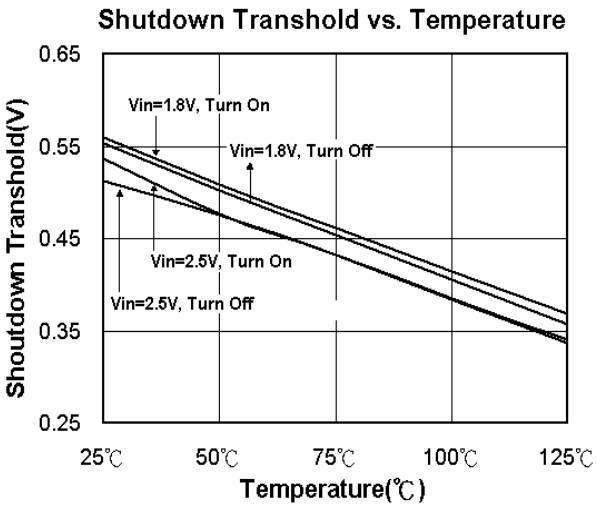
Output Short-Circuit Protection



Output Short-Circuit Protection



Typical Operating Characteristics (continued)



Function Block Diagram

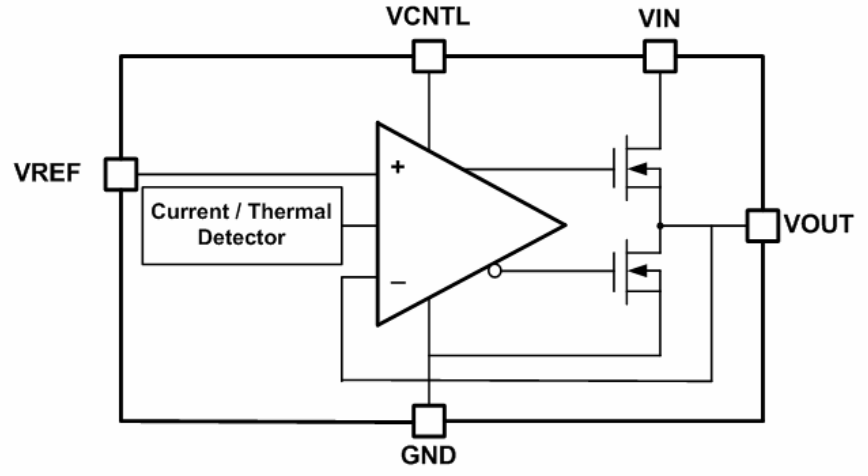


Figure3.

Pin Functions

VCNTL and VIN

VCNTL and VIN are the input supply pins for the EUP7171. VIN provides the rail voltage for VOUT generation. VCNTL is used to supply the internal control circuitry. The limitation on input voltage selection is that VIN must be equal to or lower than VCNTL. For DDR I application, a separation connection of VIN and VCNTL to 2.5V and 3.3V respectively can achieve better output drive capability.

VREF

VREF is an external reference input for the EUP7171. For SSTL-2 applications, VREF should be a 1.25V that the regulator can trace for termination voltage VOUT. It is recommended to place a 0.01µF to 0.1µF bypass capacitor at close to the VREF pin. An additional function included in the VREF is an active low shutdown. When VREF is pulled low the VOUT output will tri-state providing a high impedance output. A power savings advantage can be obtained in this mode through lower quiescent current.

VOUT

VOUT provides a regulated output for termination bus usage. It is capable of sinking and sourcing current while regulating the output voltage precisely to VREF. The regulator is designed to handle continue current up to +/-2A with fast transient response. If the application requires high load current with low voltage dropped, a large output capacitor with lower ESR (Equivalent Series Resistance) connected at VOUT is recommended. Thermal dissipation should be considered if the large current continues with long duration time. If the junction temperature exceeds the thermal shutdown point, the VOUT will turn to tri-state.

Component Selection

In order to obtain the best performance from the EUP7171, using lower **ESR** capacitor is necessary to Cin and Cout for high current load. The **ESR** of the output bulk capacitor primarily affects the capability to deliver a current surge within a specified delta voltage drop (**Δ**V) at VOUT. With a given capacitor **ESR**, the **Δ**V drop will be proportional to the load current, and a step in voltage drop will occur. (**Δ**Vstep-peak = ESR * IL), the SSTL-2 spec indicates a maximum delta voltage drop of 40mV.

A very good, low ESR electrolytic capacitor of no less than 470µF should be placed next to the terminator, which should be placed as possible to memory array. It might be possible to reduce the total capacitance, provided the performance remains stable. Examine the behavior of the VOUT bus carefully when the system is operating and verify that deviations in the bus voltage do not exceed the DDR specification (+/-40 mV).

VREF input is needed a high-frequency decoupling capacitor (CSS). A 0.1µF ceramic capacitor should be placed as possible to VREF.

PCB Layout Considerations

The EUP7171 regulator is packaged in plastic SOP-8 package. This small footprint package is unable to convectively dissipate at high current levels. The junction temperature should be kept well away from the thermal shutdown temperature in normal operation. To do this, care should be taken to derate the part dependent on several variables: the thickness of copper on PCB; the area of top side copper used and the airflow. Since multiple GND pins on the SOP-8 package are internally connected, the lowest thermal resistance will result if these pins are tightly connected on larger ground traces and more copper on top side of the printed circuit board.

If the large ground trace around the IC is unavailable on top, numerous vias from the ground connection to the internal ground plane will help. The vias should be small enough to retain solder when the board is wave-soldered.

Additional improvements can be achieved with a constant airflow across the package.

Test Circuit

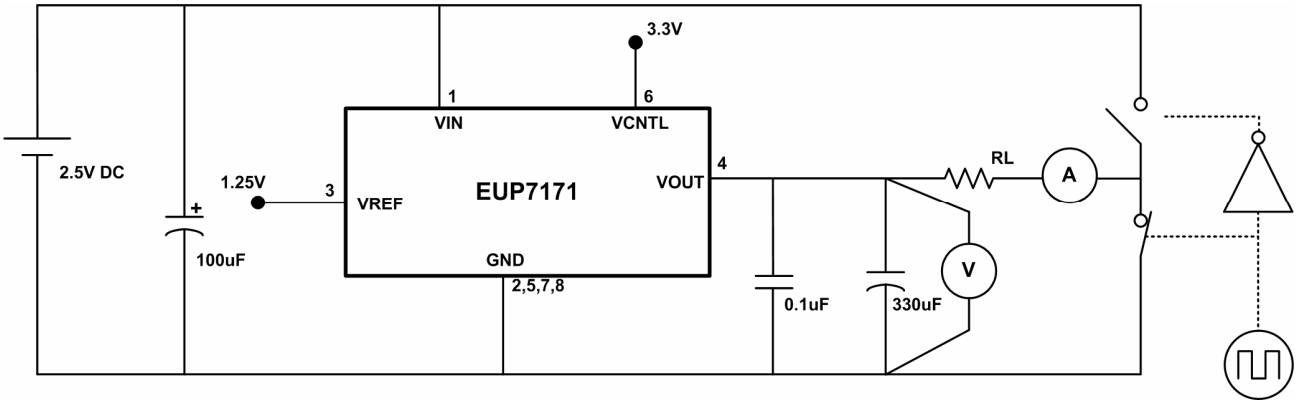
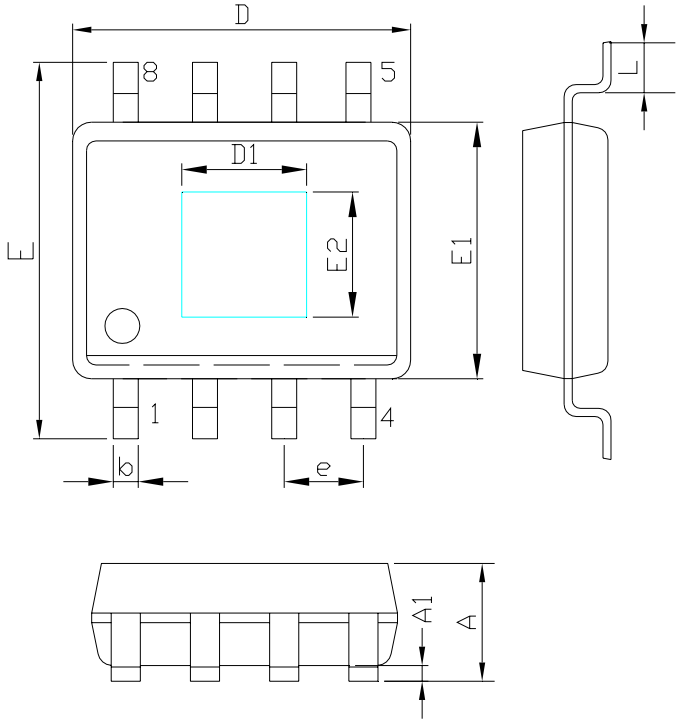


Figure 4. Load transient (+2A ~ –2A) test circuit

Packaging Information

SOP-8 (EP)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E1	3.90		0.153	
D1	2.00		0.081	
E2	2.00		0.081	
E	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	