SP6562A
Power Factor Controller IC

DESCRIPTION

SP6562A is an active transition-mode (TM) power factor correction (PFC) controller for AC-DC switching mode power supply applications.

SP6562A features an internal start-up timer for standalone applications, a one quadrant multiplier with THD optimizer for near unity power factor, zero current detector (ZCD) to ensure TM operation, a current sensing comparator with built-in leading-edge blanking, and a totem pole output ideally suited for driving a power MOSFET.

SP6562A offers great protection coverage including system over-voltage protection (OVP) to eliminate runaway output voltage due to load removal, VCC under voltage lockout (UVLO), multiplier output clamping that limit maximum peak switch current, and gate drive output clamping for external power MOSFET protection. with added system open loop protection feature, shuts down system when the feedback loop is open.

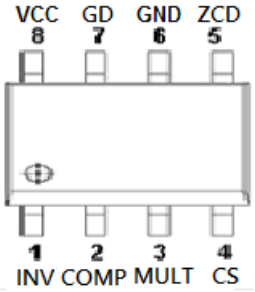
APPLICATIONS

- AC/DC Switching Power Adaptor
- PC Power Supply
- LCD TV Power Supply
- Electronic Ballast

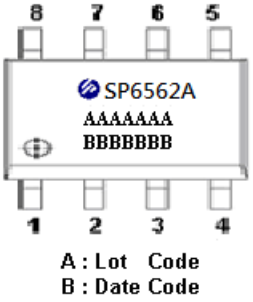
FEATURES

- Transition Mode (TM) Operation
- Low Total Harmonic Distortion(THD)
- Precise Adjustable Output Over-Voltage Protection
- Open-Feedback Protection and Disable Function
- Zero Current Detector
- Internal Start up timer
- Under-Voltage Lockout with 2.5V Hysteresis
- Low Start-up (30μA)
- Low (2.2mA) quiescent current
- 1.4% internal reference voltage
- -600/+800mA totem pole gate driver with active pull-down during UVLO and voltage clamp
- SOP-8 Package

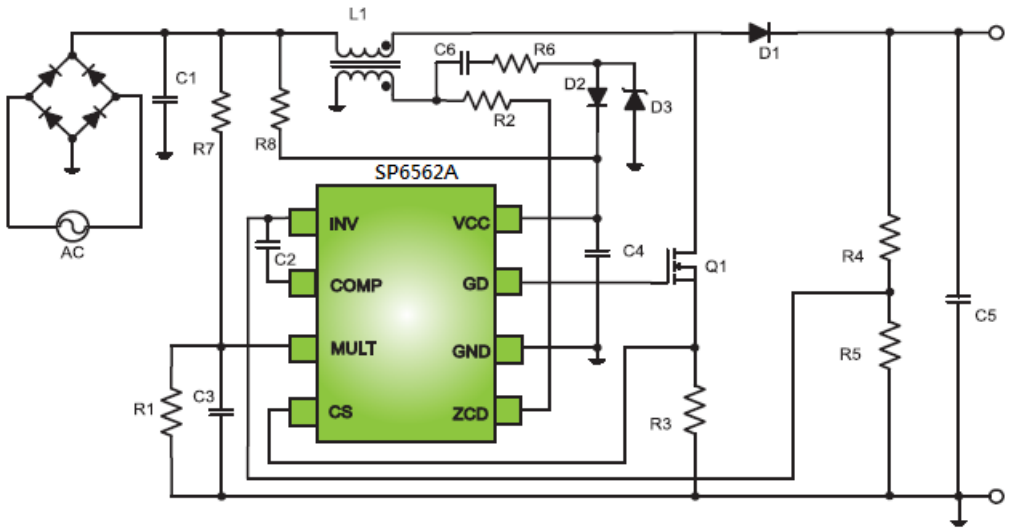
PIN CONFIGURATION(SOP-8)



PART MARKING



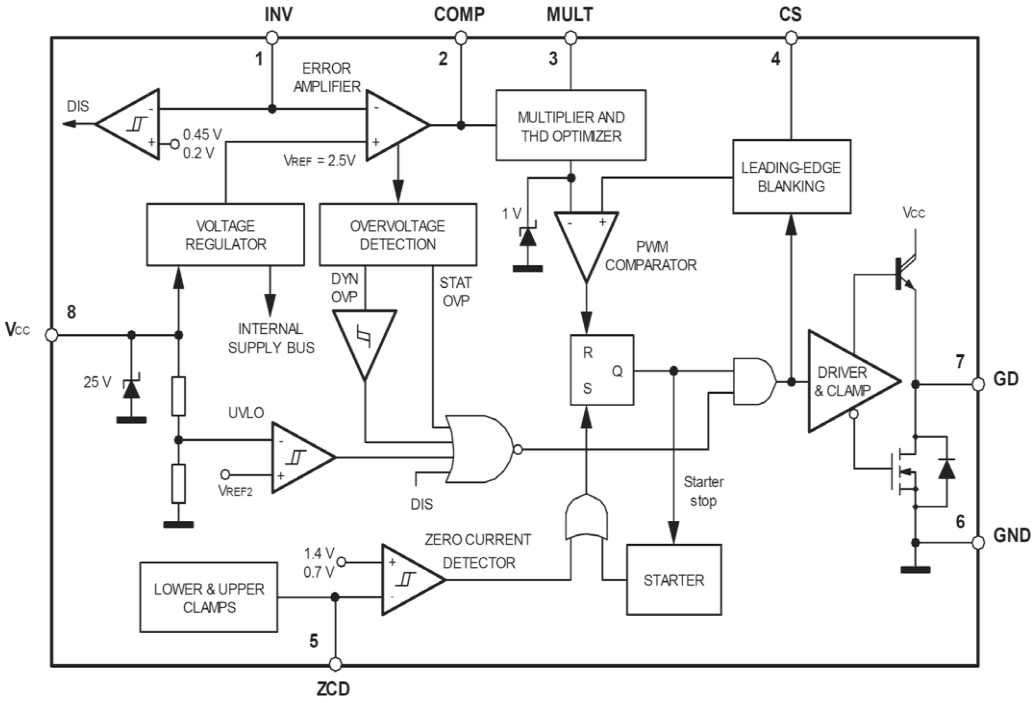
TYPICAL APPLCATION CIRCUIT FOR HIGH EFFICIENCY SMPS



PIN DESCRIPTION

Pin	Symbol	Description
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into this pin through a resistor divider. The pin doubles as an ON/OFF control input.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off. The pin is equipped with 200 ns leading-edge blanking for improved noise immunity.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Part Marking
SP6562AS8RGB	SOP-8	SP6562A

※ SP6562AS8RGB : Tape Reel ; Pb – Free ; Halogen-Free

ABSOULTE MAXIMUM RATINGS (T_A=25℃, unless otherwise specified.)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (I_{CC}≦20mA)	Self-limited	V
I_{GD}	Output totem pole peak current	Self-limited	A
	Analog inputs & outputs Voltage	-0.3 ~ 8.0	V
I_{ZCD}	Zero current detector max. current	±10	mA
T_{ope}	Operating Ambient Temperature	-40 ~ 85	℃
T_J	Operating Junction Temperature Range	-40 ~ 150	℃
T_{STG}	Storage Temperature Range	-55 ~ 150	℃
T_{LEAD}	Pb-Free Lead Soldering Temperature for 5 sec.	260	℃
$R_{\Theta JA}$	Thermal Resistance Junction – Ambient	150	℃/W

ELECTRICAL CHARACTERISTICS

(-25℃ < T_J < +125℃, V_{CC} = 12V, Co = 1nF; unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (Vcc Pin)						
V_{CC}	Operating range	After turn-on	10.5		22.5	V
Vcc_{On}	Turn-on threshold	(1)	11.2	12.5	13.3	V
Vcc_{Off}	Turn-off threshold	(1)	9.0	10	10.5	V
Hys	Hysteresis		2.0		2.8	V
V_Z	Zener Voltage	I_{CC} = 20mA	22.5	25	28	V
Supply Current						
$I_{start-up}$	Start-up current	Before turn-on, V_{CC} = 11V		30	60	µA
I_q	Quiescent current	After turn-on		2.2	3.75	mA
I_{CC}	Operating supply current	@ 70kHz		3.5	5	mA
I_q	Quiescent current	During OVP (either static or dynamic) or $V_{INV} \leqq$ 150mV		1.7	2.5	mA
Multiplier Input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 4V			-1	µA
V_{MULT}	Linear operation range		0 to 3			V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output max. slope	V_{MULT} = 0 to 1V, V_{COMP} = Upper clamp	1	1.1		V/V
K	Gain (2)	V_{MULT} = 1V, V_{COMP}= 4V,	0.31	0.38	0.44	V
Error Amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 ℃	2.470	2.5	2.530	V
		10.5V < V_{CC} < 22.5V (1)	2.455		2.545	
	Line regulation	V_{CC} = 10.5V to 22.5V		2	5	mV
I_{INV}	Input bias current	V_{INV} = 0 to 3V			-1	µA
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4V, V_{INV} = 2.4V	-2	-3.5	-5	mA
	Sink current	V_{COMP} = 4V, V_{INV} = 2.6V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5mA	5.3	5.7	6	V
	Lower clamp voltage	I_{SINK} = 0.5mA (1)	2.1	2.25	2.4	V
V_{INVdis}	Disable threshold		150	200	250	mV
V_{INVen}	Restart threshold		380	450	520	mV
Output Overvoltage						
I_{OVP}	Dynamic OVP triggering current		23.5	27	30.5	µA
Hys	Hysteresis	(3)		20		µA
	Static OVP threshold	(1)	2.1	2.25	2.4	V

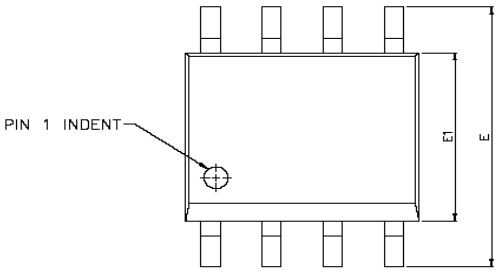
ELECTRICAL CHARACTERISTICS

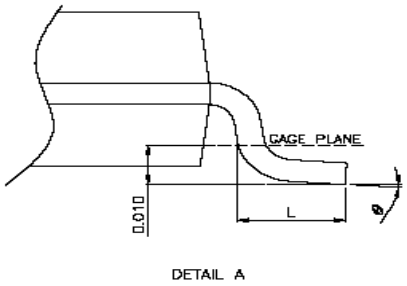
(-25℃ < T_J < +125℃, V_{CC} = 12V, Co = 1nF; unless otherwise specified.)

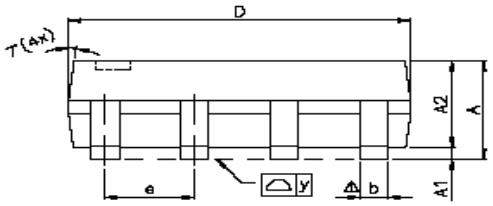
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			-1	µA
t_{LEB}	Leading edge blanking		100	200	300	nS
$td_{(H-L)}$	Delay to output			175		nS
V_{CS}	Current sense clamp	V_{COMP} = Upper clamp, Vmult = 1.5V	1.0	1.08	1.16	V
Vcs_{offset}	Current sense offset	V_{MULT} = 0		25		mV
		V_{MULT} = 2.5V		5		
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5mA	5.0	5.7	6.5	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5mA	-0.3	0	0.3	V
V_{ZCDA}	Arming voltage (positive-going edge)	(3)		1.4		V
V_{ZCDT}	Triggering voltage (negative-going edge)	(3)		0.7		V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5V		2		µA
I_{ZCDsrc}	Source current capability		-2.5			mA
I_{ZCDsnk}	Sink current capability		2.5			mA
Starter						
tSTART	Start timer period		75	190	300	µS
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100mA		0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5mA	9.0	9.5		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A
t_f	Voltage fall time			60	100	nS
t_r	Voltage rise time			100	150	nS
V_{Oclamp}	Output clamp voltage	I_{source} = 5mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc = 0 to V_{CCon}, I_{sink} = 2 mA			1.1	V

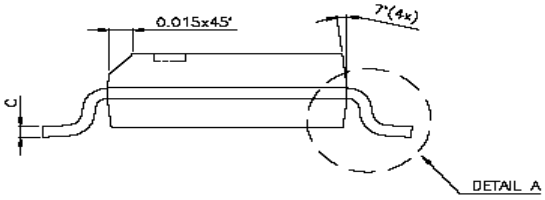
1. All the parameters are in tracking
2. The multiplier output is given by: $V_{CS} = K , V_{MULTX} \cdot (V_{COMP}-2.5)$
3. Parameters guaranteed by design , functionality tested in production

SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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