SPN03T20
N-Channel Enhancement Mode MOSFET

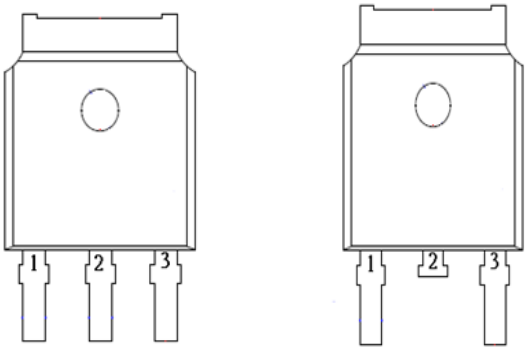
DESCRIPTION
The SPN03T20 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN03T20 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

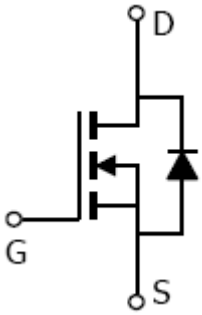
APPLICATIONS
- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch
- TV Power

FEATURES
- 200V/3A, $R_{DS(ON)}$=850mΩ@V_{GS}=10V
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-251S-3L ,TO-252-2L package design

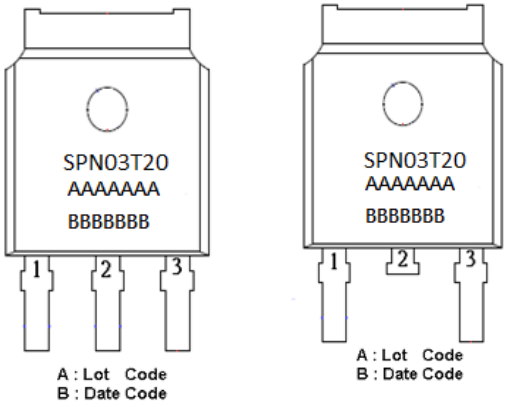
PIN CONFIGURATION

TO-251S-3L **TO-252-2L**





PART MARKING



SPN03T20
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN03T20ST251TGB	TO-251S-3L	SPN03T20
SPN03T20T252RGB	TO-252-2L	SPN03T20

※ SPN03T20ST251TGB : Tube ; Pb – Free ; Halogen - Free
※ SPN03T20T252RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	200	V
Gate –Source Voltage		V_{GSS}	±30	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	3	A
	T_A=70℃		2	
Pulsed Drain Current		I_{DM}	12	A
Avalanche Energy, Single Pulse @ L=0.1mH, T_A=25℃		E_{AS}	21	mJ
Power Dissipation	T_A=25℃	P_D	40	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	3.1	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	3.0	4.0	5.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±30V			±100	nA
Drain-Source Leakage Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V			1	uA
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS} =10V			3	A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=2A		0.7	0.85	Ω
Forward Transconductance	gfs	V_{DS}=10V,I_D=2A		3.6		S
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS} =0V			1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=160V,V_{GS}=10V I_D= 1A		4.8	9	nC
Gate-Source Charge	Q_{gs}			2	4	
Gate-Drain Charge	Q_{gd}			0.8	2	
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz		266	510	pF
Output Capacitance	C_{oss}			160	300	
Reverse Transfer Capacitance	C_{rss}			55	110	
Turn-On Time	$t_{d(on)}$	V_{DD}=100V, I_D=1A, V_{GEN}=10V, R_G=25Ω		10	20	nS
	t_r			35	70	
Turn-Off Time	$t_{d(off)}$			10	20	
	t_f			28	56	

TYPICAL CHARACTERISTICS

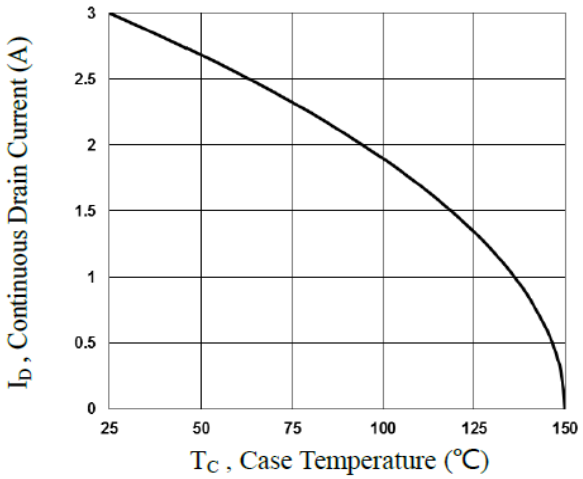


Fig.1 Continuous Drain Current vs. T_C

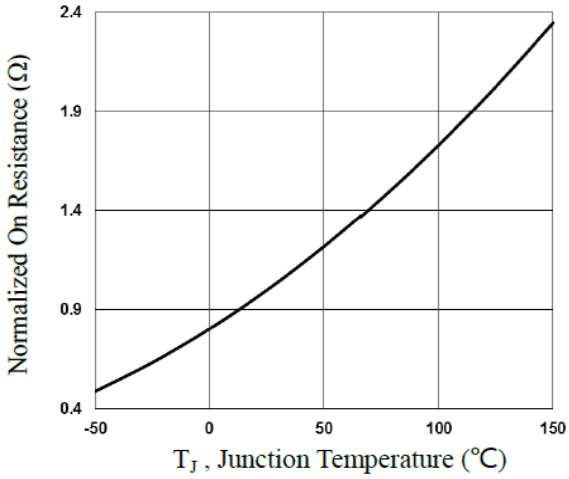


Fig.2 Normalized RDSON vs. T_J

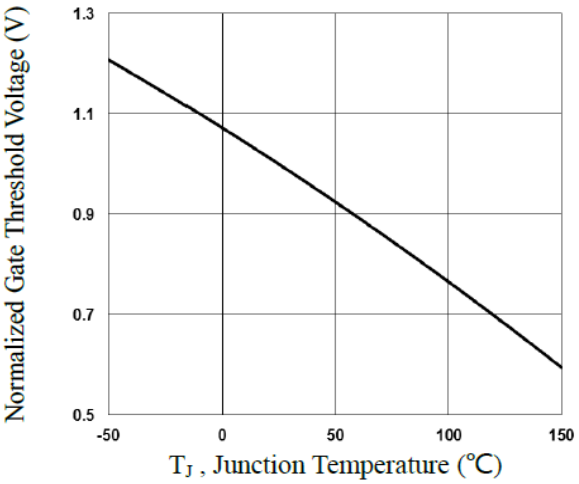


Fig.3 Normalized V_{th} vs. T_J

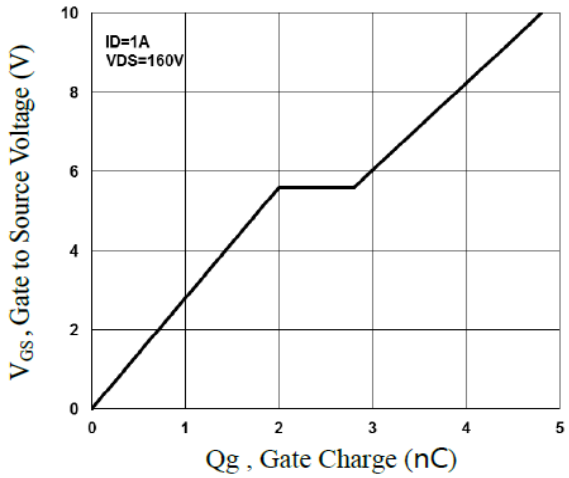


Fig.4 Gate Charge Waveform

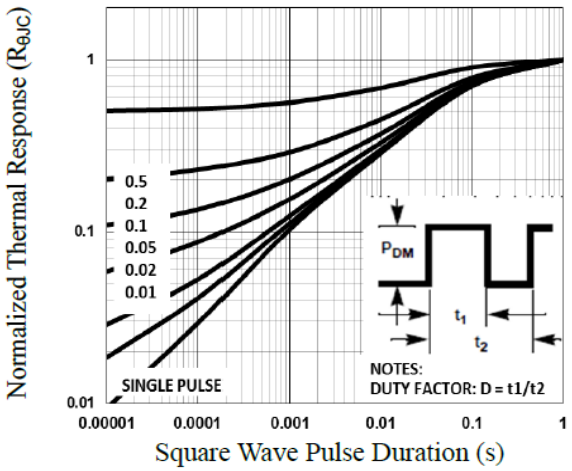


Fig.5 Normalized Transient Impedance

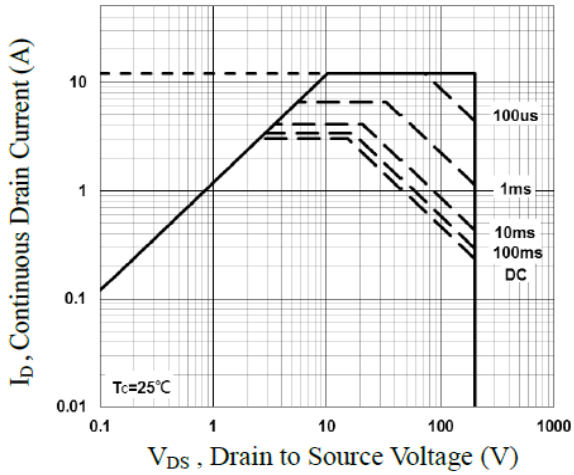
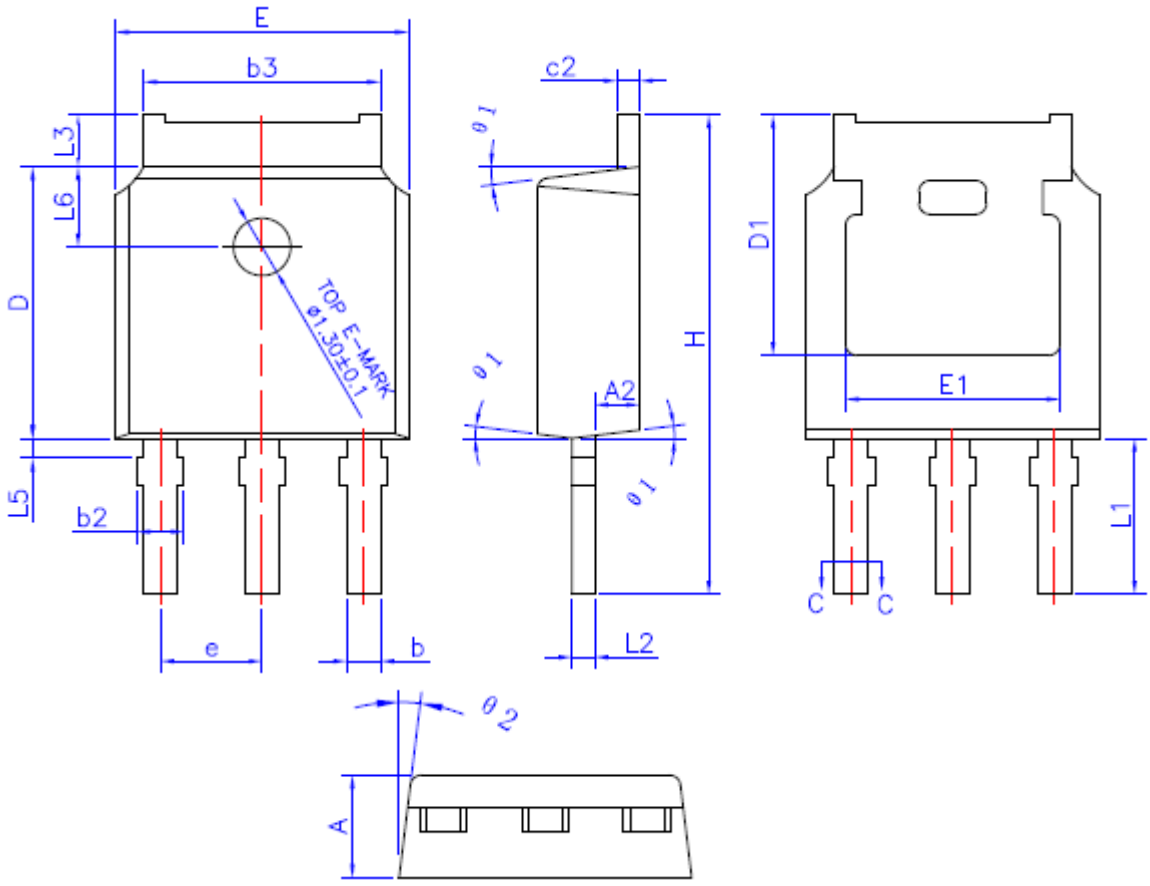


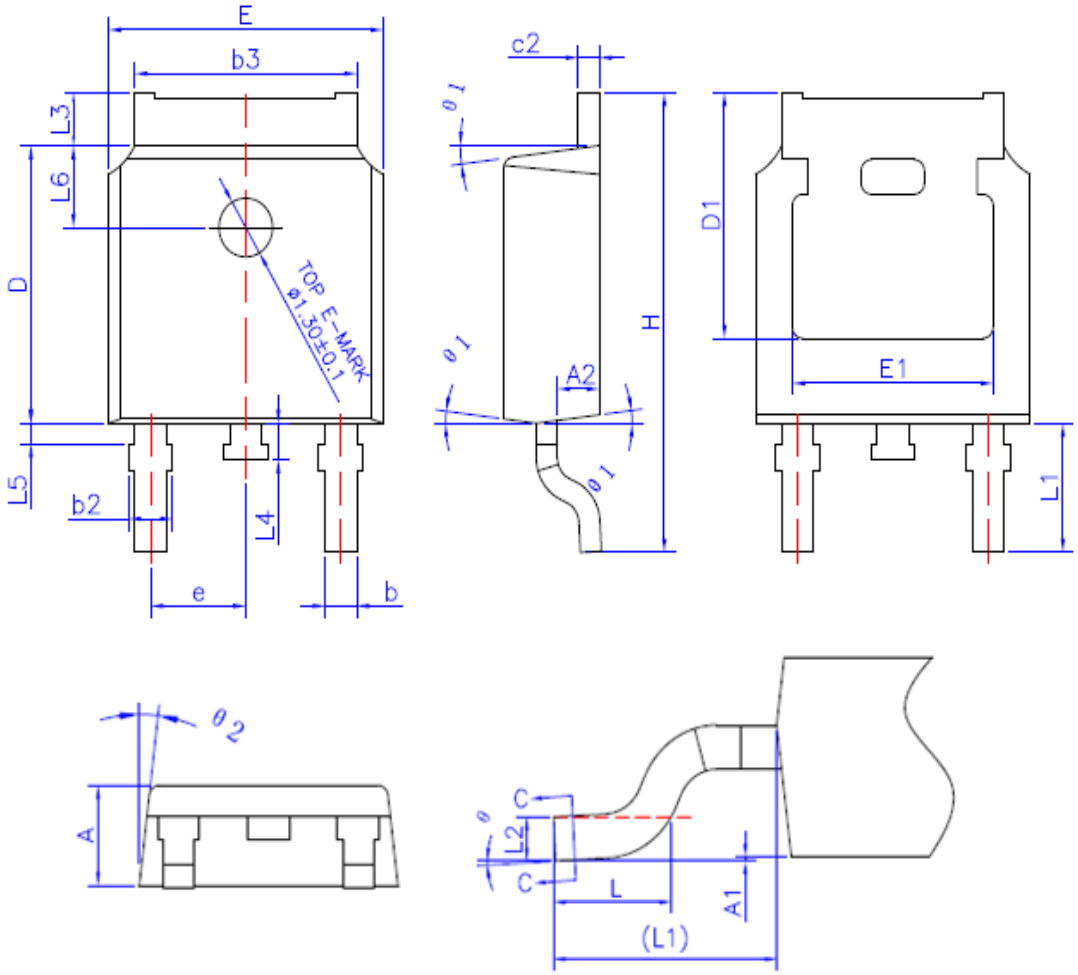
Fig.6 Maximum Safe Operation Area

TO-251S-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A2	0.86	1.01	1.16
b	0.66	-	0.86
b2	0.66	--	0.96
b3	5.10	5.28	5.46
c	0.46	--	0.60
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1		5.35REF	
E	6.40	6.60	6.80
E1		4.83REF	
e		2.3REF	
H	9.80	10.40	11.00
L1		3.50REF	
L2		0.508BSC	
L3	0.90	--	1.25
L5	0.15	--	0.75
L6		1.80REF	
θ 1	5°	7°	9°
θ 2	5°	7°	9°

TO-252-2L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	--	0.15
A2	0.90	1.01	1.10
b	0.72	-	0.85
b2	0.72	--	0.90
b3	5.13	5.33	5.46
c	0.47	--	0.60
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1	5.25	--	--
E	6.40	6.60	6.80
E1	4.70	--	--
e	2.3REF		
H	9.80	10.10	10.40
L	1.40	1.60	1.80
L1	2.90REF		
L2	0.508BSC		
L3	0.90	--	1.25
L4	0.60	0.80	1.00
L5	0.15	--	0.75
L6	1.80REF		
θ	0°	3°	8°
θ 1	5°	7°	9°
θ 2	5°	7°	9°

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