



SPN11T11

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN11T11 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN11T11 has been designed specifically to improve the over all efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

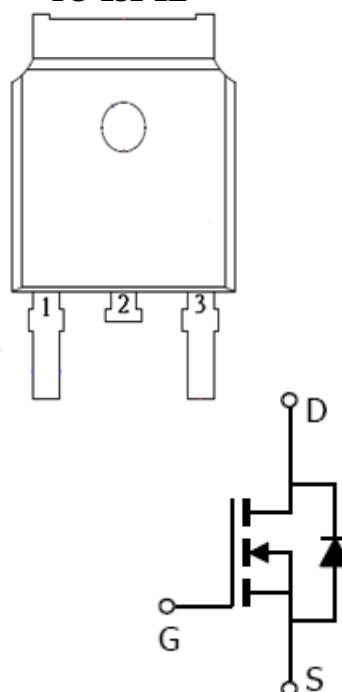
- ◆ 110V/12A, $R_{DS(ON)}=108m\Omega@V_{GS}=10V$
- ◆ 110V/12A, $R_{DS(ON)}=137m\Omega@V_{GS}=4.5V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L , package design

APPLICATIONS

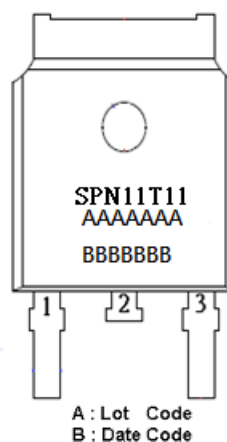
- Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

TO-252-2L



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN11T11T252RGB	TO-252-2L	SPN11T11

※ SPN11T11T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	110	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _C =25°C	I _D	12	A
	T _C =70°C		8.0	
Pulsed Drain Current		I _{DM}	24	A
Avalanche Current		I _{AS}	14	A
Power Dissipation @ T _C =25°C		P _D	40	W
Operating Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	110	°C/W



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ELECTRICAL CHARACTERISTICS

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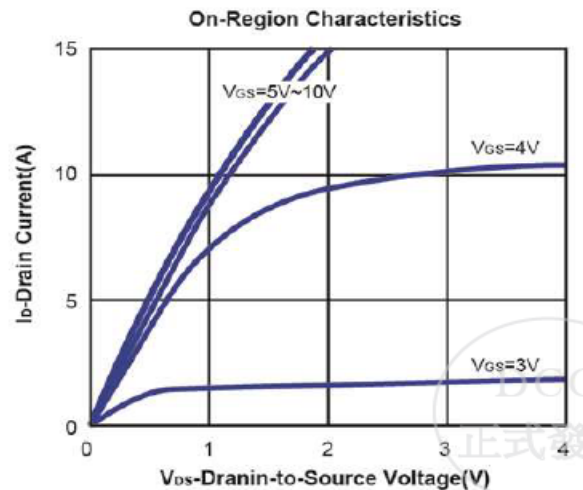
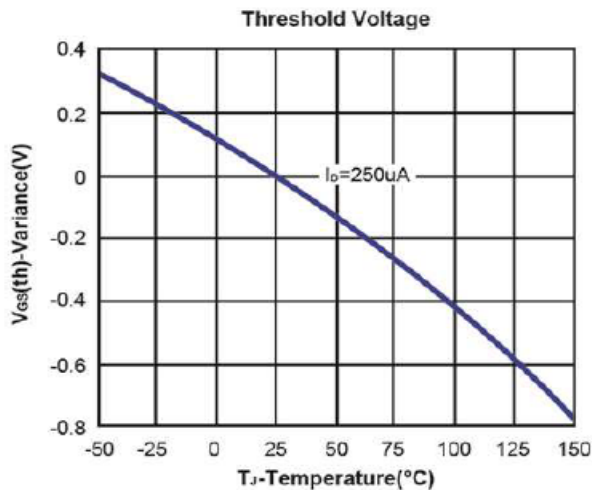
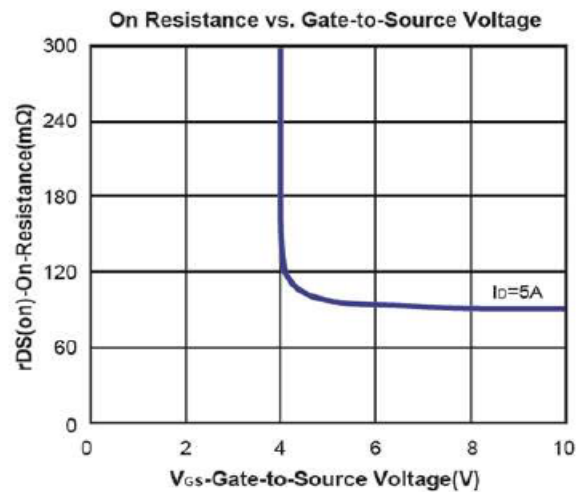
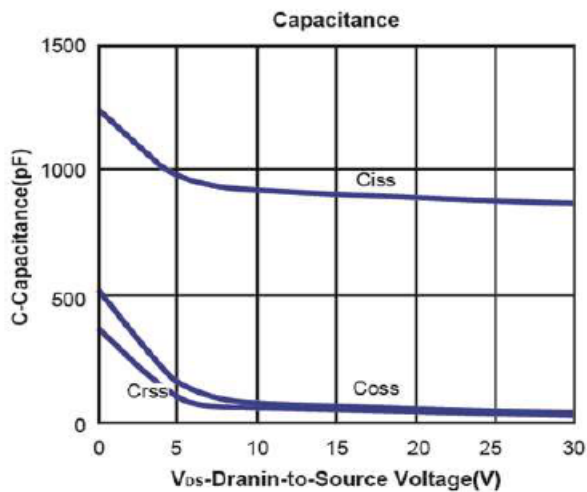
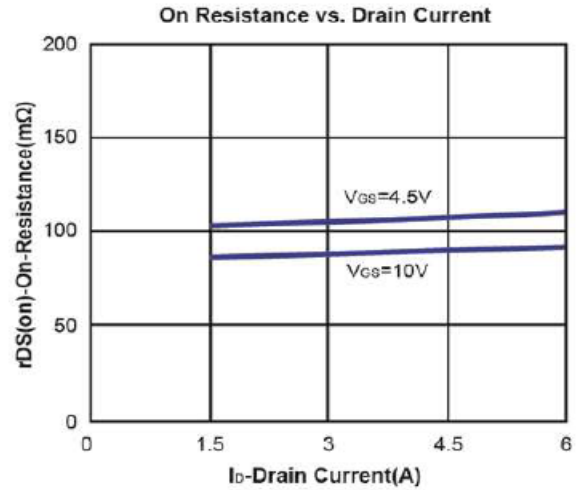
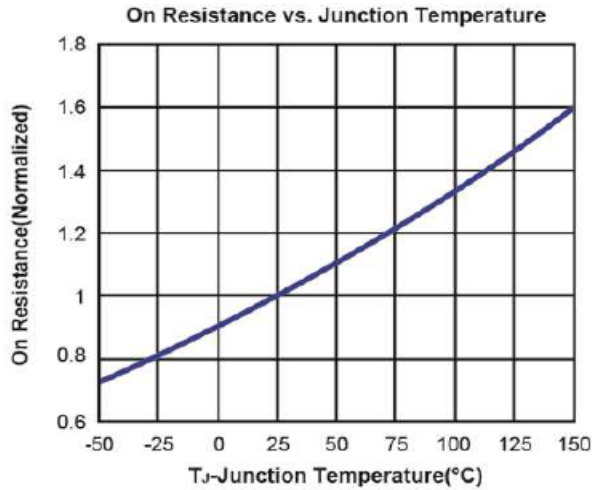
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	110			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	μA
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	12			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A$		90	108	$m\Omega$
		$V_{GS}=4.5V, I_D=3A$		105	137	$m\Omega$
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q_g	$V_{DS}=50V, I_D=5A$		22.3		nC
Total Gate Charge (4.5V)	Q_g			11.9		
Gate-Source Charge	Q_{gs}			4.8		
Gate-Drain Charge	Q_{gd}			6.4		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		895		pF
Output Capacitance	C_{oss}			56		
Reverse Transfer Capacitance	C_{rss}			43		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, I_D=5A,$ $V_{GEN}=10V, R_G=1\Omega$		13.3		nS
	t_r			25.4		
Turn-Off Time	$t_{d(off)}$			27.5		
	t_f			16.2		



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TYPICAL CHARACTERISTICS

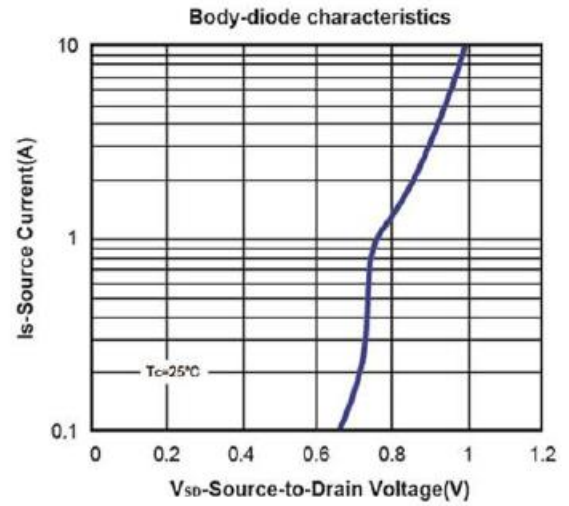
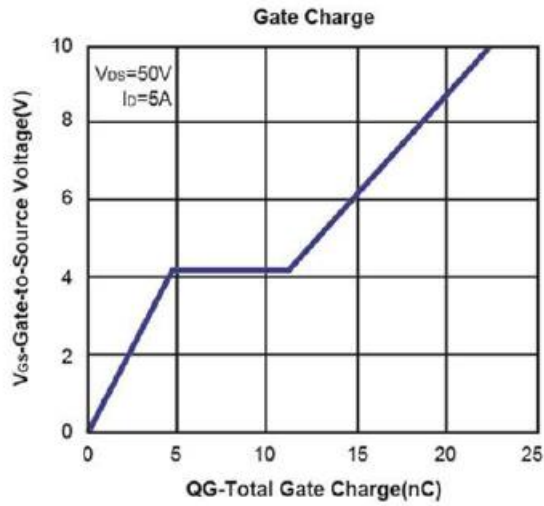




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TYPICAL CHARACTERISTICS

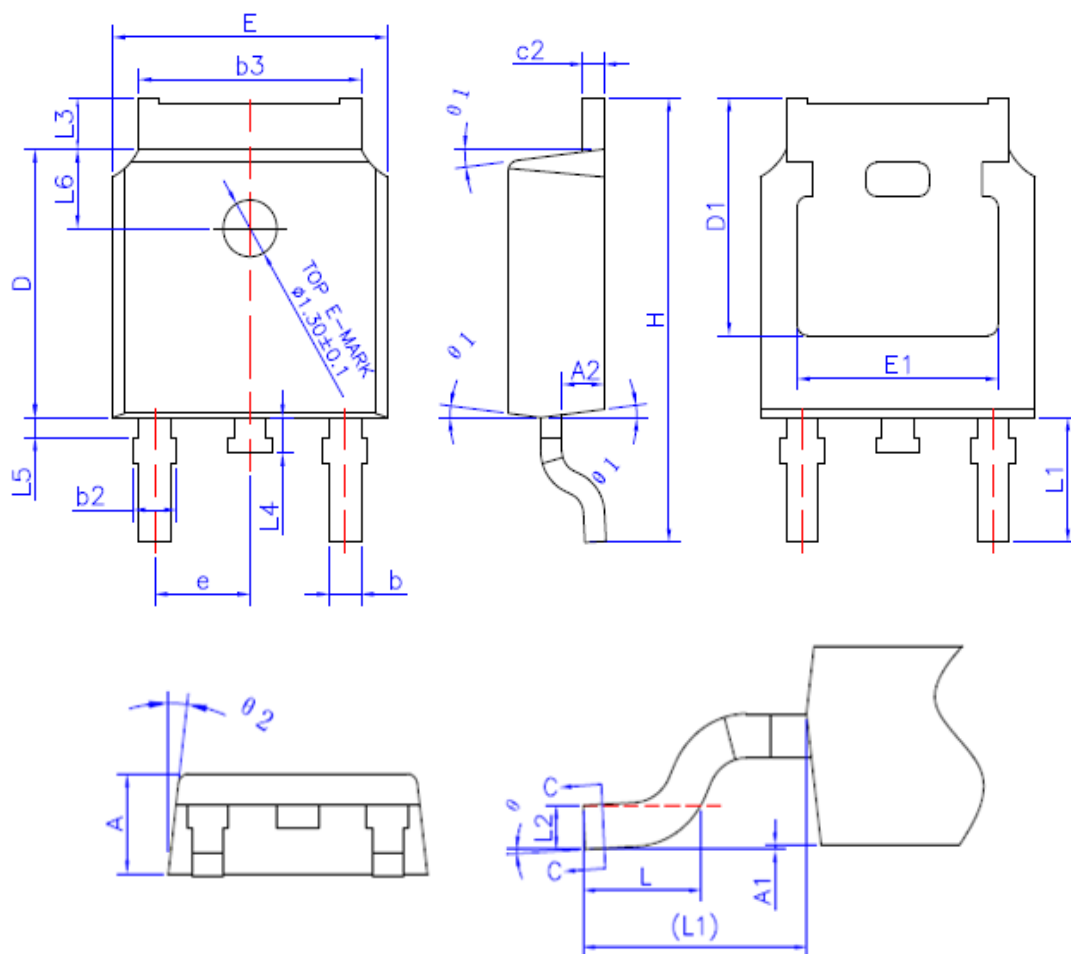




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TO-252-2L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	--	0.15
A2	0.90	1.01	1.10
b	0.72	--	0.85
b2	0.72	--	0.90
b3	5.13	5.33	5.46
c	0.47	--	0.60
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1	5.25	--	--
E	6.40	6.60	6.80
E1	4.70	--	--
e	2.3REF		
H	9.80	10.10	10.40
L	1.40	1.60	1.80
L1	2.90REF		
L2	0.508BSC		
L3	0.90	--	1.25
L4	0.60	0.80	1.00
L5	0.15	--	0.75
L6	1.80REF		
θ	0°	3°	8°
θ 1	5°	7°	9°
θ 2	5°	7°	9°



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