



# SPN120T20

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN120T20 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

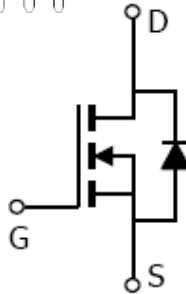
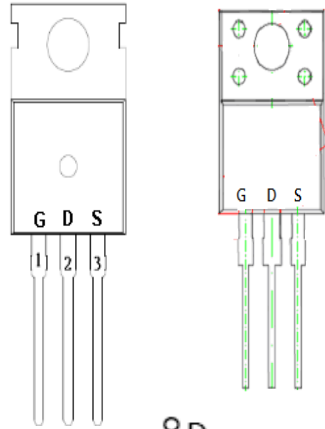
- ◆ 200V/120A,  $R_{DS(ON)}=11m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L package design

### APPLICATIONS

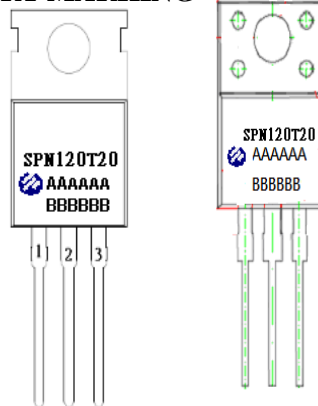
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

### PIN CONFIGURATION

TO-220-3L      TO-220F-3L



### PART MARKING



A : Lot Code  
B : Date Code

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B: Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN120T20T220TGB	TO-220-3L	SPN120T20
SPN120T20T220FTGB	TO-220F-3L	SPN120T20

※ SPN120T20T220TGB : Tube ; Pb – Free ; Halogen – Free

※ SPN120T20T220FTGB : Tube ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	200	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current (Silicon Limited)	I <sub>D</sub>	T <sub>C</sub> =25°C	132	A
		T <sub>C</sub> =100°C	93	
Pulsed Drain Current	I <sub>DM</sub>	370	A	
Avalanche Energy, Single Pulse @ L=0.4mH, T <sub>C</sub> =25°C	E <sub>AS</sub>	720	mJ	
Power Dissipation @ T <sub>C</sub> =25°C	P <sub>D</sub>	429	W	
Operating Junction Temperature	T <sub>J</sub>	-55/175	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/175	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	60	°C/W	
Thermal Resistance-Junction to Case	R <sub>θJC</sub>	0.35	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	200			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=200V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=200V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		9.4	11	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$		70		S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}=\text{Open},$ $f=1\text{MHz}$		4.0		Ω
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$		0.9		V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=100V, V_{GS}=10V$ $I_D=20A$		56		nC
Gate-Source Charge	$Q_{gs}$			18		
Gate-Drain Charge	$Q_{gd}$			5		
Input Capacitance	$C_{iss}$	$V_{DS}=100V, V_{GS}=0V$ $f=1\text{MHz}$		4970		pF
Output Capacitance	$C_{oss}$			420		
Reverse Transfer Capacitance	$C_{rss}$			7.5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=100V, V_{GS}=10V$ $I_D=20A, R_G=10\Omega$		16		nS
	$t_r$			22		
Turn-Off Time	$t_{d(off)}$			38		
	$t_f$			10		



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### TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

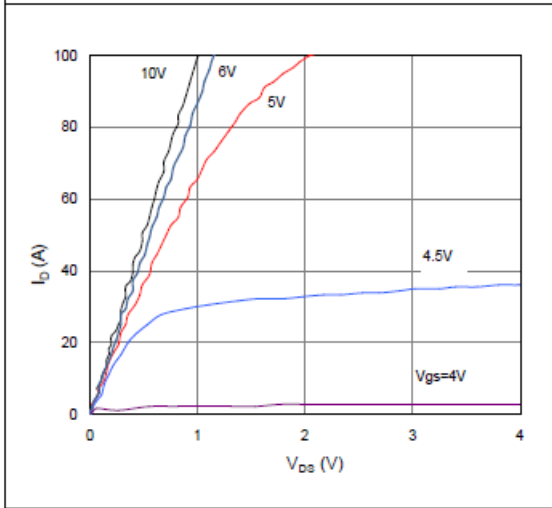


Figure 2. On-Resistance vs. Gate-Source Voltage

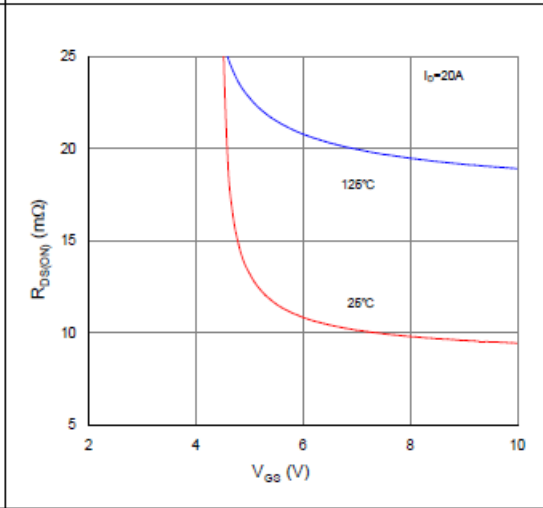


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

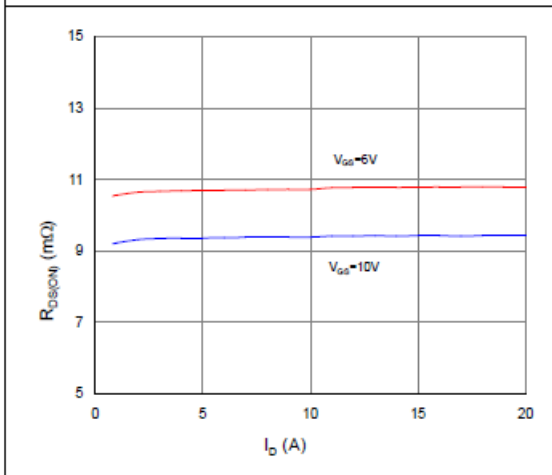


Figure 4. Normalized On-Resistance vs. Junction Temperature

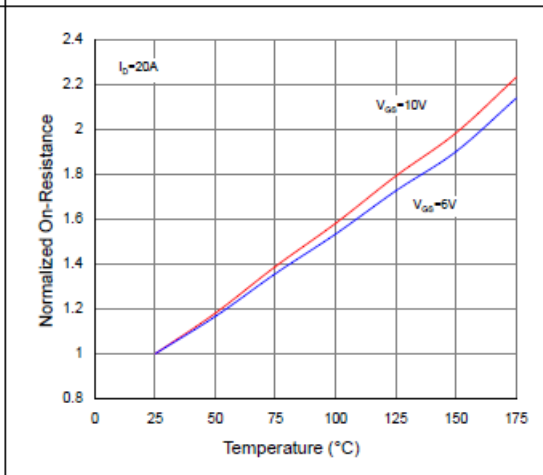


Figure 5. Typical Transfer Characteristics

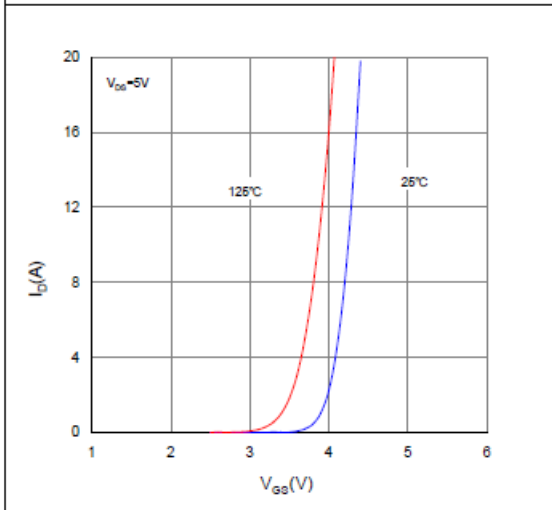
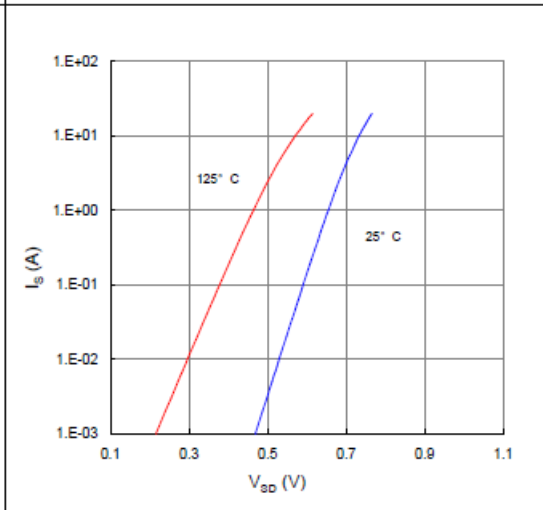


Figure 6. Typical Source-Drain Diode Forward Voltage





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### TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

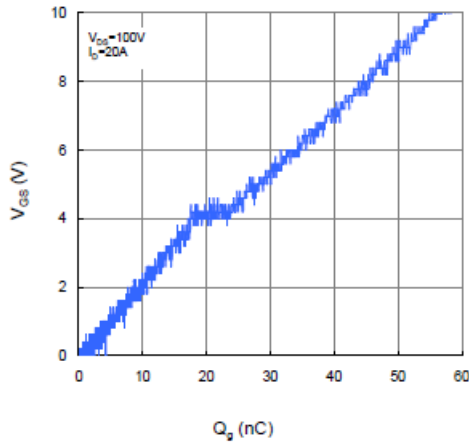


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

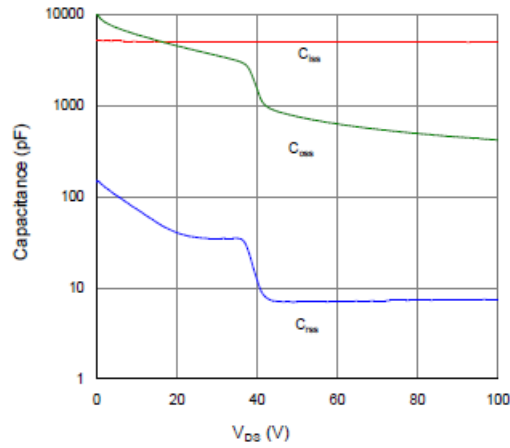


Figure 9. Maximum Safe Operating Area

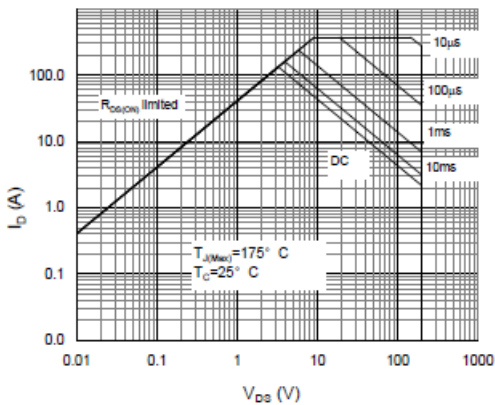


Figure 10. Maximum Drain Current vs. Case Temperature

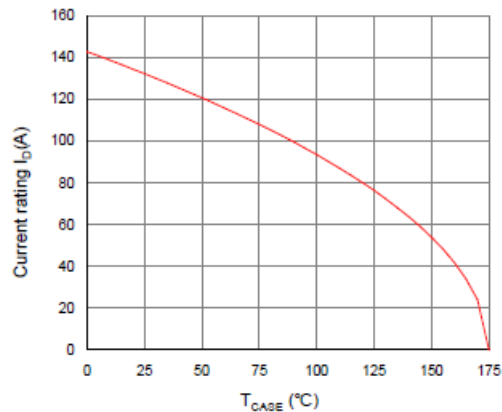
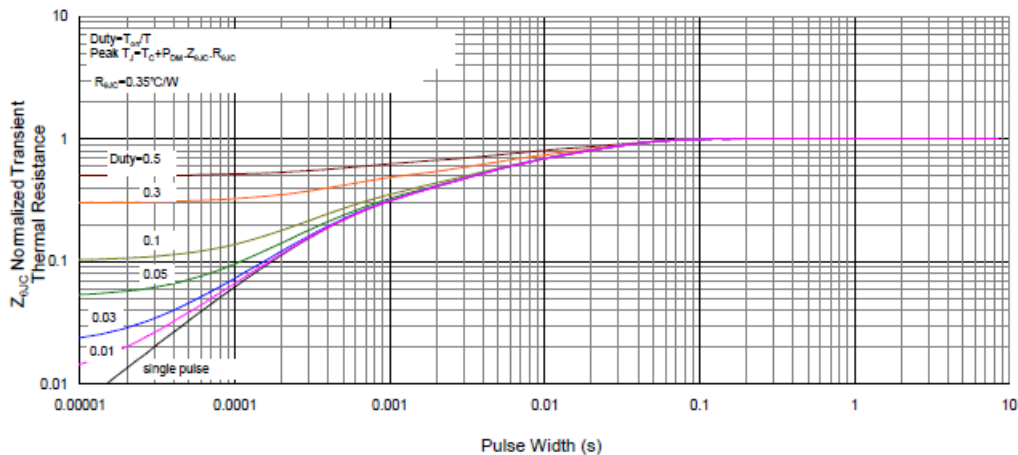


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

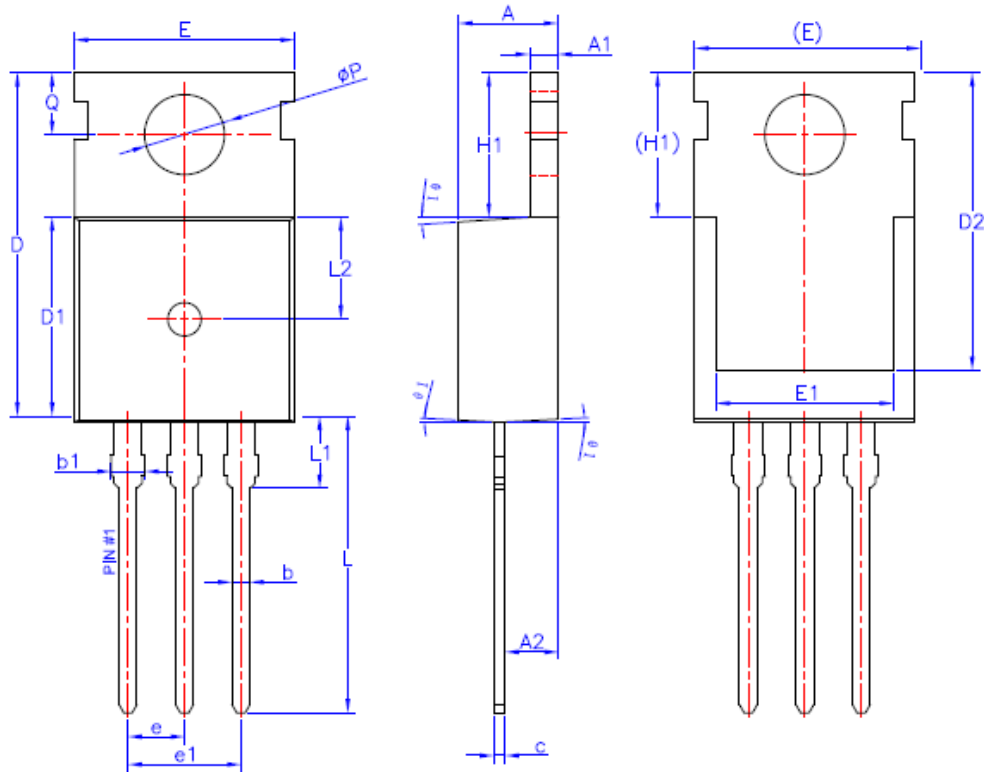




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## N-Channel Enhancement Mode MOSFET

### TO-220-3L PACKAGE OUTLINE



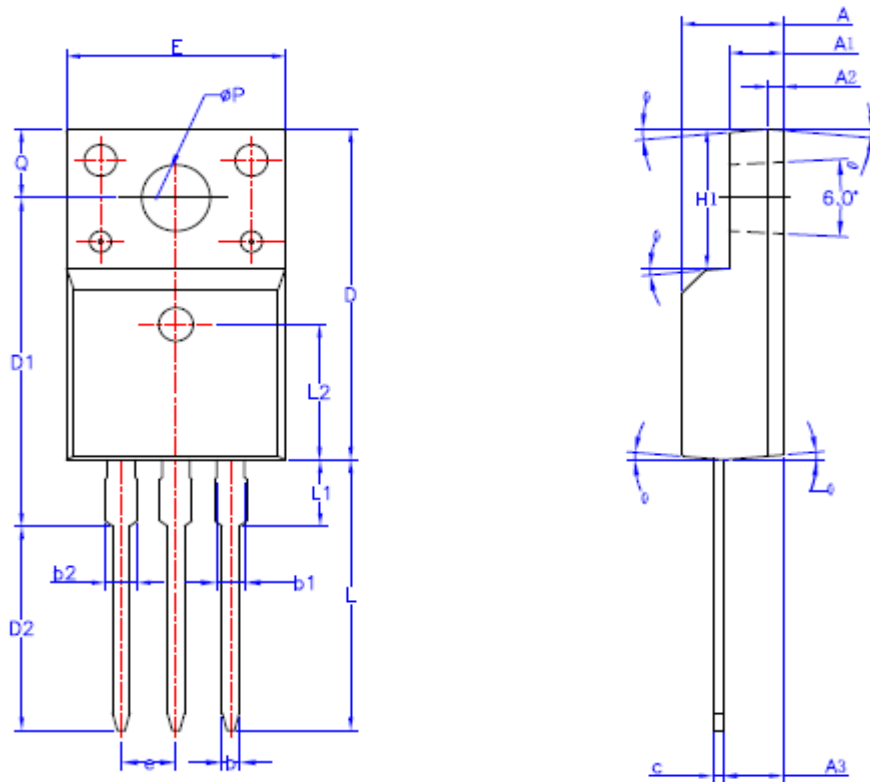
SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.27	—	1.40
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
$\phi P$	3.55	3.60	3.65
Q	2.73	—	2.87
#1	1°	3°	5°



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### TO-220F-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.83
A1	2.34	2.54	2.74
A2	0.70 REF		
A3	2.56	2.76	2.93
b	0.70	—	0.90
b1	1.18	—	1.38
b2	—	—	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	9.60	9.80	10.0
E	9.96	10.16	10.36
e	2.54BSC		
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	—	—	3.50
L2	6.50REF		
∅P	3.08	3.18	3.28
Q	3.20	—	3.40
θ 1	1°	3°	5°



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