



SPN150N04

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN150N04 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

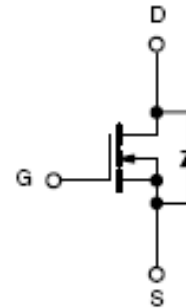
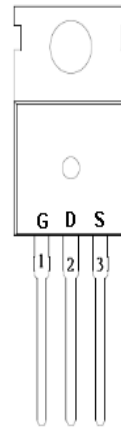
- ◆ 40V/150A, $R_{DS(ON)}=3.0m\Omega@V_{GS}=10V$
- ◆ 40V/150A, $R_{DS(ON)}=3.9m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L package design

APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

PIN CONFIGURATION

TO-220-3L



PART MARKING



A : Lot Code
B : Date Code



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T0-220-3L PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN150N04T220TGB	TO-220-3L	SPN150N04

※ SPN150N04T220TGB : Tube ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	40	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	I _D	T _C =25°C	150
		T _C =70°C	120
Pulsed Drain Current	I _{DM}	480	A
Power Dissipation	P _D	T _C =25°C	83
Power Dissipation		T _C =70°C	53
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	1.5	°C/W



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.9	2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$ $T_J=25^\circ C$			1	μA
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$			3.0	m Ω
		$V_{GS}=4.5V, I_D=20A$			3.9	
Diode Forward Voltage	V_{SD}	$I_F=1A, V_{GS}=0V$			1.3	V
Dynamic						
Total Gate Charge (10V)	Q_g	$V_{DS}=20V, V_{GS}=20V$ $I_D=30A$		79.5		nC
Gate-Source Charge	Q_{gs}			23.2		
Gate-Drain Charge	Q_{gd}			4.89		
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V$ $f=1MHz$		4264		pF
Output Capacitance	C_{oss}			897		
Reverse Transfer Capacitance	C_{rss}			401		
Turn-On Time	$t_d(on)$	$V_{DD}=20V, I_D=30A$ $V_{GEN}=10V, R_G=3\Omega$		22		nS
	t_r			7		
Turn-Off Time	$t_d(off)$			99		
	t_f			18		

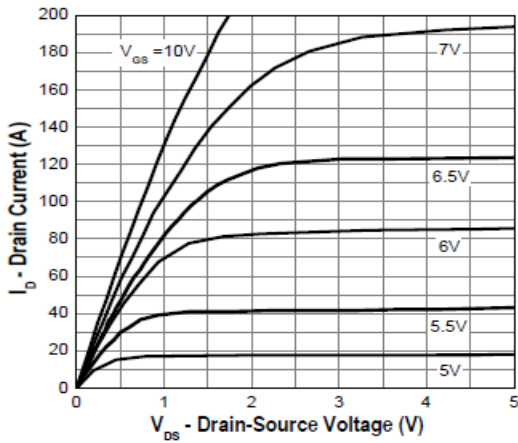


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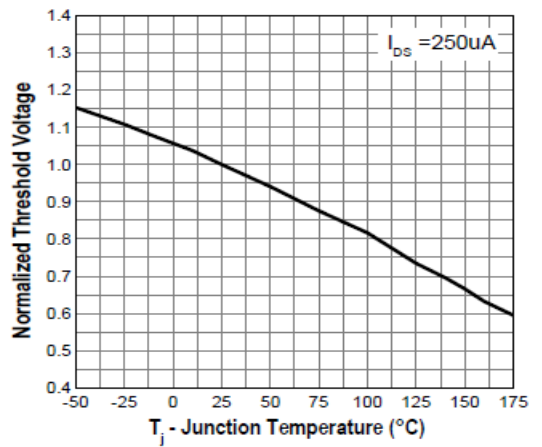
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TYPICAL CHARACTERISTICS

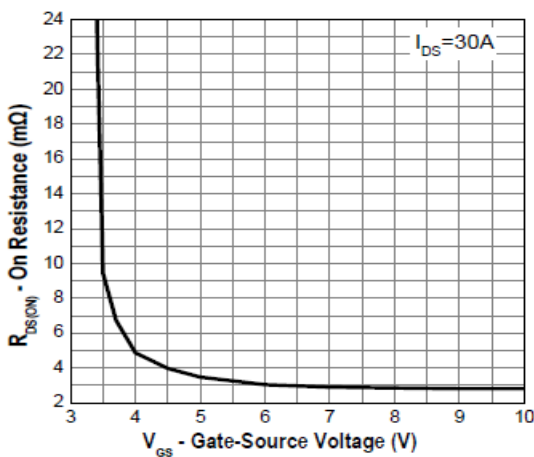
Output Characteristics



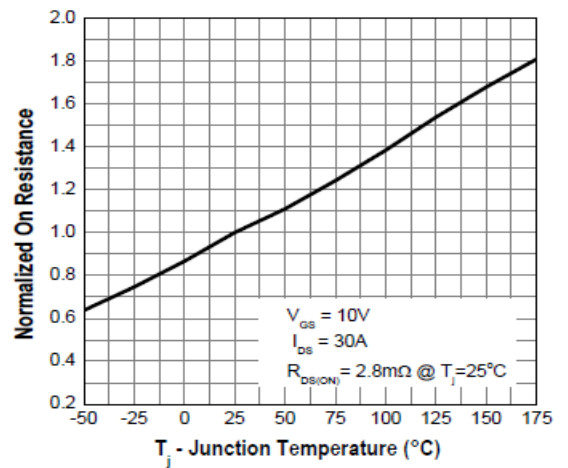
Gate Threshold Voltage



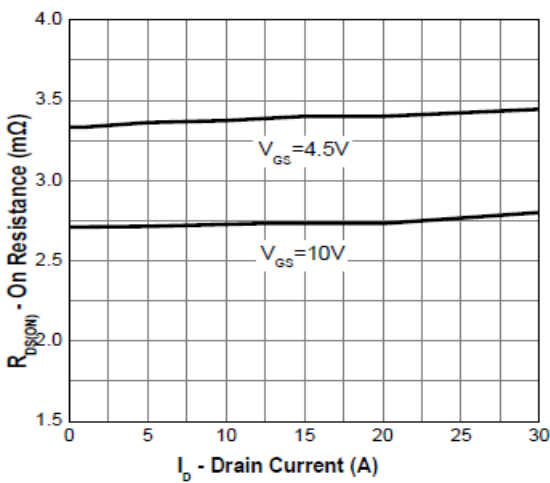
Gate-Source On Resistance



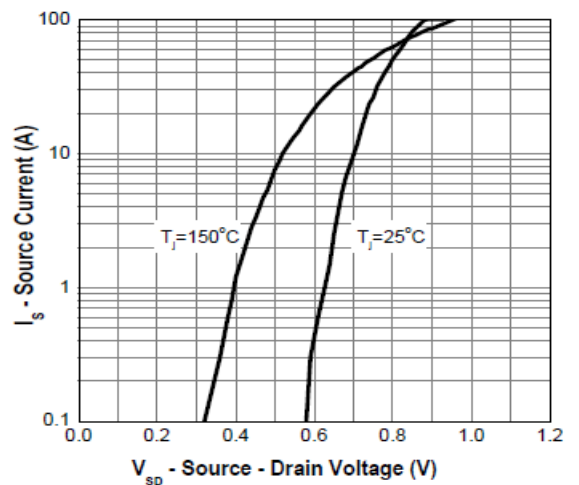
Drain-Source On Resistance



Drain-Source On Resistance



Source-Drain Diode Forward



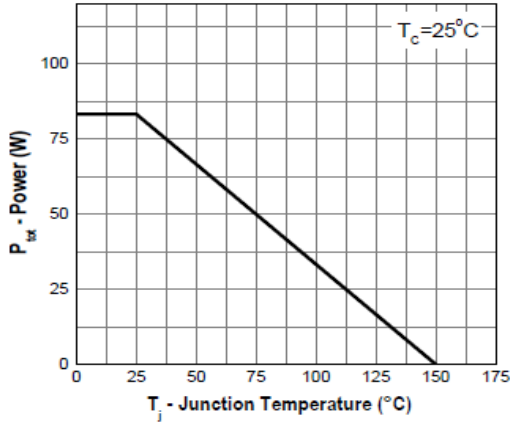


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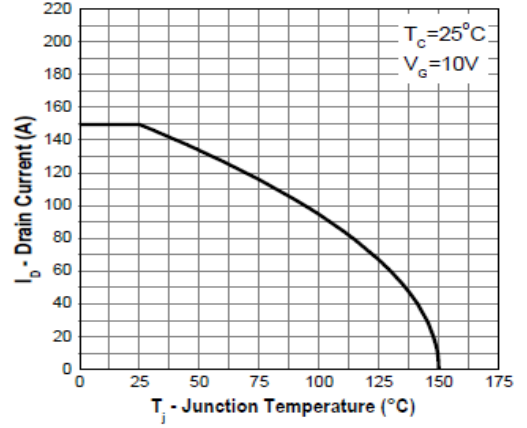
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TYPICAL CHARACTERISTICS

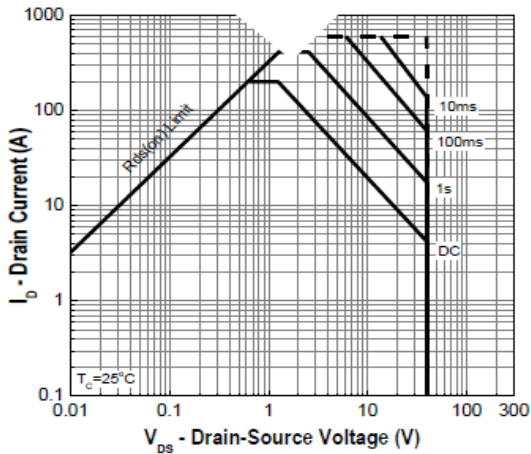
Power Dissipation



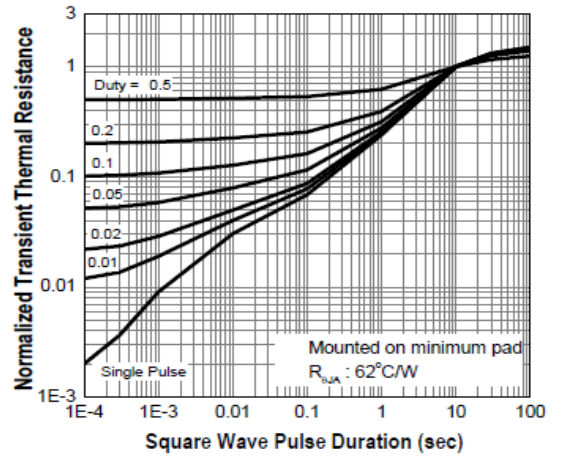
Drain Current



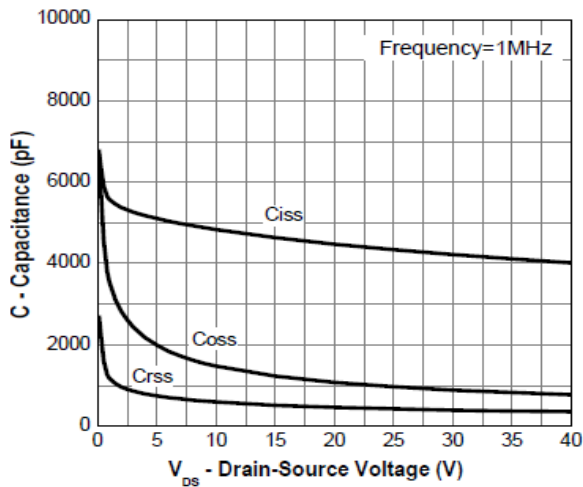
Safe Operation Area



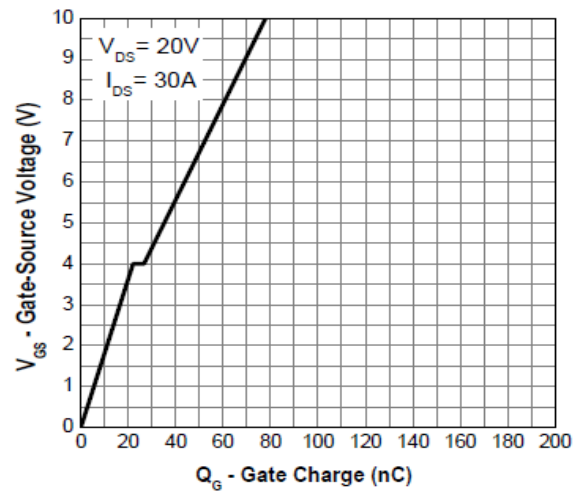
Transient Thermal Impedance



Capacitance



Gate Charge

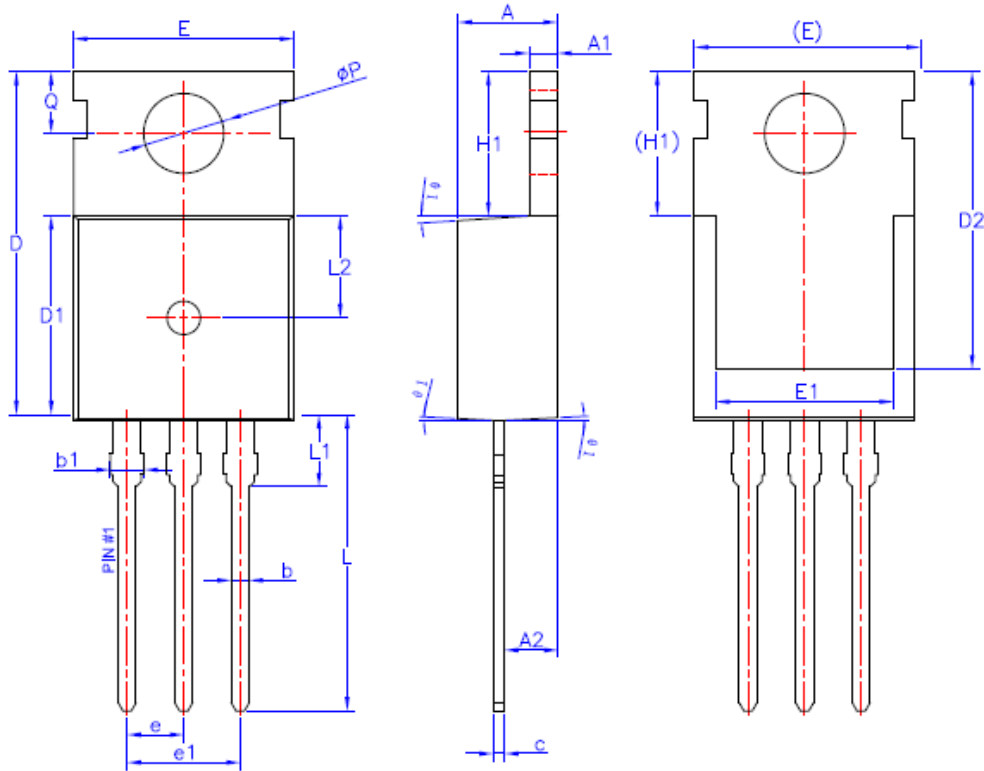




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TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	0.60	0.90
b1	-	-	1.40
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	-	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	-	-	3.50
L2	4.6REF		
ϕP	3.55	3.60	3.65
Q	2.73	-	2.87
$\theta 1$	1°	3°	5°



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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