



SPN4856

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4856 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching .

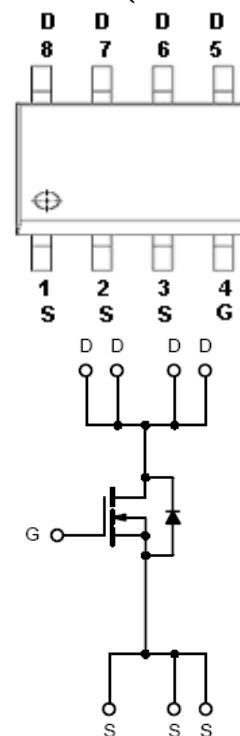
FEATURES

- ◆ 45V/15A, $R_{DS(ON)}=12m\Omega@V_{GS}=10V$
- ◆ 45V/15A, $R_{DS(ON)}=15m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8P package design

APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- Charger Adapter
- LED Lighting

PIN CONFIGURATION(SOP-8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4856S8RGB	SOP-8P	SPN4856

※ SPN4856S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	45	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current	TA=25°C	I _D	15	A
	TA=100°C		9.5	
Continuous Drain Current (Silicon Limited) TA=25°C		I _D	35	A
Pulsed Drain Current		I _{DM}	60	A
Single Pulse Avalanche Energy		E _{AS}	38	mJ
Avalanche Current		I _{AS}	27	A
Power Dissipation	TA=25°C	P _D	2.5	W
	TA=70°C		1.4	
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	50	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	45			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.8		1.8	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =36V, V _{GS} =0V, T _J =25°C			1	μA
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =1A			12	mΩ
		V _{GS} =4.5V, I _D =1A			15	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =6A		25		S
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V	0.4		1.0	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =20V, V _{GS} =10V I _D =13.3A		31.5		nC
Gate-Source Charge	Q _{gs}			3.5		
Gate-Drain Charge	Q _{gd}			9		
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V f=1MHz		1600		pF
Output Capacitance	C _{oss}			180		
Reverse Transfer Capacitance	C _{rss}			130		
Turn-On Time	t _{d(on)}	V _{DD} =20V, I _D =13.3A, V _{GS} =10V R _G =6Ω		12		nS
	t _r			82		
Turn-Off Time	t _{d(off)}			33		
	t _f			59		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.2		Ω

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=27A, R_G=25Ω, Starting T_J=25°C
3. The data tested by pulsed, pulse width ≤300μs, duty cycle ≤2%.
4. Essentially independent of operating temperature.



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TYPICAL CHARACTERISTICS

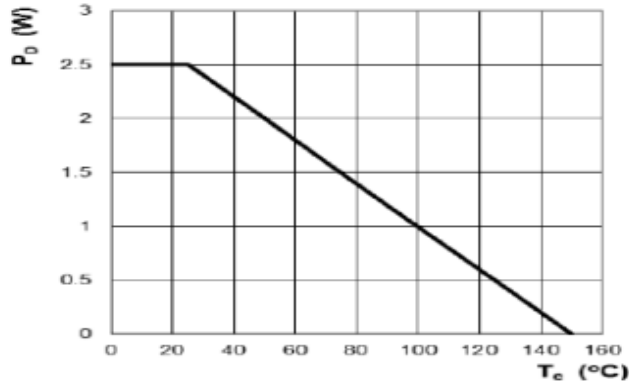


Figure 1: Power Dissipation

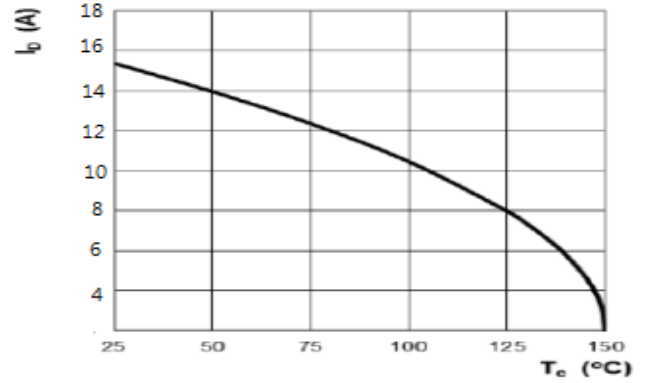


Figure 2: Continuous Drain Current vs. T_c

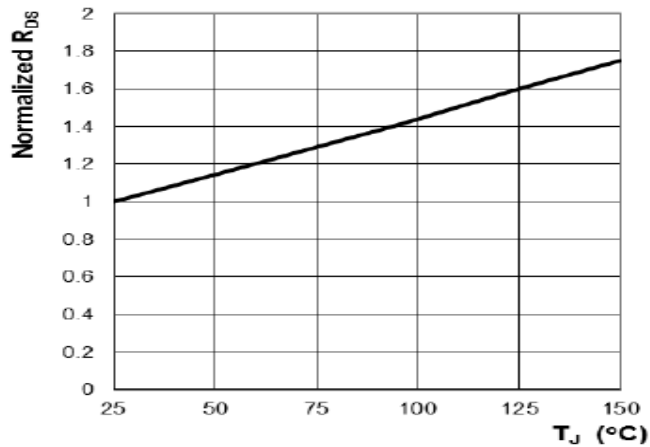


Figure 3: Normalized $R_{DS(ON)}$ vs. T_J

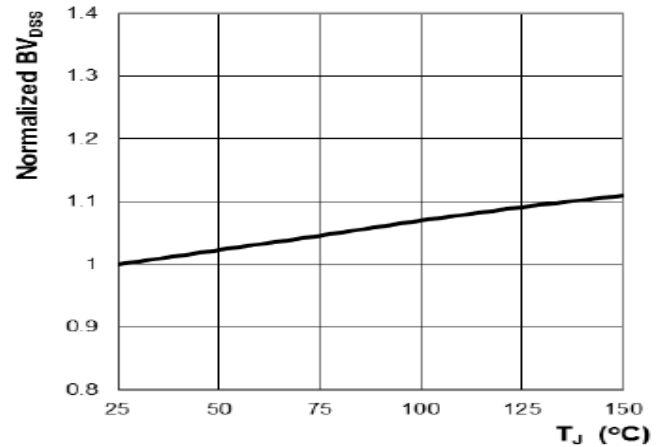


Figure 4: Normalized BV_{DSS} vs. T_J

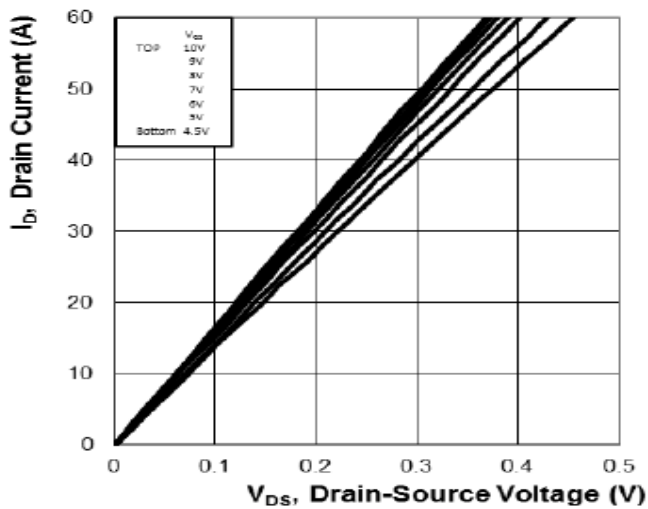


Figure 5: On-Region Characteristics

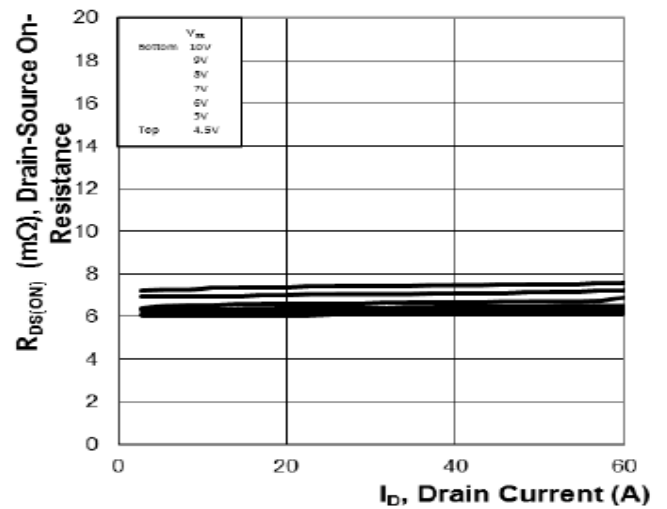


Figure 6: Typ. R_{DS} Variation vs. I_D and V_{GS}



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TYPICAL CHARACTERISTICS

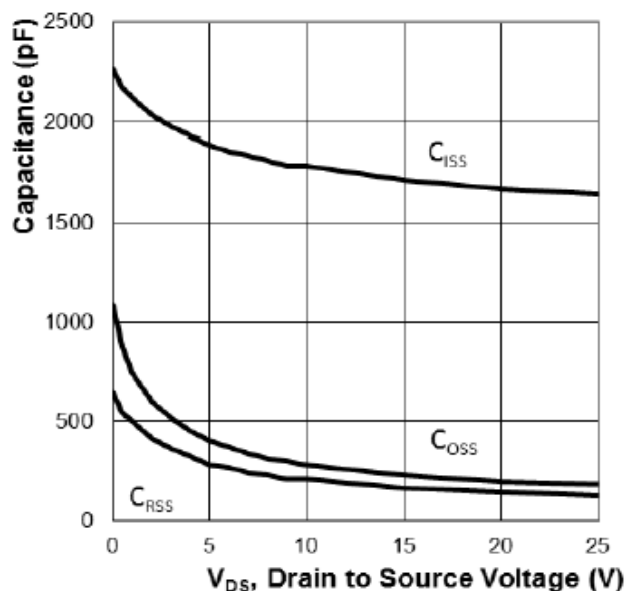


Figure 7: Typ. Capacitance Characteristics

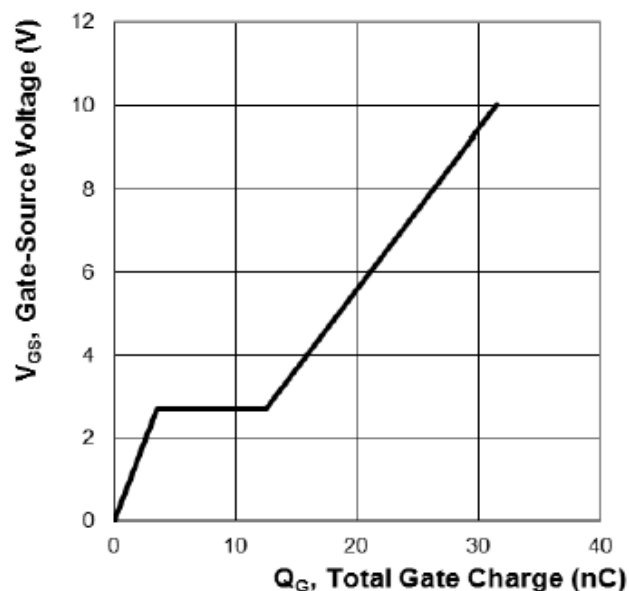


Figure 8: Typ. Gate Charge Characteristics

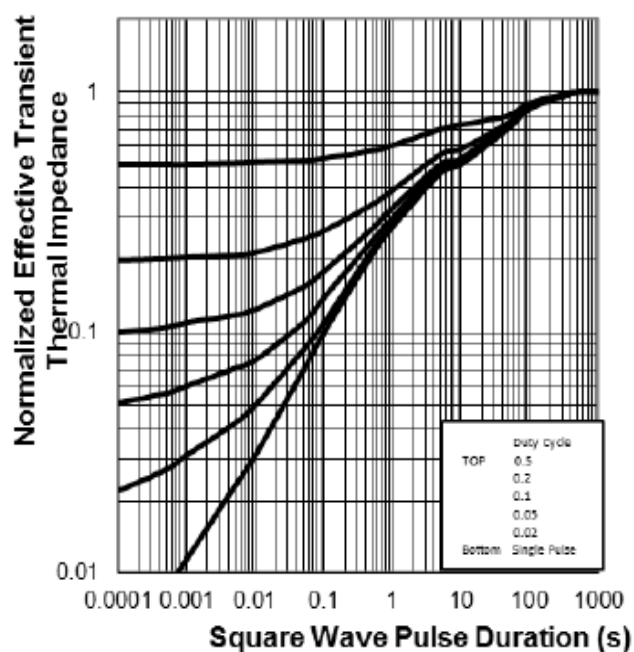


Figure 9: Normalized Thermal Transient Impedance, Junction-to-Case

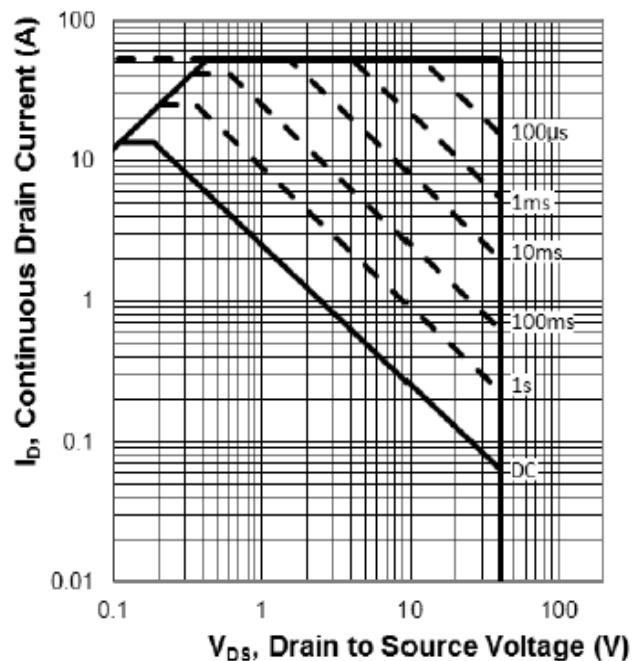


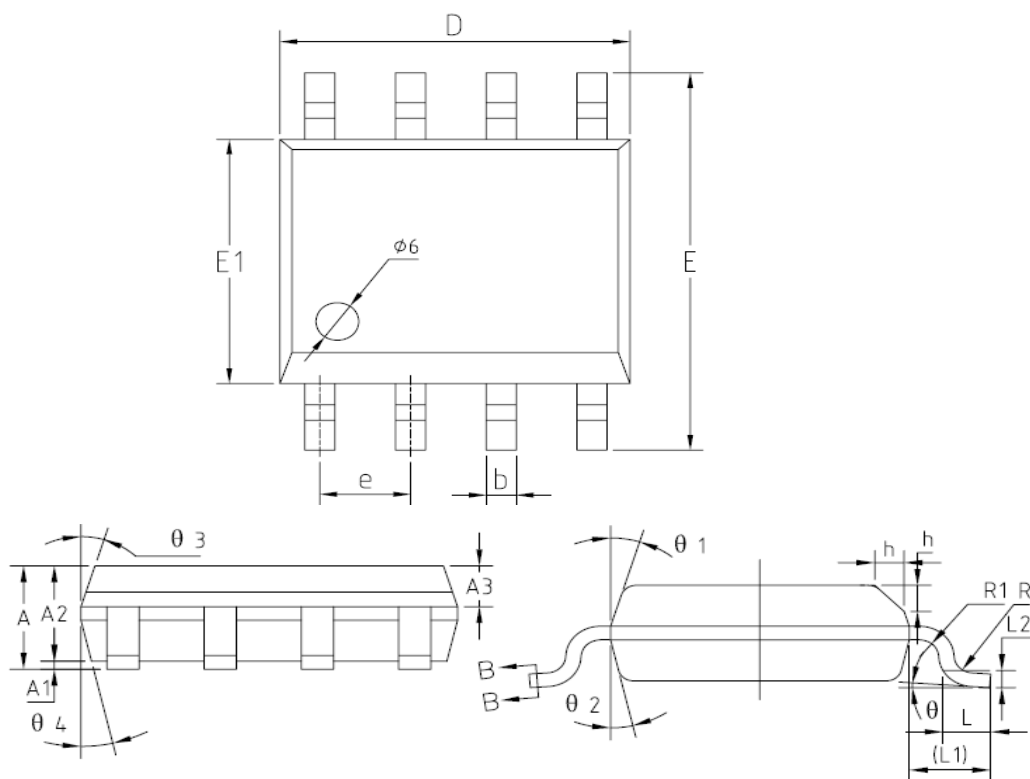
Figure 10: Maximum Safe Operation Area



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SOP- 8 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	1.35	--	1.75
A1	0.10	--	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.33	-	0.51
c	0.17	--	0.25
D	4.80	4.93	5.05
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25BSC		
R	0.07	--	--
R1	0.07	--	0.20
h	0.25	--	0.50
θ	0°	--	8°
$\theta 1$	15°	17°	19°
$\theta 2$	11°	13°	15°
$\theta 3$	15°	17°	19°
$\theta 4$	11°	13°	15°



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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