



# SPN50T10

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN50T10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN80T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

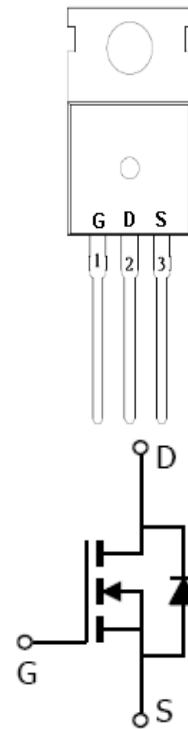
- ◆ 100V/65A,  $R_{DS(ON)}=18m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L package design

### APPLICATIONS

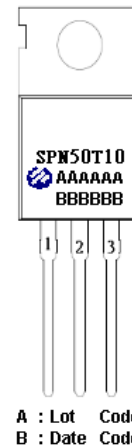
- Powered System
- DC/DC Converter
- Load Switch

### PIN CONFIGURATION

TO-220-3L



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN50T10T220TGB	TO-220-3L	SPN50T10

※ SPN50T10T220TGB : Tube ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	65	A
		TA=70°C	40	
Pulsed Drain Current	I <sub>DM</sub>	200	A	
Power Dissipation @ TA=25°C	P <sub>D</sub>	166	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	62	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$			25	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$			18	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=10V, I_D=30A$		75		S
Diode Forward Voltage	$V_{SD}$	$I_S=30A, V_{GS}=0V$			1.3	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=80V, V_{GS}=10V$ $I_D=40A$		115	180	nC
Gate-Source Charge	$Q_{gs}$			20		
Gate-Drain Charge	$Q_{gd}$			48		
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		6000	9600	pF
Output Capacitance	$C_{oss}$			550		
Reverse Transfer Capacitance	$C_{rss}$			300		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=1\Omega$ $I_D=30A, V_{GEN}=10V$ $R_G=1.66\Omega$		21		nS
	$t_r$			58		
Turn-Off Time	$t_{d(off)}$			41		
	$t_f$			15		



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## TYPICAL CHARACTERISTICS

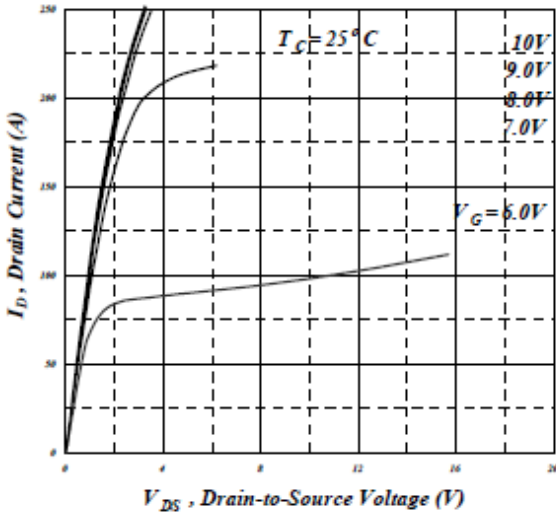


Fig 1. Typical Output Characteristics

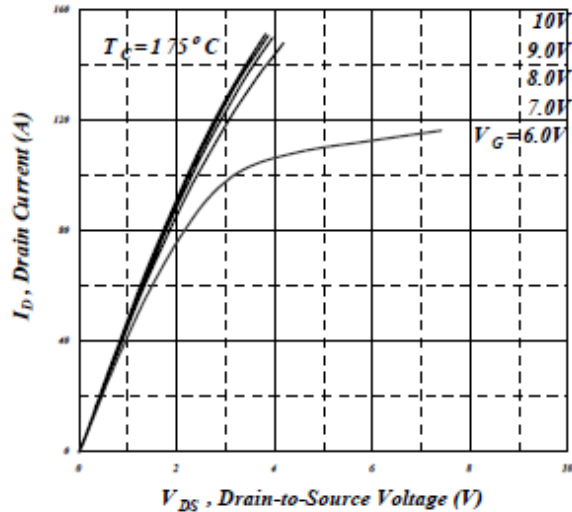


Fig 2. Typical Output Characteristics

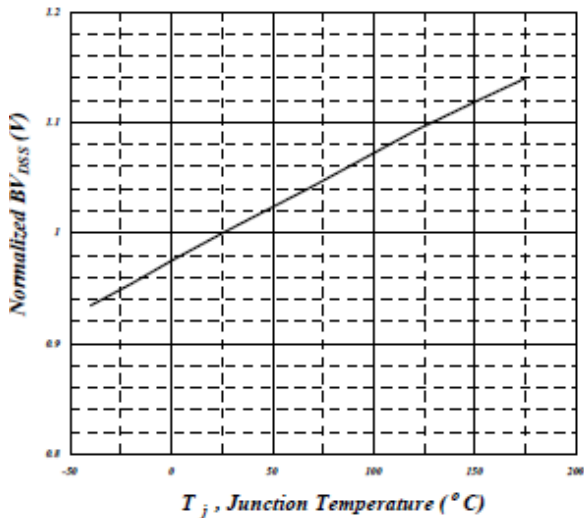


Fig 3. Normalized  $BV_{DSS}$  v.s. Junction Temperature

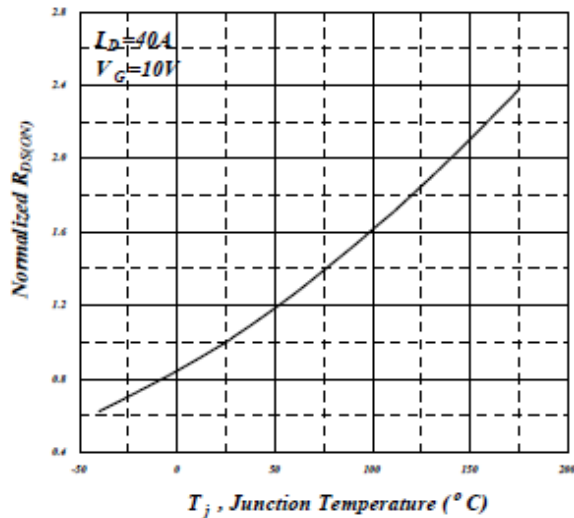


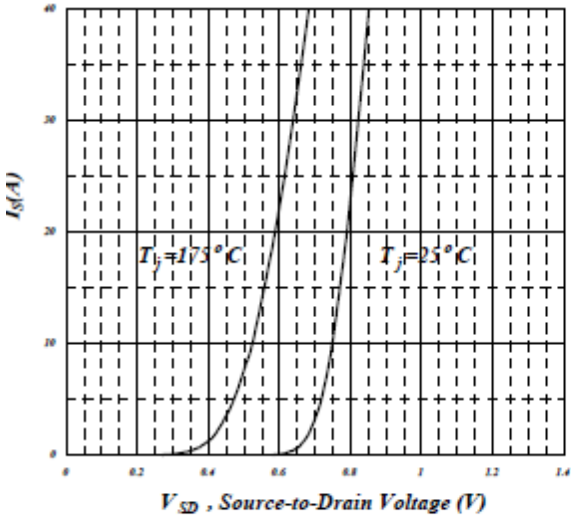
Fig 4. Normalized On-Resistance v.s. Junction Temperature



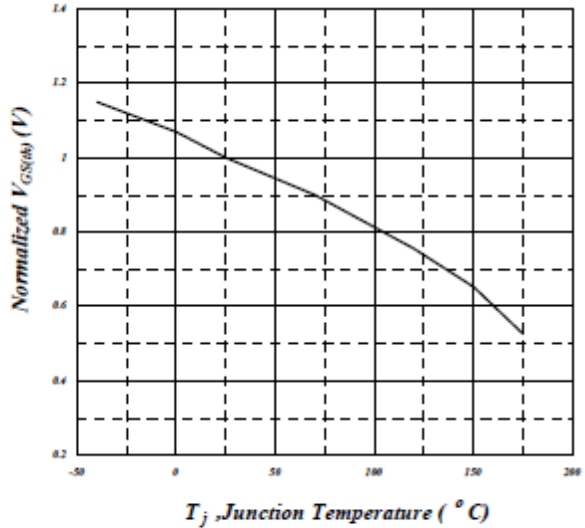
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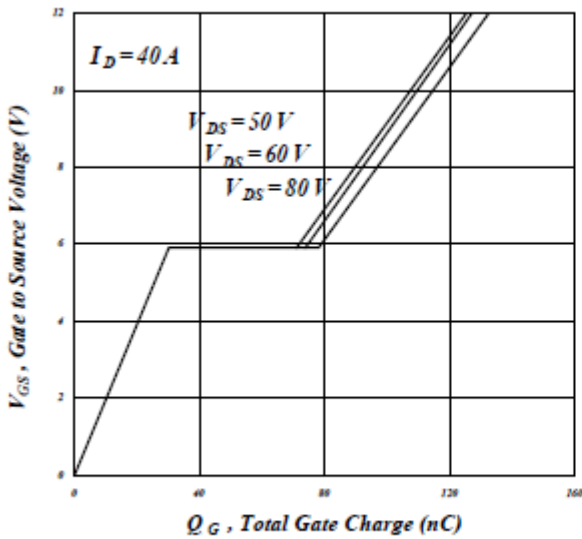
### TYPICAL CHARACTERISTICS



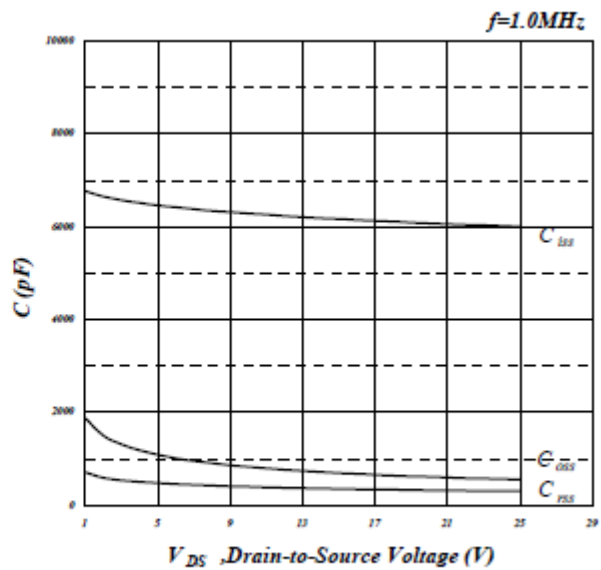
**Fig 5. Forward Characteristic of Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



**Fig 7. Gate Charge Characteristics**



**Fig 8. Typical Capacitance Characteristics**



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## TYPICAL CHARACTERISTICS

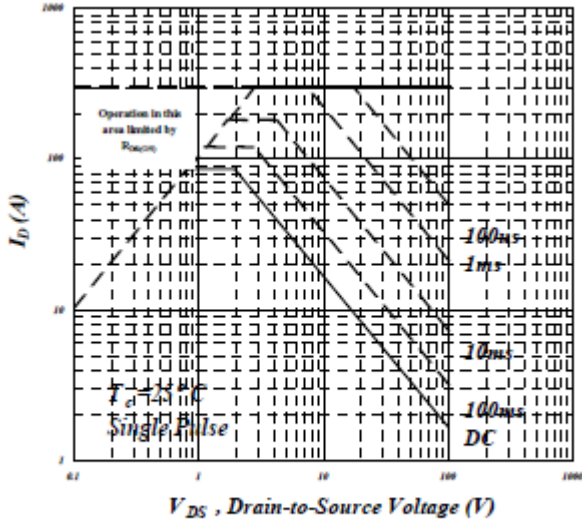


Fig 9. Maximum Safe Operating Area

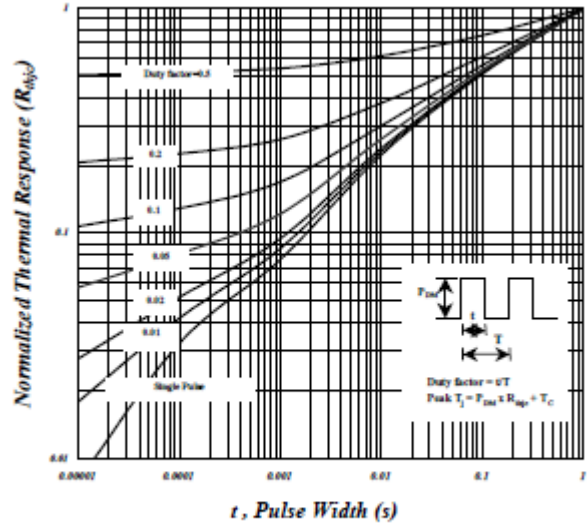


Fig 10. Effective Transient Thermal Impedance

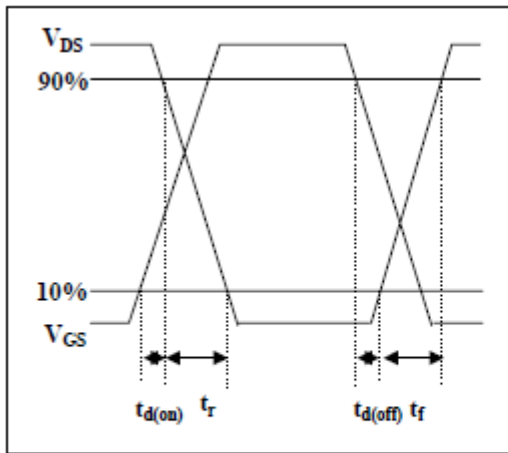


Fig 11. Switching Time Waveform

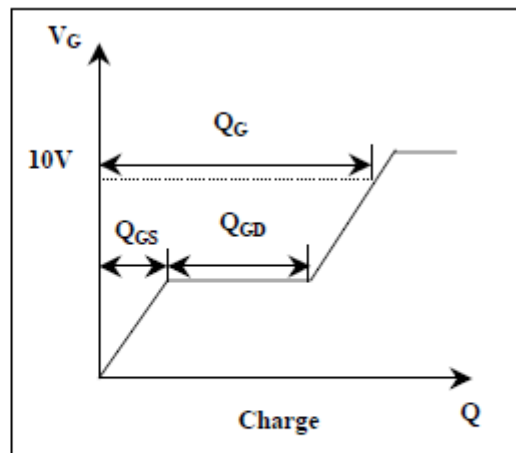


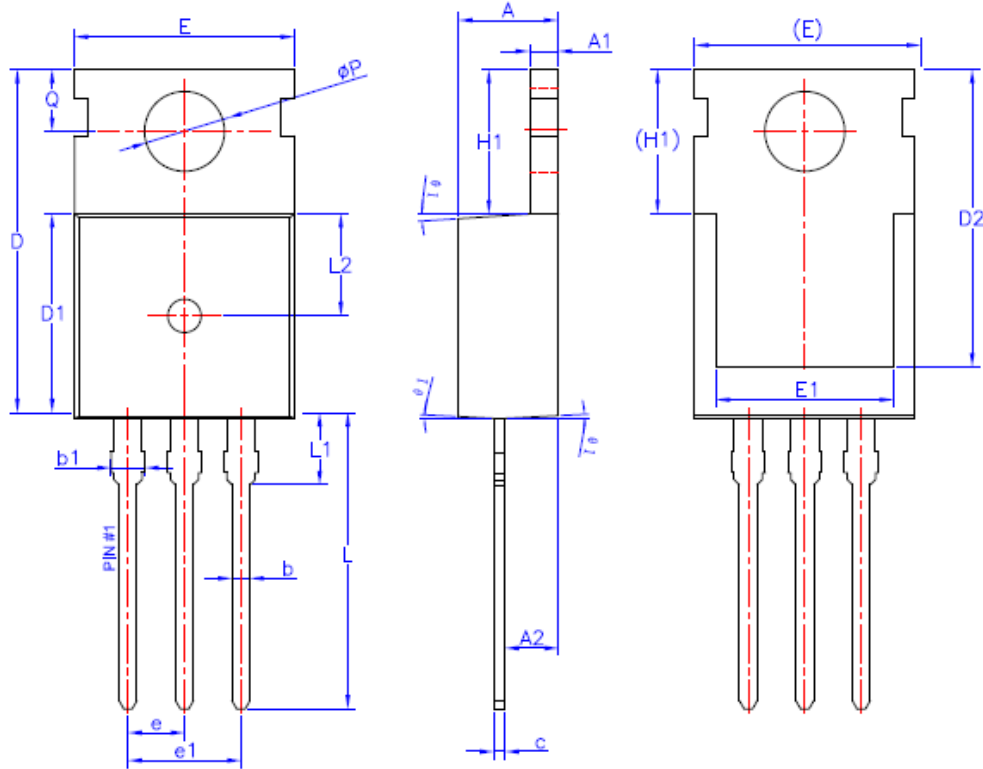
Fig 12. Gate Charge Waveform



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### TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.42	—	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
φP	3.55	3.60	3.65
Q	2.73	—	2.87
φ 1	1°	3°	5°



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