



SPN6242

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN6242 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

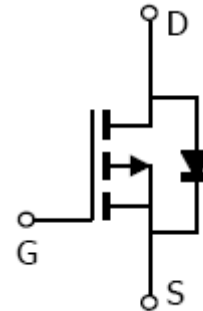
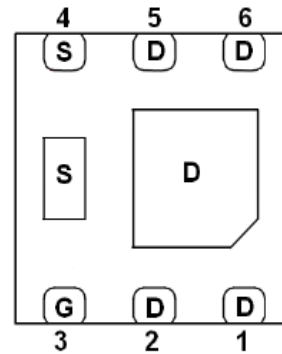
FEATURES

- ◆ 20V/3.3A, $R_{DS(ON)}=19m\Omega@V_{GS}=4.5V$
- ◆ 20V/2.8A, $R_{DS(ON)}=24m\Omega@V_{GS}=2.5V$
- ◆ 20V/2.3A, $R_{DS(ON)}=32m\Omega@V_{GS}=1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ UDFN2x2-6L package design

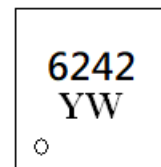
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(UDFN2x2-6L)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN6242UDN6RGB	UDFN2x2-6L	6242YW

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPN6242UDN6RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	20	V
Gate –Source Voltage	V _{GSS}	±10	V
Continuous Drain Current(T _J =150°C)	I _D	T _C =25°C	6.7
		T _C =100°C	4.2
Pulsed Drain Current (*1)	I _{DM}	26.8	A
Continuous Source Current(Diode Conduction)	I _S	6.7	A
Power Dissipation	P _D	T _A =25°C	1.9
		T _A =70°C	1.2
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	65	°C/W



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ELECTRICAL CHARACTERISTICS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.3	0.6	0.8	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 10V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V, T_J=25^\circ C$			1	uA
		$V_{DS}=16V, V_{GS}=0V, T_J=125^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=3.3A$		15	19	mΩ
		$V_{GS}=2.5V, I_D=2.8A$		18	24	
		$V_{GS}=1.8V, I_D=2.3A$		23	32	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=4A$		9.5		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V, T_J=25^\circ C$			1	V
Dynamic						
Total Gate Charge (*2,3)	Q_g	$V_{DS}=10V, V_{GS}=4.5V, I_D=4A$		5.8	8	nC
Gate-Source Charge (*2,3)	Q_{gs}			0.6	1	
Gate-Drain Charge (*2,3)	Q_{gd}			2	4	
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		600	870	pF
Output Capacitance	C_{oss}			70	100	
Reverse Transfer Capacitance	C_{rss}			45	65	
Turn-On Time (*2,3)	$t_{d(on)}$	$V_{DD}=10V, I_D=1A, V_{GEN}=4.5V, R_G=25\Omega$		5.0	9	nS
	t_r			14.4	27	
Turn-Off Time (*2,3)	$t_{d(off)}$			30	55	
	t_f			9.2	17	

Note :

- 1.Repetitive Rating : Pulsed width limited by maximum junction temperature.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.Essentially independent of operating temperature.



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TYPICAL CHARACTERISTICS

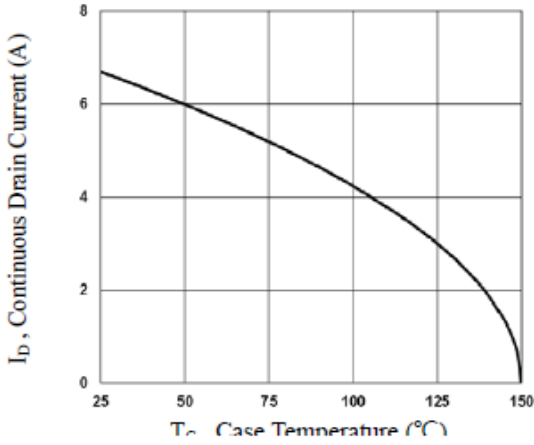


Fig.1 Continuous Drain Current vs. T_C

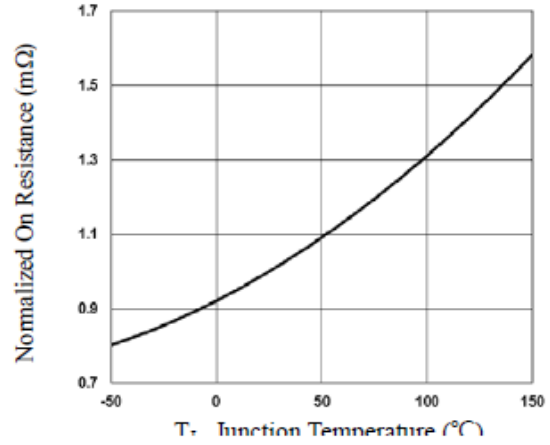


Fig.2 Normalized RDSON vs. T_J

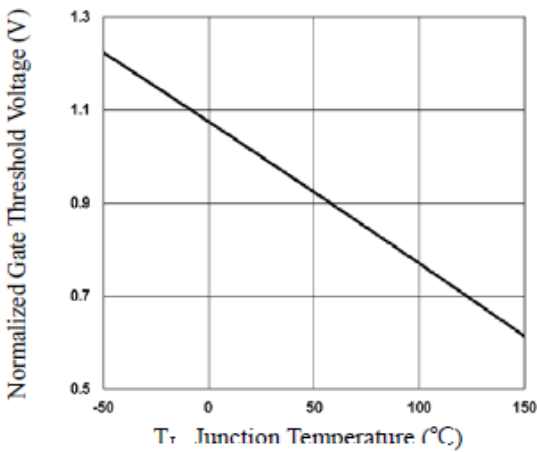


Fig.3 Normalized V_{th} vs. T_J

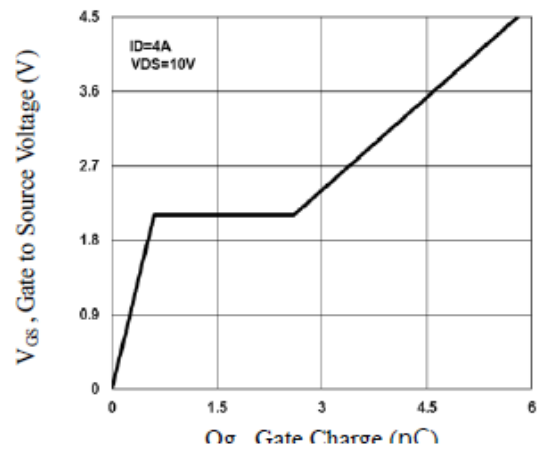


Fig.4 Gate Charge Waveform

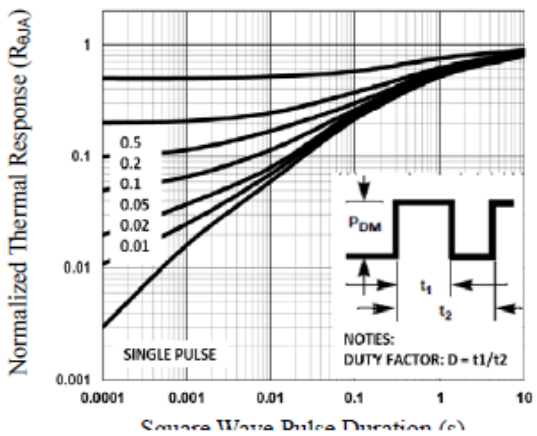


Fig.5 Normalized Transient Impedance

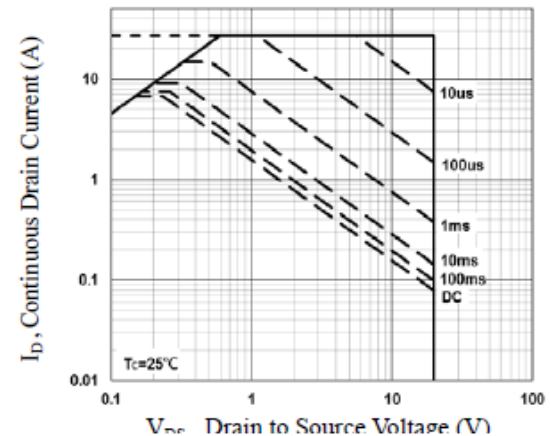


Fig.6 Maximum Safe Operation Area



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TYPICAL CHARACTERISTICS

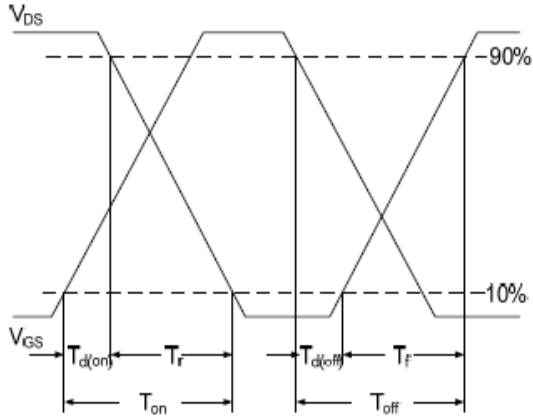


Fig.7 Switching Time Waveform

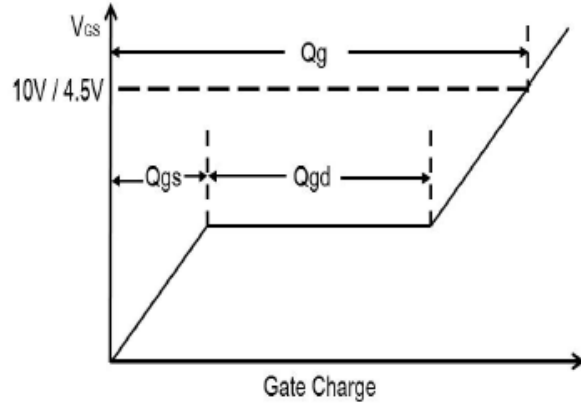
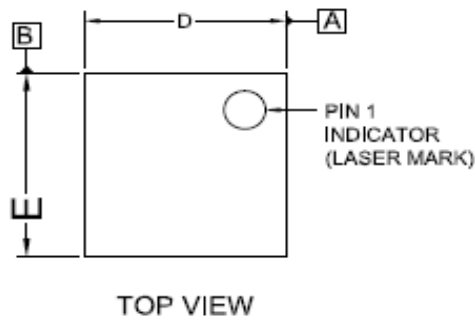
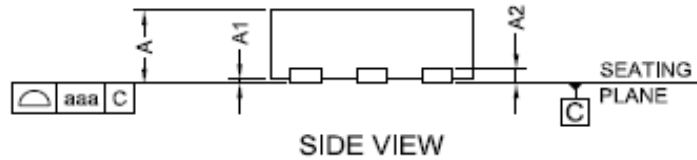
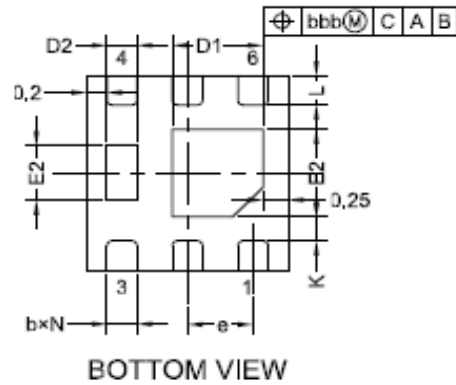


Fig.8 Gate Charge Waveform



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UDFN2X2-6L PACKAGE OUTLINE



SYMBOL	MIN	TYP	MAX
A	0,50	0,55	0,60
A1	0,00	0,02	0,05
A2	0,152REF.		
b	0,25	0,30	0,35
D	1,95	2,00	2,05
D1	0,80	0,90	1,00
D2	0,25	0,30	0,35
E	1,95	2,00	2,05
E1	0,80	0,90	1,00
E2	0,46	0,56	0,66
e	0,65BSC		
L	0,25	0,30	0,35
J	0,40BSC		
K	0,20MIN		
N	6		
aaa	0,08		
bbb	0,10		



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